

# A Physics-Based Compact Model of SiC Power MOSFETs

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**Abstract** - The presented compact model of SiC power MOSFETs is based on a thorough consideration of the physical phenomena which are important for the device characteristics and its electro-thermal behavior. The model includes descriptions of the dependence of channel charge and electron mobility on the charge of interface traps and a simple but effective calculation of the voltage-dependent drain resistance. Comparisons with both physical 2D device simulations and experiments validate the correctness of the modeling approach and the accuracy of the results.

**Index terms** - Compact model, drain resistance, interface traps, Power MOSFET, silicon carbide.

## I. INTRODUCTION

Power devices with wide-bandgap semiconductor materials have superior properties in comparison to equivalent silicon (Si-) devices. The silicon-carbide (SiC-) power MOSFET is particularly an interesting component for high voltage, high temperature, high power, and high frequency power electronic applications due to its non-dissipative gate control terminal and to the availability of an intrinsic body-diode structure that can be used for freewheeling of inductive currents.

SiC power MOSFETs are now commercially available from multiple sources and circuit designers can explore their benefits. But the different characteristics of SiC-MOSFETs compared to Si-devices require special care to fully utilize their advantages and to avoid problems. Their relatively low transconductance value makes high gate voltages necessary; their low resistance, the fast switching and the absence of a tail current (compared to IGBTs) can cause ringing and higher voltage overshoots.

Therefore, it is very important for circuit designers to have the opportunity of investigating these issues with the help of circuit simulations. For this purpose accurate and reliable models are necessary; they must be valid for all conditions of operation which can occur in the different possible applications, without compromising on computational efficiency to enable investigations of realistic multi-chip structures including parasitic elements associated with layout and packaging.

A review of SiC MOSFET models presented in the literature so far can be found in [1]. Many models are substantially the same as the models for Si MOSFETs [2]-[11]; they are adjusted to reproduce the special SiC characteristics with different parameters and/ or with some additional empirical functions which are not based on the

physical effects underlying their characteristics. Recently some models have been published which try to consider the special effects occurring in SiC MOSFETs. Effects caused by interface traps are taken into account in [12] and [13]; [13] describes the influence of traps on the threshold voltage whereas [12] considers the variation of the electron mobility due to the traps. The variable drain resistance is modelled in [12]-[15]; a short discussion of these models is given in section II.B.

Various very detailed physical models have been developed for the purpose of device simulations [16]-[18], but due to the large computational effort they are not suited for the simulation of complex circuits.

This paper presents a model which is a compromise between model accuracy and computational effort. The model is based on a description of the physical effects in SiC MOSFETs, but simplifications are made to obtain simple results requiring only few parameters and enabling high simulation speed.

The main new features of this model are:

- the influence of interface traps on the electron density and electron mobility in the MOSFET channel is taken into account,
- the variation of the resistance of the drain drift region due to non-uniform current distribution and velocity saturation of the electrons is described; this resistance is important for the saturation characteristic of the device.

To analyze the physical effects and their influence on the device behavior device simulations have been performed with the simulation tool SENTAURUS [19].

## II. MODEL DESCRIPTION

Fig. 1 shows the structure of a SiC Power MOSFET (unit cell) with the flow of the electrons inside the device.

The structure of the model is shown in Fig. 2. It is realized as a subcircuit consisting of controlled current and voltage sources and some passive elements. The controlled sources provide currents (or voltages, respectively) which can depend on various voltages between nodes of the electrical subcircuit and also on the voltages of one or several nodes of the thermal equivalent circuit (e.g.  $T_1$ ). The voltages of the thermal equivalent circuit correspond to the temperature change inside the MOSFET structure due to self-heating [20, 21]. In this way the influence of a variable temperature on the model parameters is taken into account. The model is completed by adding inductors at the nodes of drain, gate and source which represent the parasitic inductances associated with the device package. The parasitic package resistances are included in  $R_g$ ,  $R_s$ , and the

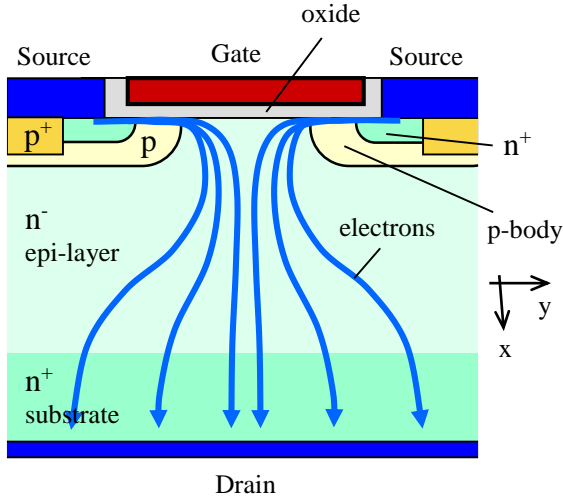


Fig. 1: Structure of the SiC Power MOSFET and electron flow

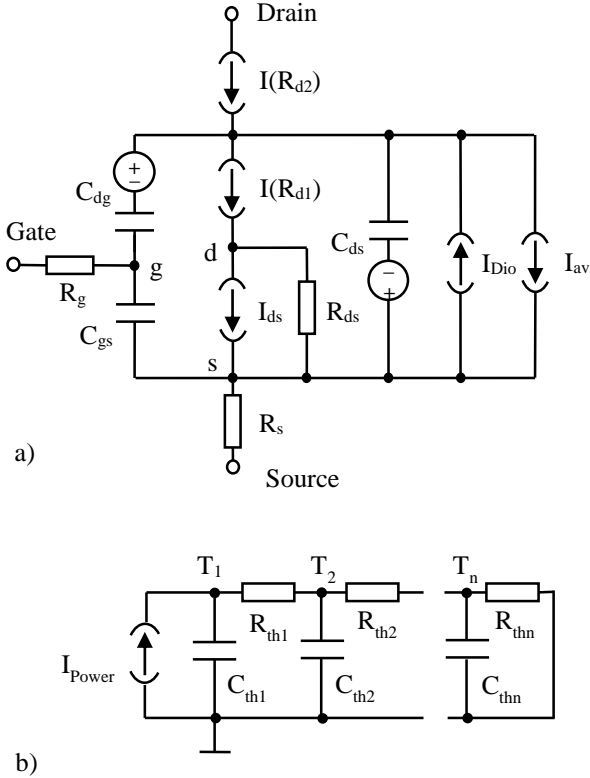


Fig. 2: Model of the SiC Power MOSFET, a) electrical subcircuit, b) thermal equivalent circuit.

current source  $I(R_{d2})$ . If the node voltages mentioned in the following text are labeled with indices with capital letters they are referred to the external contacts of the device; whereas node voltages having indices with lowercase letters refer to internal nodes of the model.

The model has been implemented in the circuit simulator PSpice, but the modeling concept is in principle transferable to other simulation software.

### A. DC-Current

SiC MOSFETs have a very large number of interface traps at the SiC-oxide interface. These traps degrade the device performance by reducing the electron density and electron mobility in the transistor channel [17]. Since the trap densities and their occupation with electrons are very temperature dependent they have also a significant influence on the temperature characteristic of the SiC MOSFET.

Taking the charge density of traps  $\sigma_{it}$  into account the electron charge density  $\sigma_n$  in the channel is given (in the case of constant electrostatic potential along the channel) by:

$$\sigma_n = c_{ox}(V_{gs} - V_{th}) - \sigma_{it} \quad (1)$$

$V_{th}$  is the threshold voltage of the transistor. The occupation of the interface traps increases with increasing gate voltage until all traps are filled and  $\sigma_{it}$  saturates. This is described with the equation:

$$\sigma_{it} = \frac{f_{it} c_{ox}(V_{gs} - V_{th})}{1 + \frac{\sigma_{itsat}}{\sigma_n}} \quad (2)$$

$f_{it}$  is a parameter with a value less than 1.  $\sigma_{itsat}$  causes a shift of the threshold voltage:

$$\Delta V_{th} = \frac{\sigma_{itsat}}{c_{ox}} \quad (3)$$

The electron charge density  $\sigma_n$  is then given by:

$$\begin{aligned} \sigma_n &= c_{ox}(V_{gs} - V_{th}) \left( 1 - \frac{f_{it}}{1 + f_{it}(V_{gs} - V_{th})/\Delta V_{th}} \right) \\ &= c_{ox} V_{geff} \end{aligned} \quad (4)$$

An effective gate voltage  $V_{geff}$  is introduced to describe this effect.  $V_{geff}$  is limited to positive values ( $V_{gs} \geq V_{th}$ ); an accurate description of the subthreshold behavior is not included in the model as it is of lesser importance. The leakage current of the MOSFET in its off-state is just taken into account with a temperature dependent resistor between drain and source.

For  $V_{ds} > 0$  the electron density decreases along the channel (in  $y$ -direction) due to the increasing electrostatic potential. The dependence of  $\sigma_n$  on the channel potential is calculated with a linear approximation and the influences of varying depletion charge and trap density are considered with a parameter  $k$ .

$$\sigma_n(y) = c_{ox}(V_{geff} - kV_{ch}(y)) \quad (5)$$

$V_{ch}(y)$  is the difference of the electrostatic potential between  $y$  and  $y = 0$  (source side of channel).

With this description of the electron charge and taking into account the influence of the lateral electric field on the electron mobility the following expression is obtained for the transistor current in the linear region:

$$I_{ds} = \frac{\beta}{1 + \frac{\beta V_{ds}}{g_{sat}}} \left( V_{geff} - \frac{k}{2} V_{ds} \right) V_{ds} \quad (6)$$

At high drain voltages the electrons near the end of the transistor channel reach their saturation velocity due to the high electric field. The electron current is then determined by the electron density near the channel end (given by eqn. (5)) and the saturation velocity  $v_{sat}$ .

$$I_{dsat} = w c_{ox} v_{sat} (V_{geff} - k V_{dsat}) = g_{sat} (V_{geff} - k V_{dsat}) \quad (7)$$

$V_{dsat}$  is the drain-source voltage value where current saturation begins. It is calculated by equating (6) and (7). The result is:

$$V_{dsat} = \frac{2V_{geff}}{k \left( 1 + \sqrt{1 + \frac{2\beta V_{geff}}{g_{sat} k}} \right)} \quad (8)$$

This leads to the current equation in saturation:

$$I_{dsat} = \frac{\beta V_{geff}^2}{k + \frac{\beta}{g_{sat}} V_{geff} + k \sqrt{1 + \frac{2\beta}{g_{sat} k} V_{geff}}} \quad (9)$$

To combine the descriptions of the linear and of the saturation region of operation into a single expression an effective drain-source voltage  $V_{deff}$  is used:

$$V_{deff} = 0.5 \left( V_{ds} + V_{dsat} + \delta - \sqrt{(V_{ds} - V_{dsat} + \delta)^2 + 4\delta V_{dsat}} \right) \quad (10)$$

$V_{deff}$  replaces  $V_{ds}$  in eqn. (6).  $\delta$  is a parameter which allows to adjust the smoothness of the transition between the two operation regimes.

The parameter  $\beta$  depends on the electron mobility  $\mu_n$ .

$$\beta = \frac{w}{l} c_{ox} \mu_n \quad (11)$$

The mobility in the transistor channel is strongly influenced by scattering due to the roughness of the SiC surface and by Coulomb scattering caused by the charge of the interface traps (besides the influence of the electric field which is already accounted for in the current equation).

The scattering due to surface roughness increases with increasing gate voltage due to the stronger attraction of the electrons to the SiC surface.

The Coulomb scattering due to the interface traps reduces the mobility mainly at low gate voltages. A large part of the

traps is already occupied below the threshold of the transistor. This is considered with the resulting value of  $V_{th}$ ; eqn. (2) describes just the increase of the trap occupation above the threshold voltage. Despite the further increase of the interface charge density above  $V_{th}$  the Coulomb scattering becomes weaker because of a screening of the interface charge by the charge of the electrons in the inversion layer.

As a consequence of these different effects the  $\beta$  of a SiC MOSFET can increase with the gate voltage at low voltage levels above  $V_{th}$  and just at high values of  $V_{gs}$  a decrease is observed like in Si MOSFETs. This behavior of  $\beta$  is described with the equation:

$$\beta = \frac{\beta_0}{1 + b(1 - V'_{geff}/V_\beta) + \theta V_{geff}} \quad (12)$$

$V'_{geff}$  is equal to  $V_{geff}$  if  $V_{geff}$  is below  $V_\beta$  and it is limited to  $V_\beta$  if  $V_{geff}$  exceeds this value.

When the MOSFET is in saturation the drain current is not really constant; it increases further with rising drain voltage. This is caused mainly by channel length modulation and this effect is taken into account with a simple linear approximation and a parameter  $\lambda$ . The resulting current equation is then:

$$I_{ds} = \frac{\beta}{1 + \frac{\beta}{g_{sat}} V_{deff}} \left( V_{geff} - \frac{k}{2} V_{deff} \right) V_{deff} (1 + \lambda(V_{ds} - V_{deff})) \quad (13)$$

This result is also used for the case of reverse bias of the transistor ( $V_{ds} < 0$ ); in this case just a minus sign is added to the right-hand side of (13),  $V_{gs}$  is replaced by  $V_{gd}$  in the expression for  $V_{geff}$  and the absolute value of  $V_{ds}$  is used in  $V_{deff}$ .

If  $V_{ds}$  is negative the body diode of the MOSFET structure is also turned on. Due to the large bandgap of SiC a significant diode current flows only if  $V_{ds}$  is below ca. -2.5 V.

## B. Drain Resistance

The higher critical electric field of SiC in comparison to silicon allows a much thinner blocking layer with higher doping concentration resulting in a much lower resistance. But the resistance of the drain region of SiC MOSFETs has still an important influence on the device characteristic. It causes a contribution to the on-state resistance which is not negligible. At low drain voltages the drain resistance is approximately constant and for this case it would be sufficient to include it in the model with just a resistor. However, at larger drain voltages the situation is different. The resistance of the drain region increases significantly as consequence of mainly two effects:

1. With increasing drain voltage the depletion regions at the junctions of the n-doped drain region and the p-bodies expand into the drain region and cause a narrowing of the path of the electron current. This is often called JFET effect. Furthermore also the drain

region directly below the gate oxide becomes depleted when the electrostatic potential in this region exceeds the gate voltage. This leads to a further strong constriction of the current path.

2. The high electric field at high drain voltage reduces the electron mobility.

The large drain resistance has the effect that at high drain voltages a large part of the voltage drops across the drain region and only a fraction of it remains across the transistor channel. This has mainly two consequences for the current characteristic:

1. When the voltage across the channel reaches the value  $V_{dsat}$  at which the saturation region of the MOSFET begins, the voltage  $V_{DS}$  which is externally applied at the contacts of drain and source is much higher than  $V_{dsat}$ . This effect increases with increasing current i.e. with increasing gate voltage. This means that the transition from linear to saturation region is shifted to significantly higher voltage levels of  $V_{DS}$ .
2. When the MOSFET is in saturation the current increase caused by channel length modulation is strongly attenuated since the voltage across the channel increases only slightly with rising  $V_{DS}$ .

This behavior of the SiC MOSFET at high voltage and current levels should also be reproduced by a compact model with sufficient accuracy. This is necessary to obtain correct simulation results of the switching waveforms and switching losses when the MOSFET is operated under hard switching conditions with inductive load. The model should also be able to predict the losses and the self-heating in the short-circuit case when very high drain voltages can occur.

The reduced effect of channel length modulation could be simply considered with an adjusted parameter  $\lambda$  in the equation of the electron current (eqn. (13)). But for an accurate modeling of the transition from linear to saturation region and to obtain correct results for the shift of the current saturation to high drain voltages it seems to be unavoidable to describe the voltage dependence of the drain resistance. However, it is rather difficult to consider the effects causing the variation of the resistance in a compact model.

For Si power MOSFETs already many attempts have been made to solve this problem [22]-[26]. But the resulting models are rather complicated, negatively impacting on computational efficiency and stability of the simulation, and they usually require the knowledge of details about the device structure and doping profiles. Only few models of the SiC power MOSFET consider the variable drain resistance so far. The model in [12] uses an empirical function to describe the variation of the drain resistance with drain and gate voltage and with temperature. The model presented in [13] depends on parameters which are related to the manufacturing process. In [14] a resistance model is developed which is based on the modeling approaches for silicon DMOS transistors. But this model is not incorporated into a compact model for circuit simulations. In [15] the drain resistance is modelled with a nonlinear voltage source and a resistance network; this model has only an implicit solution and the large number

of nodes of the resistive network has a negative impact on computation time.

This paper presents an approach which is based on substantial simplifications leading to a very simple solution which nevertheless provides results with reasonable accuracy.

The total resistance of the drain region is divided into two parts. The first part represents that region of the drain layer where the depletion regions cause a narrowing of the current path; the second part represents the rest of the drain where the full cross-section area remains available for the current.

$$R_{d1} = \frac{l_1}{qN\mu_{n1}A_1} \quad R_{d2} = \frac{L-l_1}{qN\mu_{n2}A} \quad (14)$$

$l_1$  is the thickness of the region with an averaged reduced area  $A_1$ ;  $L$  is the total thickness of the drain region (low doped epi-layer), and  $A$  is its total area.

$N$  is the doping concentration of the drain.

The decrease of the electron mobility at high electric fields is taken into account with the formula:

$$\mu_{n1} = \frac{\mu_0}{1 + \frac{\mu_0 V_{R1}}{v_{sat} l_1}} \quad (15)$$

$V_{R1}$  is the voltage drop across the first part of the drain region. An equivalent expression is used for the mobility in the second part of the drain.

The following equation of  $R_{d1}$  is then obtained:

$$R_{d1} = \left( \frac{L}{qN\mu_0 A} \frac{l_1}{L} + \frac{V_{R1}}{qNv_{sat} A} \right) \frac{A}{A_1} = \left( R_{d0} \frac{l_1}{L} + \frac{V_{R1}}{I_{sat}} \right) \frac{A}{A_1} \quad (16)$$

The result for  $R_{d2}$  is correspondingly:

$$R_{d2} = R_{d0} \left( 1 - \frac{l_1}{L} \right) + \frac{V_{R2}}{I_{sat}} \quad (17)$$

The thickness  $l_1$  depends on the expansion of the depletion region into the depth of the drain layer (in  $x$ -direction). Neglecting the (shallow) depth of the p-bodies  $l_1/L$  can be approximately calculated by:

$$\frac{l_1}{L} = F_l \sqrt{1 + \frac{V_{ds} + V_{R1}}{\phi_i}} \quad (18)$$

$\phi_i$  is the built-in voltage of the pn-junctions. The parameter  $F_l$  is determined by the condition that  $l_1$  approaches  $L$  when  $V_{ds} + V_{R1}$  reaches the breakdown voltage of the transistor. All the variations of the current flow are lumped into an effective, averaged area  $A_1$  and its voltage-dependence is kept very simple:

$$\frac{A}{A_1} = 1 + a_{r1} \sqrt{V_{ds}} + a_{r2} V_{dg} \quad (19)$$

The term with  $V_{ds}$  and the parameter  $a_{r1}$  describes the area reduction due to the depletion regions of the pn-junctions, and the term with  $V_{dg}$  and the parameter  $a_{r2}$  considers the additional effect of the depletion region under the gate oxide which is formed when the electrostatic potential in this region exceeds the gate voltage. Only the positive voltage range of  $V_{ds}$  and  $V_{dg}$  is used in (18) and (19); the variables  $V_{ds}$  and  $V_{dg}$  are set to zero if the voltages have negative values.

Since  $\Phi_i$  is a parameter used for the voltage-dependent drain-source capacitance and  $F_l$  is determined by the breakdown voltage, four parameters are used for the modeling of the drain resistance.

The value of  $R_{d0}$  is important for the on-state voltage of the MOSFET,  $a_{r1}$  has a strong influence on the transition from linear to saturation region,  $a_{r2}$  influences slightly the saturation characteristic at high drain voltages,  $I_{sat}$  gives an upper limit of the current which can flow through the drain layer.

With an additional constant factor in  $R_{d2}$  further resistance components resulting from substrate layer, contact and package can also be included.

### C. Further Model Components

The voltage-dependent capacitances of the SiC-MOSFET are modeled with a capacitor of fixed value in series with a controlled voltage source (Fig. 2). The voltage source provides such a voltage across the capacitor that the product of voltage and capacitance results in the required value of the charge [27].

The temperature dependence of the SiC-MOSFET is considered by describing the variation of the model parameters with temperature. Self-heating can also be simulated with the help of a thermal network which consists of a current source and one or several pairs of thermal capacitances and thermal resistances (Fig. 2b). The current  $I_{Power}$  of the current source corresponds with the total power dissipated in the device which is calculated as the sum of the current and voltage products of all current sources and resistors of the MOSFET model. The voltages at the thermal capacitances are equivalent to a temperature rise which is added to the ambient temperature.

A further effect included in the model is the breakdown behavior ( $I_{av}$  in Fig. 2).

## III. RESULTS

### A. Comparison of Model and Device Simulations

Simulations with the device simulator SENTAURUS [19] have been used to support the model development and to validate the model results. The analyzed structure is shown in Fig. 1. The dimensions and doping concentrations have been chosen in such a way that the characteristics of a 1.2 kV SiC MOSFET, manufactured by Cree Inc. (CMF2010D [28]), could be reproduced. The density of interface traps at

the semiconductor-oxide boundary has been selected according to the analysis presented in the paper [17] and to adjust the  $I_{DS}(V_{GS})$ -curve to the experimental result.

The influence of the interface traps on the electron charge in the transistor channel can be seen in Fig. 3. It shows how the electron charge density  $\sigma_n$  increases with the gate voltage in the cases with and without interface traps. Without traps a linear increase of the electron density with rising  $V_{GS}$  results (except for a very small voltage range at threshold). Interface traps reduce the electron density and a linear dependence on the gate voltage is obtained only for larger values of  $V_{GS}$  when all traps are occupied.

Fig. 3 also shows how this behavior is described with the model equation for  $\sigma_n$  (4).

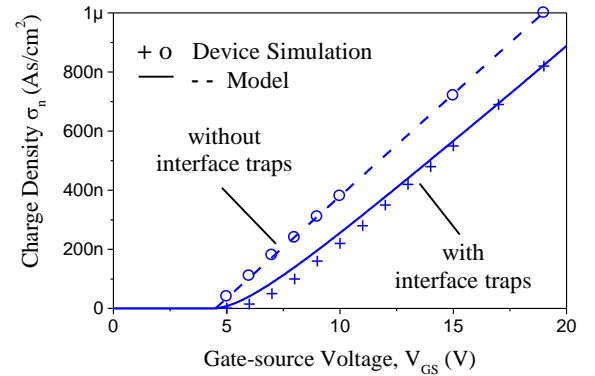


Fig. 3: Electron charge density in transistor channel.

The effect of the drain resistance on the internal drain-source voltage is demonstrated in Fig. 4. The internal drain-source voltage is obtained by subtracting the voltage drop occurring along the current path in the drain region from the voltage which is externally applied at the drain and source contacts. This internal voltage corresponds with the voltage  $V_{ds}$  which is used in the model equations.

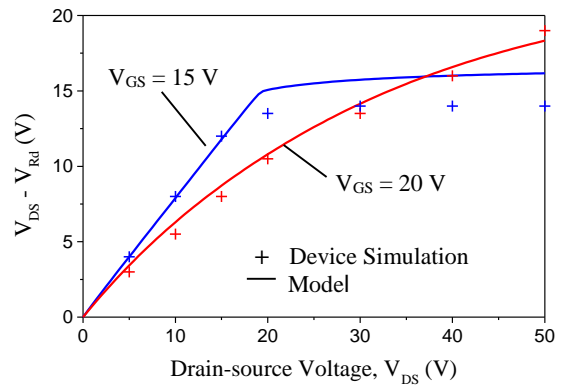


Fig. 4: Internal drain-source voltage  $V_{ds} = V_{DS} - V_{Rd}$ .

With rising drain voltage the drain resistance increases significantly due to the constricted current path and causes a large voltage drop in the drain. This retards the increase of the voltage across the transistor channel especially at high gate voltage which has the consequence that the current saturation of the transistor is reached only at rather high values of the drain voltage.

When the drain region below the gate oxide begins to be depleted the electrostatic potential remains nearly constant at a point close to the pn-junctions where the electrons are injected from the transistor channel into the drain. Therefore the internal drain-source voltage becomes limited to a value which is approximately equal to the gate-source voltage.

The comparisons of the results produced by the model and extracted from device simulations show that the simple model of the drain resistance can describe the basic effects with the sufficient accuracy necessary to obtain the current-voltage characteristics correctly.

### B. Comparison with Measurements

The model has been compared with measurements of a few different SiC Power MOSFETs which are available from device manufacturers so far. As example the results obtained with the newest SiC-MOSFET from Cree Inc. are presented. It is a 1.2 kV, 30 A transistor (C2M0080120D [28]).

Fig. 5 shows the transfer characteristics of the measured device and the model at different temperatures.

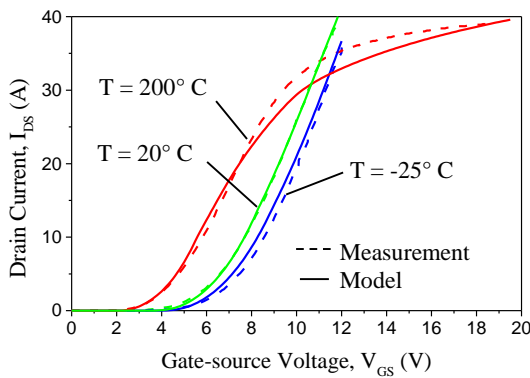


Fig. 5: Transfer characteristics at different temperatures,  $V_{DS} = 10$  V.

Fig. 6 to Fig. 8 demonstrate the output characteristics at room temperature,  $-25^\circ\text{C}$ , and  $200^\circ\text{C}$ , respectively.

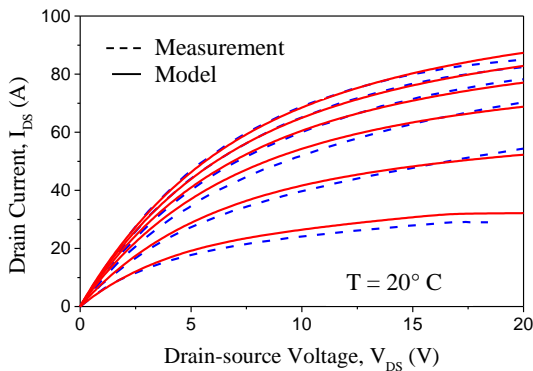


Fig. 6: Output characteristics at room temperature. The gate-source voltage varies from 10 V to 20 V with increments of 2 V.

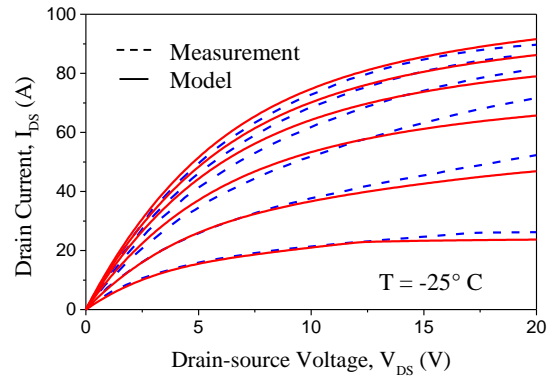


Fig. 7: Output characteristics at  $-25^\circ\text{C}$ . The gate-source voltage varies from 10 V to 20 V with increments of 2 V.

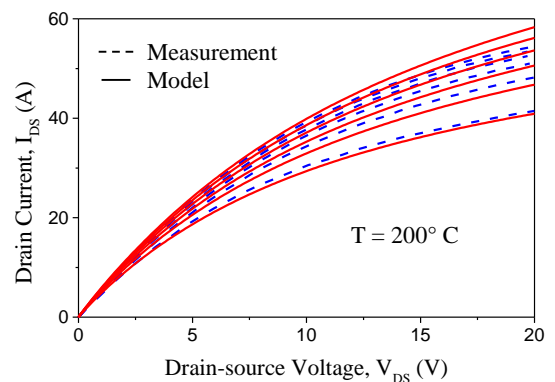


Fig. 8: Output characteristics at  $200^\circ\text{C}$ . The gate-source voltage varies from 10 V to 20 V with increments of 2 V.

At high temperatures the large resistance of the drain region causes a significant limitation of the current. At low temperature the reduced electron mobility in the transistor channel is the main reason for the current limits.

The variation of the drain-source on-state resistance  $R_{on}$  with temperature is shown in Fig. 9.

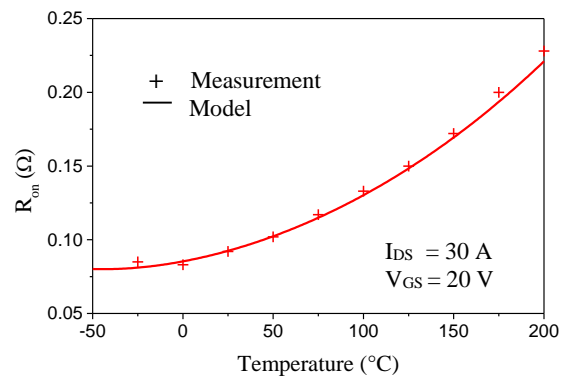


Fig. 9: Variation of the on-state resistance with temperature.

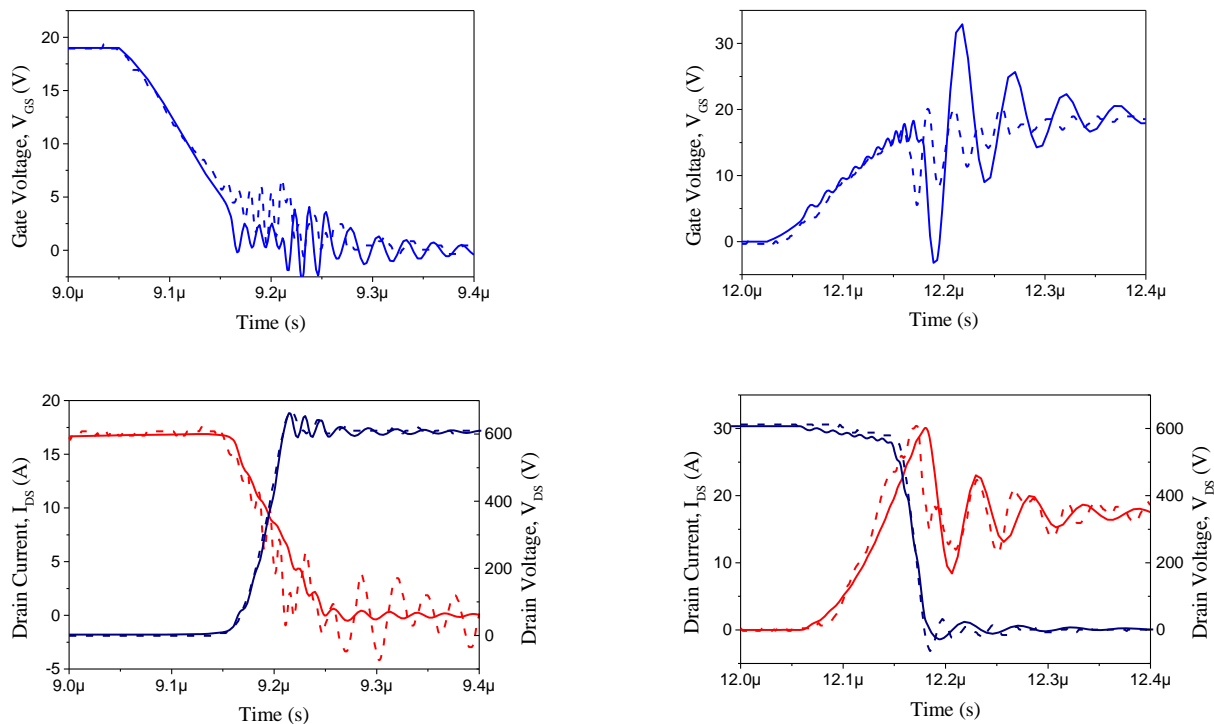


Fig. 10: Turn-off and turn-on behavior of the SiC-MOSFET with inductive load and freewheeling diode at  $T = 150^{\circ}\text{C}$ , - - - measurement, — simulation.

The switching behavior has been investigated with a test circuit consisting of the SiC-MOSFET, an inductive load of  $320\ \mu\text{H}$  and a SiC Schottky diode used as freewheeling diode. In the simulated circuit the parasitic inductances of the device packages and the connections between the circuit components as well as the parasitic capacitance of the inductive load are considered. The gate drive is simplified with just a pulsed voltage source and a gate resistor. For the Schottky diode a model provided by CREE is used.

Fig. 10 shows the waveforms of gate-source voltage, drain-source voltage and drain current which are obtained by measurements and by simulations at turn-off and turn-on of the SiC-MOSFET.

The agreement between simulation and measurements is quite good for the main switching characteristics like the voltage and current slopes. Major differences are just observed for some oscillations. For the turn-off transient the current ringings are much larger in the experiment than in the simulation; for the turn-on transient the ringings of the gate voltage are larger in the simulation than in the measurement. But it is actually rather difficult to reproduce all oscillations correctly since the parasitic elements of the circuit are considered just in a very simplified way and also the influence of the measurement tools is neglected.

#### IV. CONCLUSION

A compact model of SiC Power MOSFETs has been developed which reproduces the device behavior with good

accuracy for the whole range of operating biases and temperatures. This has been achieved by taking into account the physical phenomena which are responsible for the special characteristics of SiC MOSFETs. Interface traps at the SiC-oxide interface reduce the electron density and electron mobility in the transistor channel, and they cause a variation of the mobility with gate voltage and temperature which is (at low  $V_{gs}$ ) contrary to that in Silicon MOSFETs. The resistance of the drain region increases strongly with the drain voltage and the resulting voltage drop at high current levels is decisive for the current-voltage characteristics.

To keep the calculation as simple as possible and to obtain a better fit empirical functions and parameters are partly used, but they are closely related to the physical phenomena which are the origin of the device behavior.

Due to the inclusion of the relevant effects and the accuracy over a very broad voltage and temperature range the model is well suited to investigate the behavior of SiC MOSFETs with the help of circuit simulations in many diverse applications. The advantages of SiC MOSFETs as well as possible problems can be explored and the capability to simulate fast transient self-heating effects can also support the analysis of performance and robustness.

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