A Comprehensive Study of Short-Circuit Ruggedness of Silicon Carbide Power MOSFETs

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***Abstract*— The behavior of silicon carbide (SiC) power MOSFETs under stressful short-circuit (SC) conditions is investigated in this paper. Two different SC failure phenomena for SiC power MOSFETs are thoroughly reported. Experimental evidence and TCAD electrothermal simulations are exploited to describe and discriminate the failure sources. Physical causes are finally investigated and explained by means of properly calibrated numerical investigations and are reported along with their effects on devices' SC capability.**

***Index Terms*— Short-circuit (SC) failure mechanism, SC ruggedness, silicon carbide (SiC) power MOSFETs, thermal runaway.**

I. Introduction

SILICON carbide (SiC) power MOSFETs have experienced rapid technological developments, making them a commercial reality in the field of power semiconductor devices. Such devices are gradually replacing silicon device counterparts in different power electronic systems. Their application range includes energy conversion and distribution, avionics and automotive, renewable energy, and electric traction. The major upsides come from several material features generally considered superior to those of silicon [1], [2]. Higher critical electric field, lower leakage current, and higher thermal conductivity, to name a few, reflect a lower ON resistance, a higher switching frequency, and a better temperature capability for SiC devices. Even though over the years there has been a fast progress in device technology [3], which allowed for the production of commercial devices with better performances (switching frequency, power efficiency, long term reliability, etc.), there is still margin for quality and cost improvement. The cost of single device is not yet competitive but benefits can become dominant at application level where compact and highly efficient systems could be realized [4], [5].

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In recent years, many works [6]–[10] have carried out investigation and characterization of reliability of SiC devices; nevertheless, many issues still have to be fully addressed.

Through in-depth investigations it will be possible to suggest design rules and engineering improvements that will push up devices' performance boundaries.

In order to define their limit to withstand the most demanding working operations, devices are usually analyzed during highly stressful conditions, that is, most commonly during unclamped inductive switching and short circuit (SC), two routine techniques regularly used for characterizing silicon power devices (see [11], [12]).

An SC event can occur in a variety of ways in an industrial environment. This is especially true for motor driving systems, where different kinds of protection circuits were proposed to avoid catastrophic failure during overload and SC events at the inverter stage (see [13]–[16]). Therefore, in this scenario, a device should be designed to have reasonable SC withstand time prior to the intervention of the protection circuitry. Nevertheless, this could not be achieved without an understanding of the underlying physical mechanisms that bring the device to failure.

In the recent past, different papers addressed the SC robustness of SiC power MOSFETs. In [17]–[19], an experimental evaluation of robustness and performances of commercially available devices was given. The reported results showed the weakness of the gate during SC tests and at different failure modes. Experiments on SiC power MOSFET and JFET were carried out in [20] under SC fault condition. The device temperature was also estimated to be very high, leading to melting of aluminum and finally to device failure. Wide experimental data on different commercial devices and numerical investigations through electrically and thermally coupled models were exploited to analyze the temperature dependence of SC withstanding capability in [21]. In [22], electrothermal simulations are shown to analyze the SC SOA using compact models. Reference [23] presents numerical and experimental analyses of a failure mode during pulsed overcurrent. However, these results did not examine the possible failure mode in SC, which must be analyzed through testing and modeling. In this context, the aim of this paper is to present an interpretation of the inner physical dynamics limiting the SC capability of SiC MOSFETs. A broad set of experimental measurements is performed to evaluate

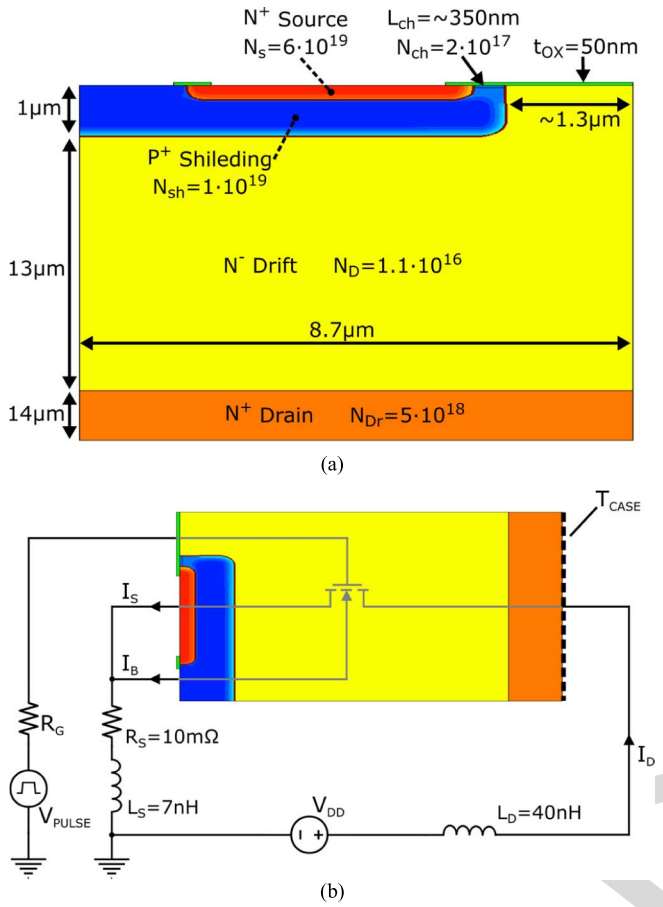


Fig. 1. (a) Simulated structure (not in scale). (b) Mixed-mode schematic.

different SC failure modes of commercially available SiC MOSFETs.

After an introduction, in Section II, both the experimental and simulation methods used to carry out the analysis are illustrated, giving information on the test setup and the TCAD structure. Section III reports in detail the main results gained, and their analysis leads to determining two separate failure modes. In Section IV, the physical phenomena limiting the SC reliability of devices are discussed, recognizing that temperature is the main impacting factor.

II. Analysis Approaches

Experimental data were collected through extensive testing of commercially available devices that were characterized during the failure event under different operating conditions. The outcomes were subsequently investigated, and with the aid of numerical electrothermal simulations, the physical mechanisms involved in the failure event have been properly inspected, giving an insight into different phenomena occurring inside the device.

A. Simulated Structure

Thanks to device symmetry, a half elementary cell of a planar MOSFET [Fig. 1(a)] was reproduced for this study and analyzed with the TCAD Synopsys Suite.

Even though the structure was calibrated to match the behavior of a commercial device, it does not represent the actual device structure. Hence, it could be taken as a more general case study. Theoretical assumptions and literature data (see [24]) were used to define doping and dimensions [reported in Fig. 1(a)]. Principal models and corresponding parameters are listed in the Appendix. For simulation purpose, body and source terminals were physically separated but connected at the same electrical node.

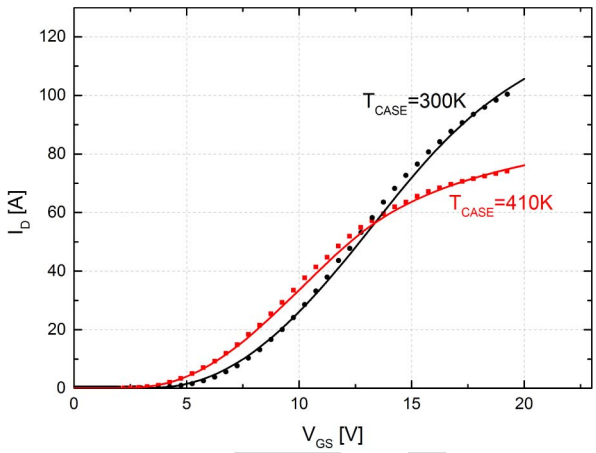


Fig. 2. Measured (symbols) and simulated (solid) isothermal I_D–V_{GS} characteristics ($V_{DS} = 20$ V).

Mixed-mode simulations were performed, in which a physically based device was placed alongside a circuit description (in a SPICE netlist format) as depicted in Fig. 1(b). Additional components were included to consider the parasitic elements introduced in a real circuit by wires and connections. Specifically, stray inductance and parasitic resistance on the source loop (L_S, R_S) affect the di/dt during the turn-ON phase; stray inductance on the drain (L_D) is responsible for voltage spikes during switching transients. Fig. 1(b) shows their estimated values.

It is well known that temperature strongly affects the behavior of power devices, and therefore self-heating effects could not be neglected. Accordingly, temperature-dependent parameters were included, and heat generation and transport equations were solved in conjunction with semiconductor equations. The thermal problem was solved applying the isothermal condition on the back of the device (T_{CASE}) and adiabatic conditions on the remaining edges.

In order to reflect the operation of an actual device, the structure was calibrated obtaining a suitable match with isothermal I_D–V_{GS} characteristics of a 1.2-kV 36-A 80-mΩ commercial device [25], selected as case study. The curves were measured at $V_{DS} = 20$ V by means of a pulsed curve tracer and are illustrated in Fig. 2 for backside temperatures of 300 and 410 K.

The calibration procedure implied the choice of suitable physical models (e.g., mobility doping dependence, carrier recombination, etc.) and the proper tuning of their parameters. Device behavior is largely dependent on the quality of the oxide–semiconductor interface and could not be correctly reproduced without including fixed charges and trap levels usually present therein. References [26] and [27] have reported the impact of interface defects and dislocations on

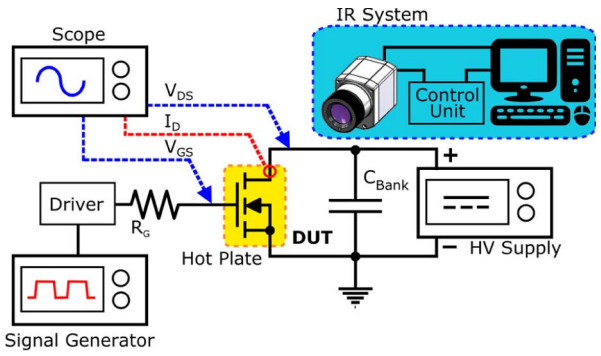


Fig. 3. Test setup diagram.

MOSFET devices. These trap levels are commonly considered to be acceptor-like above mid-gap energy E_i, i.e., negatively charged when occupied. One of the effects is a positive shift of the threshold voltage, which can then be analytically expressed as [28]

$$V_{TH} = V_{FB} + 2\phi_B + \frac{1}{C_{OX}}\left(\sqrt{2\varepsilon_s q N_A(2\phi_B)} + q\int_{E_i}^{E_i+q\phi_B} D_{it}(E)dE\right) \quad (1)$$

where D_{it} is the interface trap density, and other symbols have the common meaning. Furthermore, the filled traps give rise to Coulomb scattering that turns into a mobility decrease of channel electrons flowing close to the surface.

The number of filled traps decreases as the temperature increases since trapped electrons tend to be emitted. This leads to a lowering of the threshold voltage. In addition, both a reduction in Coulomb scattering and a higher number of free carriers improve the channel mobility. Therefore, there is a temperature range in which mobility actually increases with temperature, until all electrons are released.

B. Experimental Setup

SC tests were performed on the aforementioned device for different operating conditions (i.e., V_{DS}, T_{CASE}, V_{GS}, t_{PULSE}). In addition, in order to give a widespread validation of the obtained results, other manufactures' devices that were 1.2-kV 80-mΩ rated were tested [29], [30].

A schematic of the experimental system is shown in Fig. 3. The gate driving system consists of a MCP1404 driver IC manufactured by Microchip and a 5-Ω gate resistor. The gate voltage goes from 0 to 20 V. Voltage is applied by a HVdc power supply, and it is held during the SC pulse by a 1-mF capacitor bank. The DUT is placed on a hot plate through which it is possible to set the case temperature. A custom advanced infrared (IR) thermography system, fully described in [31], was used to acquire the surface temperature of the device during the SC test. Featuring an equivalent time sampling technique, it is able to acquire fast transient dynamics, with 1 MHz equivalent frame rate. Thus, it is possible to track the temperature evolution, and therefore the current distribution, during the applied SC pulse. In addition, the system allows a single-shot capture of the temperature map at any desired time instant along the test. This feature

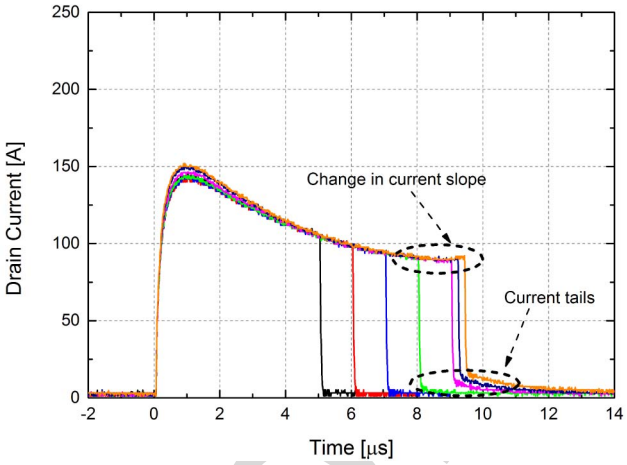


Fig. 4. I_D short-circuit waveforms (V_{DS} = 600 V; V_{GS} = 16 V; T_{CASE} = 75 °C; CREE).

was used, as will be shown later, to catch the heat spreading at its maximum, i.e., at the pulse turn-OFF edge. If the device fails, this corresponds to spotting the current distribution right before the failure event, which could lead to useful information about the failure mechanism itself. IR camera integration time was set to 1 μs and a two-point calibration procedure was performed to compensate the emissivity contrast effect [32]. Furthermore, due to high temperature reached during the experiment exceeding the camera calibration range, thermal images were elaborated in postprocessing to represent the normalized temperature increase

$$T_n = \frac{T - T_0}{T_{max} - T_0} \quad (2)$$

where T_0 is the case temperature and T_{max} is the maximum temperature for each thermal map.

III. Experimental and Simulation Results

This paragraph describes the main results obtained through experiments and simulations. Tests were carried out using two distinct approaches:

1) short pulses (≤20 μs) at high voltage (≥400 V);
2) long pulses (100 μs) at low voltage (≤200 V).

Based on the results it was possible to infer two different failure mechanisms during SC, both related to temperature increase inside the structure, as will be discussed later.

A. High-Voltage Short-Pulse Tests

In the following, the most relevant results are summarized. From single-pulse SCt waveforms (Figs. 4 and 5), the appearance of two phenomena becomes immediately evident; specifically, the current tends to change slope at the end of the pulse and current tails, usually present in bipolar devices, which originate after the turn OFF.

These effects were already reported in [33], and they are present in different devices as well, upheld by test results (Figs. 6 and 7).

Generally, it is an uncommon behavior for a power MOSFET, since as a unipolar device, it should not have any

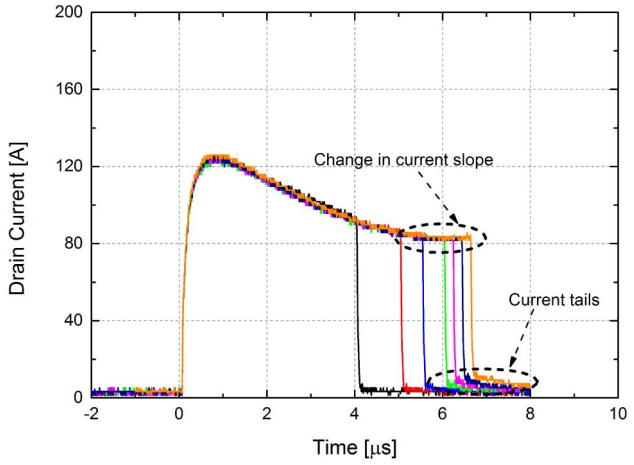


Fig. 5. I_D short-circuit waveforms (V_{DS} = 800 V; V_{GS} = 18 V; T_{CASE} = 150 °C; CREE).

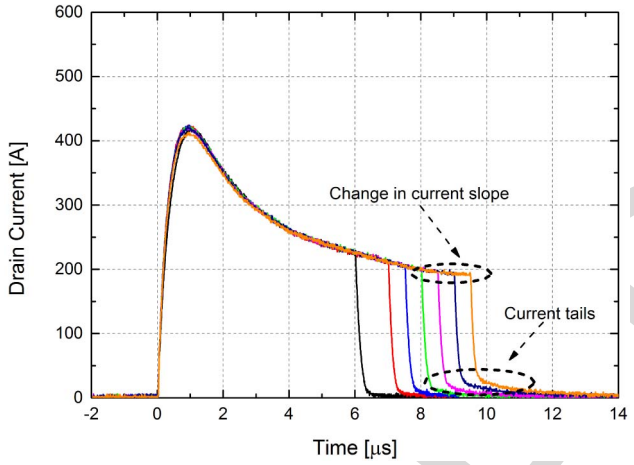


Fig. 6. I_D short-circuit waveforms (V_{DS} = 400 V; V_{GS} = 20 V; T_{CASE} = 27 °C; ST).

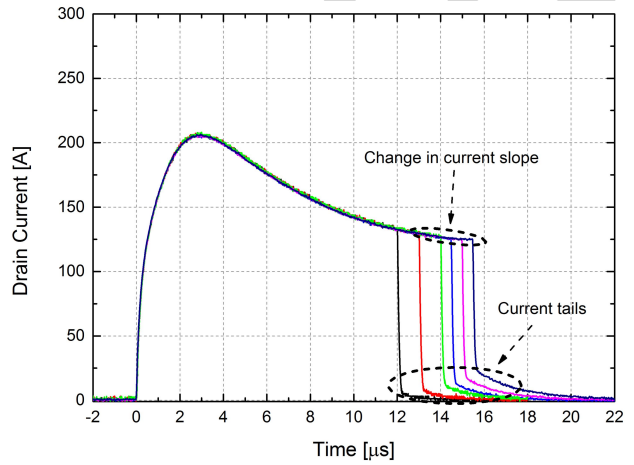


Fig. 7. I_D short-circuit waveforms (V_{DS} = 600 V; V_{GS} = 18 V; T_{CASE} = 27 °C; ROHM).

current tails, and it should have a negative current slope when biased above the temperature compensation point.

These two effects could be considered temperature related, since as the pulse length increases and/or applied voltage and

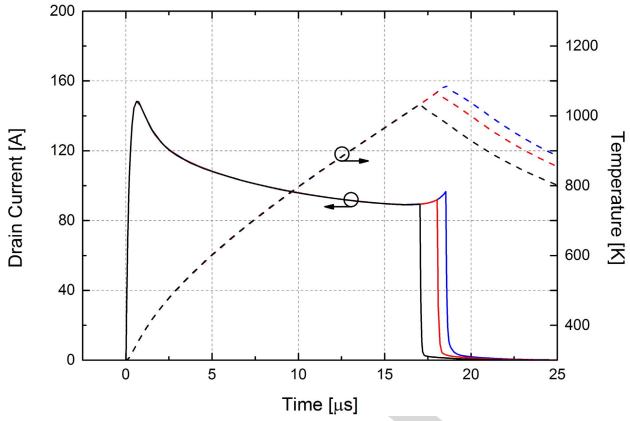


Fig. 8. Simulated drain current and surface temperature (V_{DS} = 400 V; V_{GS} = 18 V; T_{CASE} = 27 °C).

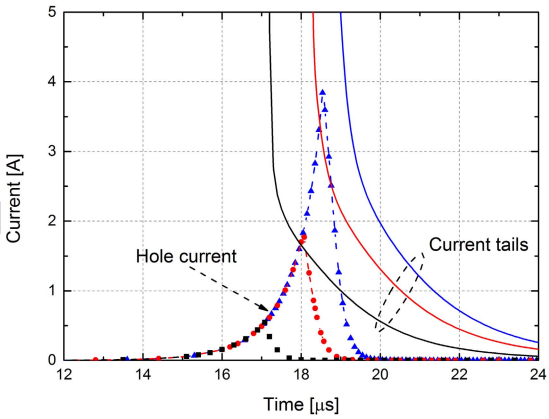


Fig. 9. Details of current tails (solid line) and hole current (dashed line) from the simulation of Fig. 8 (V_{DS} = 400 V; V_{GS} = 18 V; T_{CASE} = 27 °C).

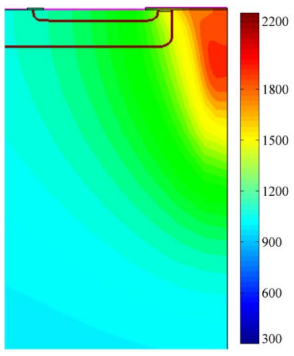


Fig. 10. Temperature distribution at t = 18.5 μs (V_{DS} = 400 V; V_{GS} = 18 V; T_{CASE} = 27 °C, scale in K).

back temperature are higher, they become more and more relevant up to device catastrophic failure.

Deeper investigations were carried through physical electrothermal simulations.

In Fig. 8, simulated drain current waveforms are depicted along with the average surface temperature; the same behavior observed experimentally has also been reproduced. The first interesting result can be pointed out (Fig. 9): the formation of hole current flowing out of the body terminal. It becomes visible when the current starts to change its slope.

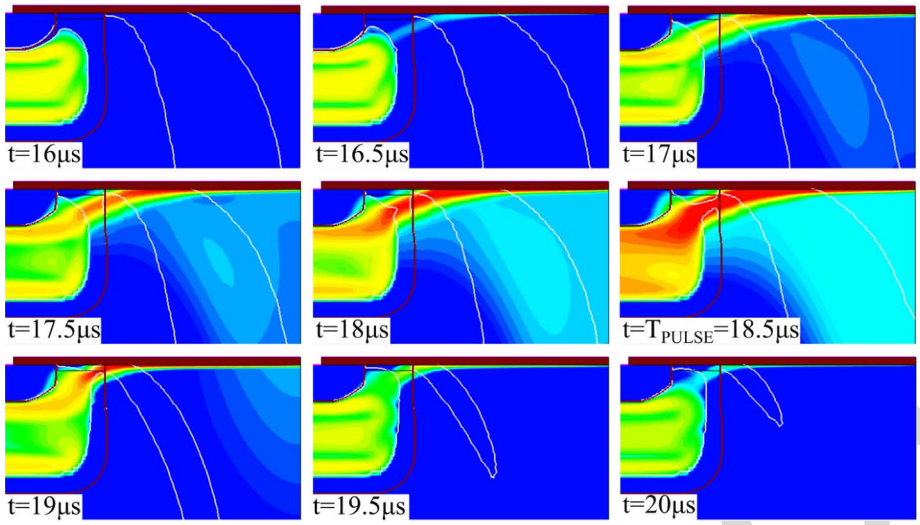


Fig. 11. Simulated hole current density ($V_{DS} = 400$ V; $V_{GS} = 18$ V; $T_{CASE} = 27$ °C).

The second aspect that can be spotted is that the heat is mainly generated in the JFET region and an extreme high-temperature peak value is reached therein (Fig. 10). Fig. 11 depicts the hole current density at different time instants along a 18.5-μs SC pulse. In the beginning, the hole concentration has a very low value, and therefore the leakage current of the body/drift p-n junction is negligible. As the temperature increases, it leads to an increase in the number of holes, and consequently leakage current keeps increasing gradually. This phenomenon gives rise to the hole current coming out the body terminal. Using formulas and values reported in [24], [34], and [35], it is possible to carry out an approximate estimation of the leakage current as a function of temperature

$$j_s = q n_i^2 \left(\frac{D_p}{L_p N_D} \right) \tag{3}$$

where D_p and L_p (1–2 μm, [24]) are the diffusivity and the diffusion length, respectively, and n_i is given by

$$n_i = 1.7 \cdot 10^{16} T^{3/2} e^{-2.08 \cdot 10^4 / T} \tag{4}$$

D_p can be calculated from mobility μ_p

$$\mu_p = 125 \left(\frac{T}{300} \right)^{-2.7}. \tag{5}$$

Combining (3)–(5) with the assumption of a device approximately 3 mm × 3 mm and SiC physical parameters from [36], the leakage current can roughly be estimated to be ∼30 A at $T = 2000$ K. Far from being an accurate calculation, this result indicates the temperature range in which the leakage current is expected to have a value comparable to the ON-state current value during SC, that is, when the device is experiencing thermal runaway. On the other hand, to get a current tail similar to the one experimentally observed, the temperature peak value should not be much far from the one obtained in simulation. Thus, holes are thermally generated due to locally elevated temperature increase. The electric field in the drift region drags the generated carriers toward the top of the device. Hole density keeps increasing until a certain point along the body/drift edge when the p-n junction does not exist anymore. This is due to excessive carrier concentration that punches through the junction.

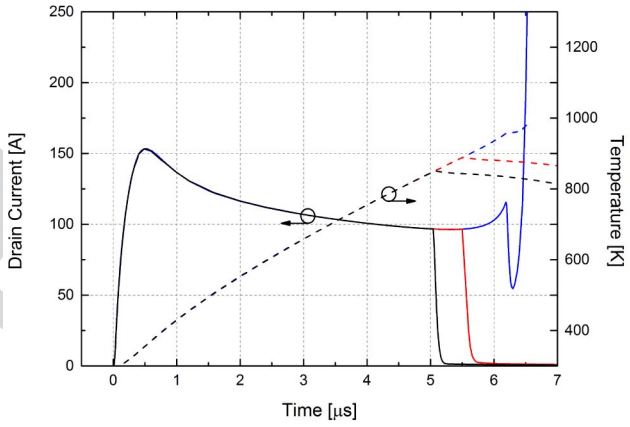


Fig. 12. Simulated drain current and surface temperature ($V_{DS} = 800$ V; $V_{GS} = 18$ V; $T_{CASE} = 27$ °C). AQ:5

Obviously, electrons are thermally generated at the same time and are free to flow from source to drain even when the applied gate voltage is zero. The current tail is indeed built up by the merging of the aforementioned leakage currents. The tail then slowly decreases to zero within a time linked to the one needed to remove all the generated carriers. Nevertheless, the leakage current could reach a level at which thermal runaway takes place leading to device failure. This is a positive feedback phenomenon inducing an uncontrollable increase in the drain current up to MOSFET destruction (Fig. 13). It is furthermore inferred that these devices do not comply with the usual required SC capability of silicon power devices, which is at the minimum withstanding a SC pulse of 10 μs with two-third rated voltage applied. AQ:6

To better comprehend the inner device dynamics preceding the failure event (i.e., during the current tail), temperature distribution was acquired at the turn OFF of a 8-μs SC pulse. To easily accomplish this task, the temperature evolution was

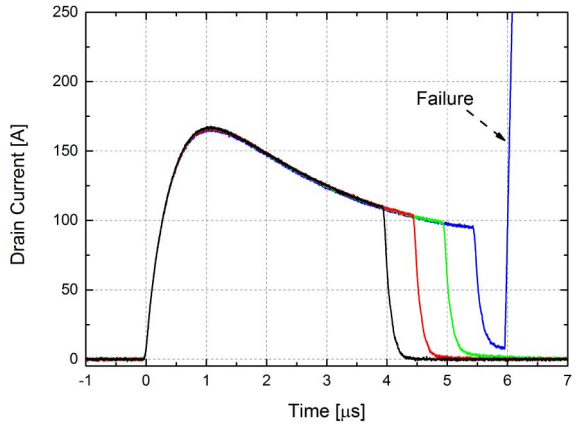


Fig. 13. I_D short-circuit waveforms (V_{DS} = 800 V; V_{GS} = 18 V; T_{CASE} = 27 °C; CREE).

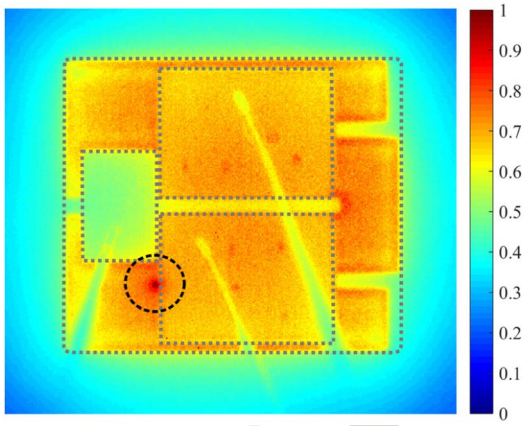


Fig. 15. Normalized temperature increase at t = 8 μs for the experiment of Fig. 14.

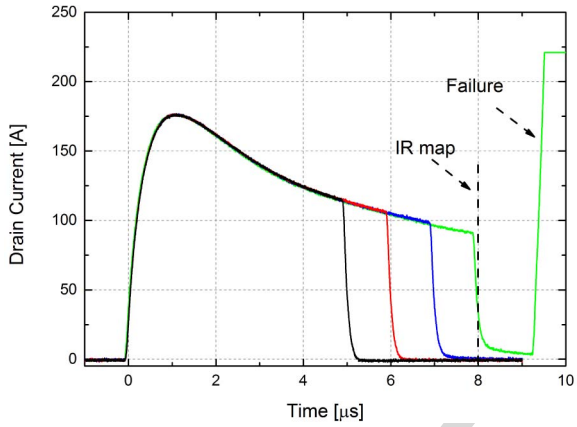


Fig. 14. I_D short-circuit waveforms (V_{DS} = 600 V; V_{GS} = 18 V; T_{CASE} = 27 °C; CREE).

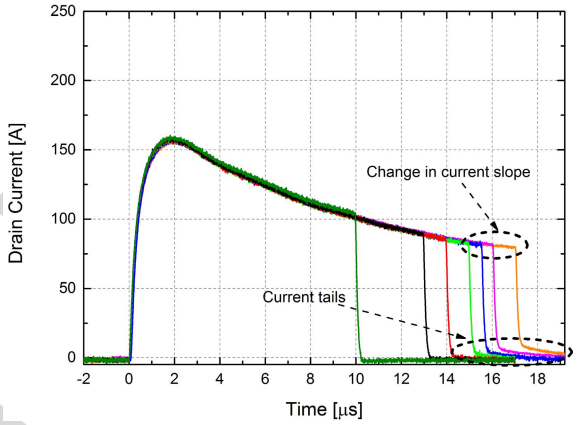


Fig. 16. I_D short-circuit waveforms (V_{DS} = 400 V; V_{GS} = 18 V; T_{CASE} = 27 °C; CREE).

slowed down choosing V_{DS} = 600 V. The thermal map of Fig. 15 corresponds to the current distribution at turn OFF, that is, just before the failure event (as indicated in the figure). It clearly reveals that the failure arises from high power density being confined to an extremely small area (encircled red dots in the figure) corresponding to the formation of a hot spot.

When there is local growth of leakage carriers, a cluster of adjacent cells might tend to drain more current triggering the thermal runaway event. The current crowds in a limited portion of the total area, activating a self-sustained process that promptly entails the creation of the hot spot. The increase in the current at the end of the SC pulse (before thermal runaway takes place) is much more pronounced in simulation than in experimental waveforms. It is a consequence of the used simulation approach, in which just a single cell is investigated. Thus, the electrothermal interaction with surrounding cells, leading to a stronger positive feedback, is not taken into account.

Nonetheless, the mechanism explained above is not the only source of failure that was observed.

At some different applied conditions, for which the power applied is lower (e.g., the one in Fig. 16), current tails still appear but the device experiences a different phenomenon. For this test, SC pulses of gradually increasing width were applied to the DUT and thermal maps were acquired at the end of each experiment. After a certain pulse length (17 μs in this case), the device does not turn ON anymore. Inspection of temperature distribution at the end of different pulses (Fig. 17) illustrates areas on the device surface that are activated partially. Focusing on the encircled area of Fig. 17(b) and the same device portion in Fig. 17(a), a transition from an almost uniform current to a less homogeneous one is visible. Since for a MOSFET without any unstable behavior the current should expand in all active areas, it could be assumed that those areas were somehow degraded. They are thus prone to carry less current, eventually being inoperative. Moreover, a residual resistance of tens of ohms was measured between the gate and the source.

B. Low-Voltage Long-Pulse Tests

In order to try to get a better understanding of the origin of the aforementioned observed failure, different tests were performed. Devices were subjected to SC for long pulse widths (100 μs) but with a low applied voltage (<250 V). In this way, it is possible to slow down the temperature dynamics, and hence to analyze the device response to long thermal stress. The pulse length is kept constant and the voltage

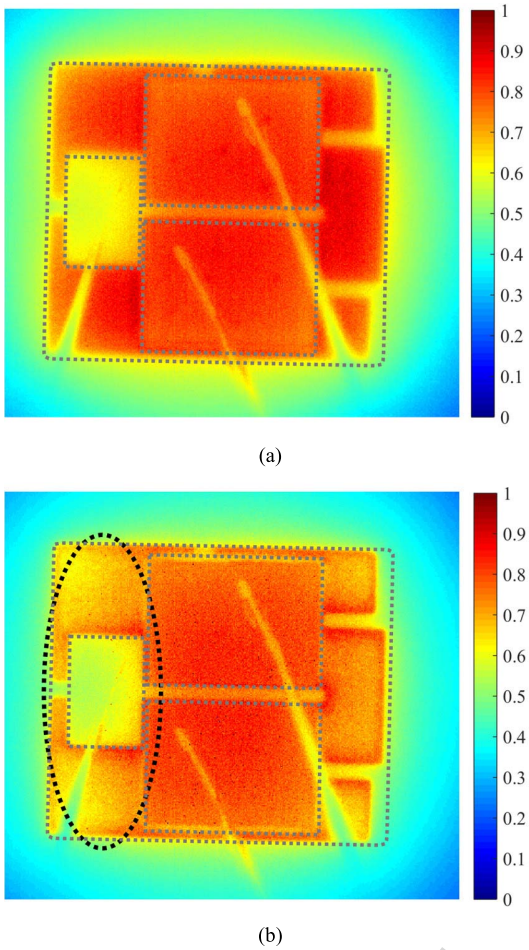


Fig. 17. Normalized temperature increase for the experiment of Fig. 16 at (a) $t = 10$ μs and (b) $t = 17$ μs.

is increased at each step. Resulting current waveforms at different V_{DS} are reported in Fig. 18, where the effect of temperature rise on the current profile is clearly visible. When a certain voltage value is reached (175 V in this case), the device is not able to withstand the entire pulse duration and fails after approximately 85 μs, corresponding to the time instant at which the drain current drops to zero. In addition, it is interesting to note that, at the same time, the gate–source voltage drops to zero as well, and the gate current suddenly increases (Fig. 18). It is then straightforward to assume that the device turned OFF because an SC had happened between the gate and the source, confirmed by the subsequent measure of R_{GS} (<1 Ω). It could be supposed that the metallization and/or passivation layers on the top of a MOSFET might be melted or somehow corrupted.

Hence, in this case, the device does not undergo catastrophic failure as previously explained, but it is not operative anymore because of damage to the gate/source structure.

IV. Discussion

After description in the previous section, here an explanation of different failure mechanisms during SC for a SiC power MOSFET is given. As made clear by the reported results, two separate phenomena might happen when a device fails.

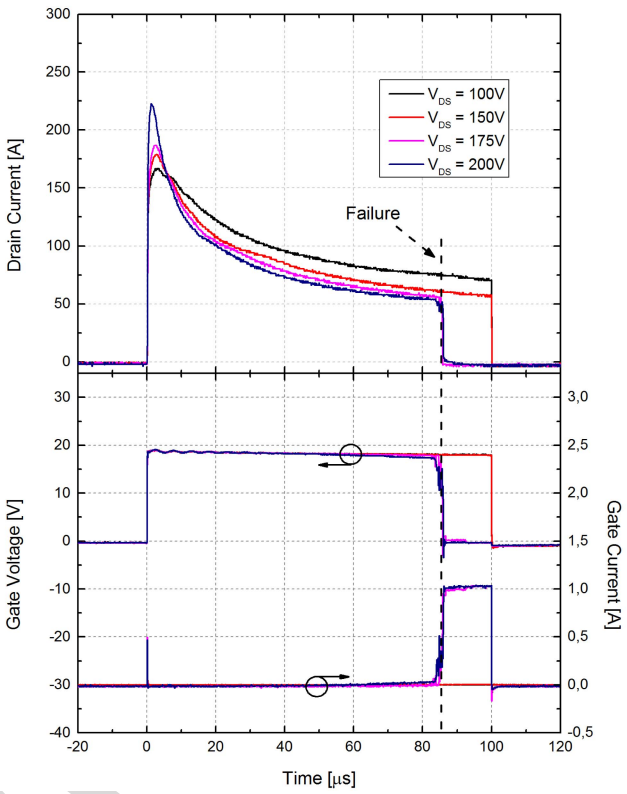


Fig. 18. I_D, V_{GS}, I_G waveforms for a 100-μs pulse test.

It is convenient to indicate them as *failure mode I* and *failure mode II*.

In the first type, the device experiences a destructive mechanism due to exponential rise in drain current subsequent to thermal runaway triggering. The second type failure, on the other hand, involves the degradation of the gate structure, with subsequent inability to turn the device ON, which is why it could be considered a soft failure.

Both are regulated by the temperature increase inside the device, and more precisely by its growth rate.

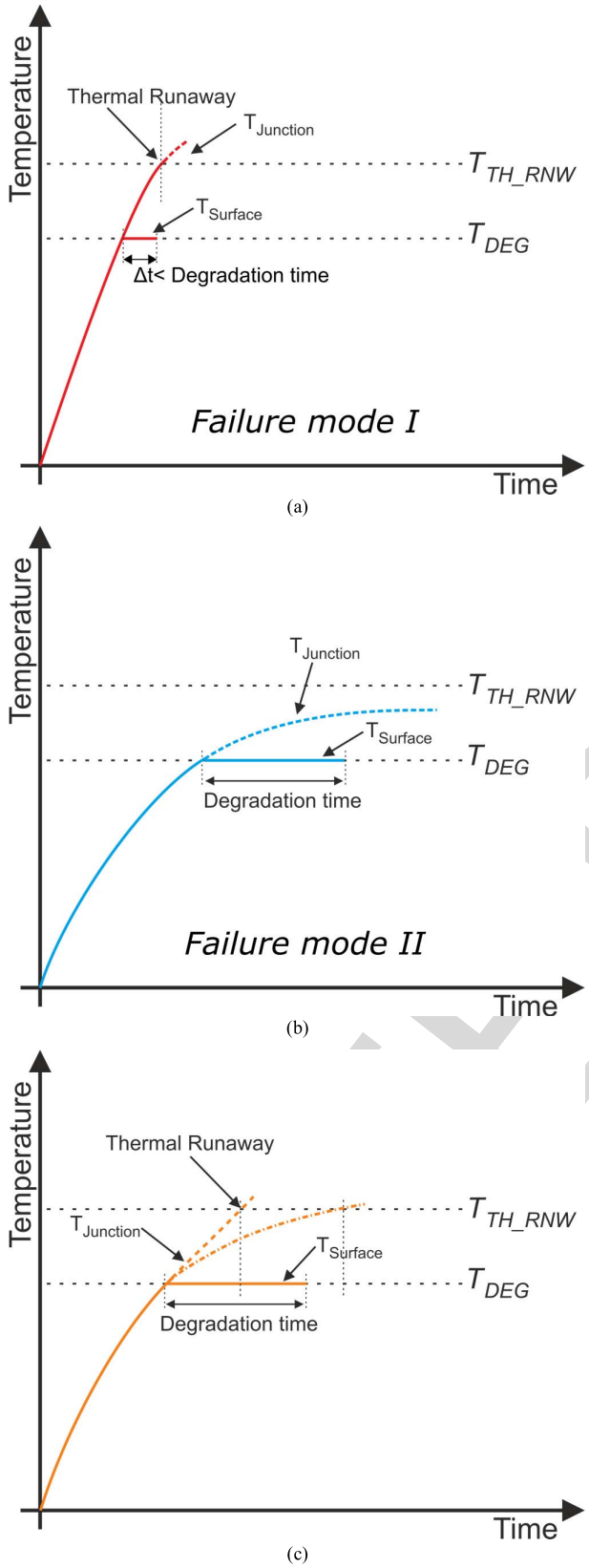
The concept can be better clarified with the aid of Fig. 19. It is useful to define two temperature values:

1) T_{DEG}, when surface degradation occurs;
2) T_{TH_RNW}, when thermal runaway takes place.

The value at which top-layer materials get corrupted is related to the temperature at which melting or change in properties happens in passivation and metallization layers, and it is obviously lower than the triggering point of thermal runaway.

Temperature rise is, of course, related to the amount of power that a device is subjected to, and therefore to the applied voltage. When the power applied is low, temperature has slow dynamics and might reach T_{DEG}, but it cannot reach T_{TH_RNW}. If the surface is exposed to T_{DEG} for sufficient time, permanent damage occurs [Fig. 19(b), *failure mode II*]. The gate/source structure is compromised, and therefore the device loses partially or totally its ability to conduct current.

On the other hand, a higher power leads to a prompt temperature increase. It suddenly reaches T_{TH_RNW}; a large amount of carriers are then generated, and the leakage current reaches



AQ:9 Fig. 19. Interpretation of two types of failure.

386 a value at which thermal runaway is activated. Drain current
387 rises uncontrollably and the device blows up (*failure mode I*).
AQ:10 388 In this case, the time duration for which the device

TABLE I
ARORA MOBILITY MODEL PARAMETERS

A_{min} [cm^2/Vs]	22.83
α_m	-0.536
A_d [cm^2/Vs]	53.92
α_d	-2.2
A_N [cm^{-3}]	$2 \cdot 10^{17}$
α_N	0.72
A_a	0.76
α_a	0.722

remains at T_{DEG} is not enough for the surface to be fully damaged [Fig. 19(a)]. 389 390

Under all other conditions, for a moderate applied power, the failure is regulated by the time needed to degrade the device and the one needed to reach the thermal runaway point. When the former is higher, even if the temperature has a value able to produce detrimental degradation, thermal runaway is the predominant mechanism. 391 392 393 394 395 396

V. CONCLUSION 397

In this paper, interpretation of SC failure event of SiC Power MOSFETs has been given. The aim is to define the limits of their SC capability. 398 399 400

Thanks to the investigation of experimental data, two different failure dynamics have been identified. The first is related to thermal runaway induced by the high value of leakage current. Gate–source shorting due to breakup of top layers is the second failure mechanism observed. Which one occurs depends on the power the device has to dissipate (i.e., by the bus voltage) which affects the temperature rise time. 401 402 403 404 AQ:11 405 406 407

Thanks to numerical simulations, it has been possible to carry out an in-depth analysis of the physics involved in those phenomena. 408 409 410

It is then possible to state that the SC withstanding capability of SiC power MOSFETs is limited by the heat generated inside the structure, specifically in the JFET region. 411 412 413

Even though one of the most marked properties of SiC is the material's higher thermal conductivity, SiC devices have usually reduced volume compared to the same rated silicon devices. It results in extremely high temperature increase, which drastically reduces the device SC ruggedness. 414 415 416 417 418

APPENDIX 419

In Section II-A, the structure implemented was reported, along with the geometrical dimensions [Fig. 1(a)]. As explained, numerical parameters were calibrated to fit the static I_D–V_{GS} curves of a commercial device and to reproduce the same behavior observed experimentally during SC. Among all, mobility and interface traps play a key role. 420 421 422 423 424 425

Channel mobility was modeled using the Arora model implemented in the simulator [37], whose parameters for electrons were chosen during the calibration procedure (Table I), and its analytical expressions are 426 427 428 429

$$\mu_{\text{Arora}} = \mu_{\min} + \frac{\mu_d}{1 + (N_D/N_0)^{A^*}} \qquad \text{(A.1)}$$ 430

TABLE II
INTERFACE DEFECT PARAMETERS

Q_F [cm^{-2}]	$2.68 \cdot 10^{12}$
Q_A [cm^{-2}]	$7 \cdot 10^{11}$
E_0 [eV]	0.18
E_S [eV]	0.1

with

$$\mu_{\min} = A_{\min} \left(\frac{T}{300\ \text{K}} \right)^{\alpha_m}, \quad \mu_d = A_d \left(\frac{T}{300\ \text{K}} \right)^{\alpha_d} \tag{A.2}$$

$$N_0 = A_N \left(\frac{T}{300\ \text{K}} \right)^{\alpha_N}, \quad A^* = A_a \left(\frac{T}{300\ \text{K}} \right)^{\alpha_a}. \tag{A.3}$$

In addition, both positive fixed charges Q_F and acceptor-type traps Q_A were introduced at the SiO_2/SiC interface. Traps were described with a uniform energy distribution [37]

$$E_0 - 0.5E_S < E < E_0 + 0.5E_S \tag{A.4}$$

where E_0 is the center of the energy distribution from the conduction band level E_C. Table II reports the used numeric values.

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