# Experimental Study of the Short-Circuit Performance for a 600V Normally-Off p-Gate GaN HEMT


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***Abstract*—In this paper, the short-circuit robustness of a normally-off GaN HEMT is investigated in relation to applied bias conditions and pulse duration. The results align with previous studies on normally-on devices in highlighting an electrical type of failure. Here, however, the relevance of the specific gate-drive circuit design and corresponding device operational conditions is demonstrated. A gate-bias dependence (GBD) of the failure, correlated to the applied drain-source voltage, is introduced as a novel specific feature for the p-Gate type device.**



***Keywords*—Short-Circuit, GaN, HEMT, Normally-Off, p-Gate, Gate-Bias Dependence.**


## I. Introduction

Semiconductor devices with higher efficiency and reliability are significant milestone for power electronic applications (PEA) in the recent decade. Therefore, the high electron mobility transistor (HEMT), which is a wide band gap (WBG) semiconductor based on an AlGaN/GaN heterojunction, exhibits a promising solution. The unique functionality and characteristics of a GaN HEMT, in comparison to a Si MOSFET or IGBT device, lead to several advantages in the application. On the other hand, in most PEAs the switching devices are required to exhibit a normally-off operation. The usage of insulated- or p-doped gates (p-gate) [1] is one of the key technological solutions to achieve that.

In typical PEAs, a number of overload operational conditions have to be considered to ensure the device- and system/circuit robustness. Typically, this conditions are managed by system-level failure-detection and shut-down mechanisms to avoid destructions. Therefore, a crucial device withstand capability is required, to guarantee their intervention. The short-circuit (SC) robustness is a very important feature of power transistors, strictly required by a number of applications (e.g., motor drives). The common minimum requirement is to withstand a short-circuit with $50\%$ of the maximum breakdown-voltage for an SC duration of $10\ \mu s$. During an SC the device has to be capable of a high power dissipation, that eventually leads to an excessive self-heating related failure. A previous publication of normally-on GaN HEMT SC robustness [2] concluded the failure to be an electrical effect rather than an impact of a thermal issue. It is predicted, that the electrical impact occurs due to an accumulation of holes under the gate, which generates localised high electric fields and causes premature breakdown. Furthermore, the study determined a dependency of the time to failure, which is correlated to the gate-bias.

In this paper, a comprehensive experimental study of a normally-off p-gate HEMT is carried out. The test set-up is presented in chapter II and therefore the impact on the SC behaviour in chapter III. The SC robustness is investigated and presented according to the applied drain-source voltage in chapter IV and the SC duration in chapter V. Furthermore, during the study a variation of the gate-bias occurred, which correlates to the drain-source voltage. The characteristic and impact of this gate-bias dependence (GBD) is as a novelty introduced in chapter VI

## II. Measurement Set-Up

To determine the SC capability of the device, a measurement set-up composed of three major parts is used, as illustrated in Fig. 1. The SC duration can be adjusted by applying a voltage-pulse of a variable time ($t_{\mathrm{SC}}$) on the gate-driver that further transmits an equivalent power-pulse to the gate for biasing the DUT in on-state. Feedback related effects during the SC failure can lead to driver destruction, therefore the gate-loop is galvanic (optical) decoupled. The device under test (DUT) is low inductive linked with an external source and interconnected stabilisation capacitor in the power-path. Hence, the drain-source voltage $V_{\mathrm{DS}}$ can be assumed constant due to the large capacitance value.

Driving a p-gate HEMT features the existence of an on-state forward gate-current $I_{\mathrm{G}}$. The amount of the current

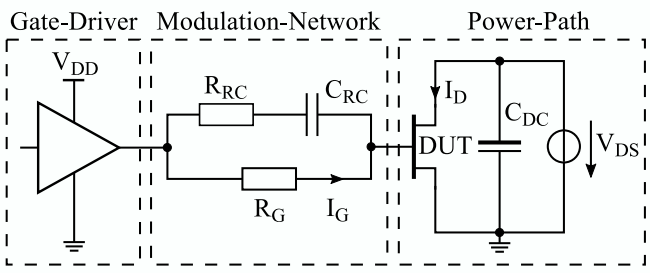


Fig. 1: Test set-up, composed of:
a galvanic (optical) decoupled gate-driver,
a modulation-network of the gate-signal
(common used in p-gate GaN HEMT applications),
and a power-path with the device under test (DUT)

$I_G$ can be adjusted with an appropriate gate-resistance $R_G$. Consequently, the gate-source voltage $V_{GS}$ is set by $I_G$ with the equivalent voltage drop over $R_G$. Therefore, as part of the gate-drive circuit, a modulation-network is used. This topology ensures a, with the usage in PEAs, comparable gate-bias condition of the SC behaviour. Furthermore, the network provides optimised transient on- and off-state bias conditions of the DUT which are illustrated in Fig. 2 (bottom).

## III. SC Behaviour and Test Conditions

Various influences on the SC behaviour, related to the impact of the gate-drive circuit, can be captured. In the following, the relations are exemplary described, together with the extent of variation in the gate-drive circuit.

The waveform of the drain-current $I_D$ is depicted in Fig. 2 (top), with the respective $V_{GS}$ in Fig. 2 (bottom), serving as the impact exemplification. In the first time interval $t_1$ of the SC, a steep rise of the current $I_D$ occurs. The slope is mainly determined by the applied voltage $V_{DS}$ and the parasitic inductance of the SC loop. The p-gate structurally lacks a capacitive nature, therefore $V_{GS}$ is equal to the value of the drive-voltage $V_{GS,peak} = V_{DD}$. During the second time interval $t_2$ the voltage converge to its saturation value $V_{GS,sat}$, in accordance to the functionally of the gate-drive circuit. Therefore, the current $I_D$ tends to decrease, which is further gained due to the impact of the self-heating. The issue of self-heating is related to an excessive power-dissipation and occurs as a thermal mobility degeneration [3]. In the last interval $t_3$, the temperature within the device reaches a stable value, which leads to a respective saturation of the current $I_{D,sat}$.

To cover the impact of the gate-drive circuit, a variation of test conditions is carried out. These test conditions are illustrated in TABLE I, with their respective achievements of SC capability. In the range of bias currents $I_G$ (obtained from $(V_{DD} - V_{GS}) / R_G$), an insignificant nominal reduction of on-state performance is predicted. Therefore, condition A corresponds to a high and B to a low value within this range, in order to investigate transferability on the SC performance and the capability respectively. To investigate the implication of $V_{DD}$, the characteristics of condition C, which exhibits a lower value, are compared to condition B. In order to keep a comparable low bias current $I_G$ condition, the value of $R_G$ is reduced. Due to the GBD (as extensively explained in chapter VI) a decrease of $V_{GS}$, correlated to an increase of $V_{DS}$, can be observed. For comparability of p- and insulated-gate devices, the aim of condition D is to disregard the GBD. Therefore, in all terms of operation, an adjustment of $R_G$ is necessary to ensure a constant operation point.

TABLE I: Variation of test conditions and results of failure related SC limitation. The failure-time is determined with $V_{DS} = 300\ V$ and the failure-voltage with $t_{SC} = 10\ \mu s$.

| Conditon | | A | B | C | D |
|---|---|---|---|---|---|
| Gate-resistance | $R_G\ [\Omega]$ | 470 | 4.7 k | 980 | var. |
| Drive-voltage | $V_{DD}\ [V]$ | 12 | 12 | 5 | 12 |
| Failure-voltage | $V_{DS}\ [V]$ | 350 | 400 | 450 | 225 |
| Failure-time | $t_{SC}\ [\mu s]$ | 20 | 40 | >250 | - |

## IV. Voltage to Failure

The procedure of investigating the voltage restricted SC capability (see TABLE III) involves a retain of the minimum required SC duration and a stepwise increase of the voltage

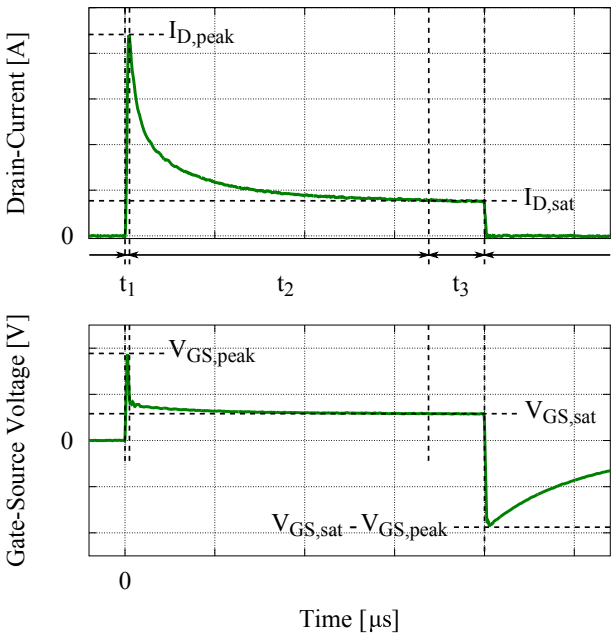


Fig. 2: Drain-current vs. time (top), gate-source voltage vs. time (bottom). Exemplary waveforms of the SC behaviour, within the characteristics according to the gate-drive circuit.

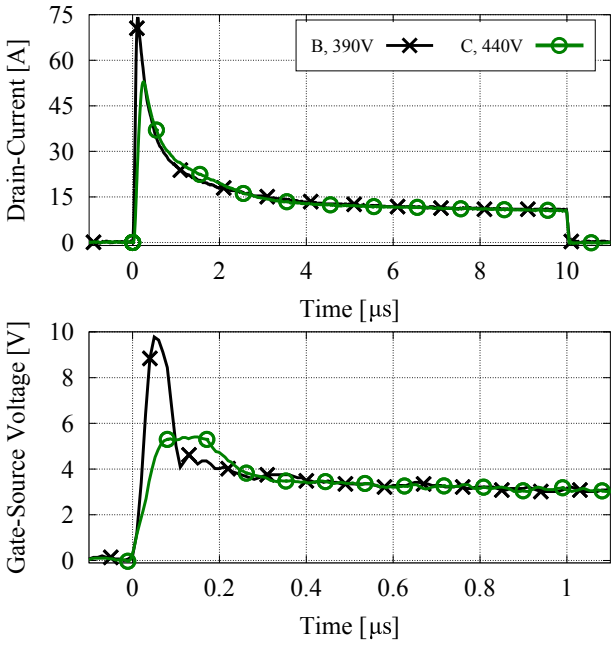


Fig. 3: Drain-current vs. time (top), gate-source voltage vs. time - zoom (bottom). Experimental results of maximum achieved voltage capability, by comparing conditions B and C.

$V_{DS}$, until a failure occurs.

Reaching the voltage restriction leads, in all conditions, to a device destruction within a few hundred nanoseconds. The device withstands the required SC duration for voltages $V_{DS}$ below the failure-voltage, therefore a significant thermal related failure can be neglected. Condition A withstands voltages until $V_{DS} = 340\ V$, whereas with condition B $V_{DS} = 390\ V$ and with C up to $V_{DS} = 440\ V$ is achieved. The earlier restriction of condition A in comparison to B, can be referred to the gate-current and is further detailed in chapter V. The current $I_D$ and the corresponding $V_{GS}$ waveforms for conditions B and C are depicted in Fig. 3. Therefore, the major difference is related to the initial value of the current $I_{D,peak}$, see Fig. 3 (bottom). The carrier density affects the magnitude of the electrical field, which leads to an electrical breakdown in the structure for an exceedance of a critical value.

Furthermore, the range of voltage withstand capability, defined as ratio of failure- and the nominal breakdown voltage, diverse from approximately $60\%$ up to $75\%$ regarding the condition variation.

## V. Time to Failure

The investigation of the SC duration capability (see TABLE III) is similar to the procedure for the voltage restriction. Therefore, the minimum required voltage $V_{DS}$ is kept constant and the time $t_{SC}$ is stepwise increased, until a failure occurs.

For condition C, an SC duration related restriction has not been observed. The waveform of the current $I_D$ is depicted in Fig. 4 (top), together with an estimation of the junction-temperature in Fig. 4 (bottom). The temperature is determined with a numerical 3D temperature simulator which is presented

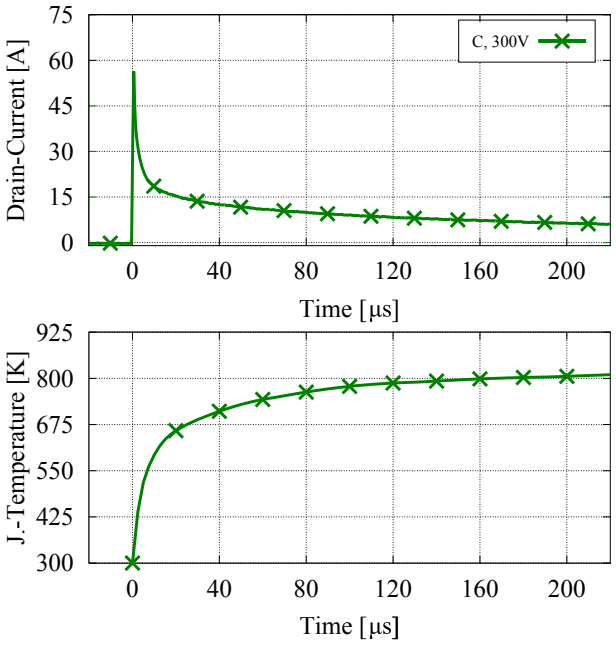


Fig. 4: Drain-current vs. time (top), junction-temperature vs. time (bottom). Extract of the experimental achieved SC duration capability of condition C.

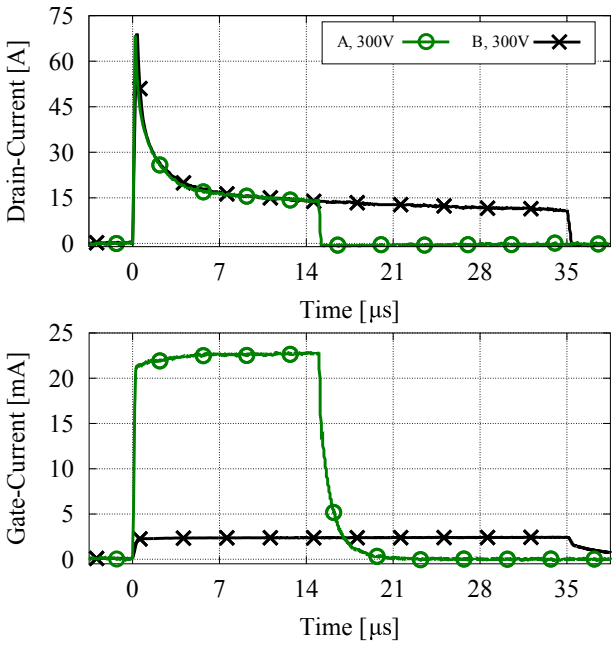


Fig. 5: Drain-current vs. time (top), gate-current vs. time (bottom). Experimental results of maximum achieved SC duration capability, by comparing conditions A and B.

in [4]. The temperature settles for $t_{SC} \geq 160\ \mu s$. An abrupt thermal related failure for higher durations is not expected, based on the results of this investigation respectively the performed operation condition.

For conditions A and B, a clear limitation of the SC duration is observed. The comparison with condition C further emphasizes that the failure is mainly related to the initial value of the current $I_{D,peak}$ (see chapter IV). Considering equal peak values $I_{D,peak}$, in terms of condition A and B, an underlying limitation can be observed. The current $I_D$ waveform, for these two conditions within the last measurement before device destruction are depicted in Fig. 5 (top). Whereas the progression of $I_D$ is identical, the main difference can be observed at the gate-bias current $I_G$. The respective waveforms of $I_G$ are depicted in Fig. 5 (bottom). The value of $I_G$ for condition A is one order of magnitude higher than in B. The injection of holes into the gate increases with the amount of the current $I_G$. Therefore, an assumption of hole accumulation under the gate [2] can be made.

## VI. Gate-Bias Dependence

The SC behaviour of conditions B and D, for two different $V_{DS}$, shows the significant characteristics of the GBD. Therefore, depicted in Fig. 6 (top), the zoom into the SC saturation region of $I_D$ the corresponding $V_{GS}$ (bottom). Comparing the current saturation values $I_{D,sat}$ at a specific voltage (e.g $V_{DS} = 100\ V$), indicates a significant lowering for condition B. This characteristic are further observed for the value of the saturation voltage $V_{GS,sat}$. Furthermore, for both conditions an approximately identical lowering of the current saturation values $I_{D,sat}$, between the two different voltages (e.g.

$V_{DS} = 100\ V$ to $V_{DS} = 200\ V$), occurs. According to the specific aim of condition D (see chapter III) a constant value of $V_{GS,sat}$ is achieved, whereas a $V_{DS}$ dependency occurs in case of condition B. However, the change of $I_{D,sat}$, for a constant bias at condition D, also refers to a thermal mobility degeneration due to excessive power dissipation [3], as discussed in chapter III. Consequently, the further difference of the saturation values between conditions B with D relates to the impact of the GBD.

For an ideally constant current $I_D$, the power dissipation behaves linear within the device, at an increase of voltage $V_{DS}$. According to the thermal mobility degradation a non-uniform power dissipation occurs. Due to the GBD, a further gain of non-uniformity, for the operation of the p-gate HEMT, can be observed. The extent is illustrated as the percentage change of the dissipated power $P_D$ in Fig. 7 (top) and current $I_G$ (bottom), as function of $V_{DS}$ within the minimum required range. Therefore, the percentage change is defined as the ratio of saturation values (at $t_3$, referring to the definition in chapter III) and the respective low voltage SC value. The forced increase of $I_G$ in condition D, in order to achieve a constant operation point, leads to a voltage related failure at $V_{DS} = 225\ V$. Therefore, measurements of higher $V_{DS}$ values could not be achieved. Therefore, the existence of the early failure confirms the observations obtained in chapter V. However, the GBD manifests itself in an unintended increase of $I_G$ approximately $(4\% \cdot I_G)\ /\ (100\ V)$ for $V_{DS} \geq 125\ V$. Furthermore, the p-gate HEMT provides, for increasing values of the drain-source voltage, a respective self-contained lowering of performance-related temperature gain.

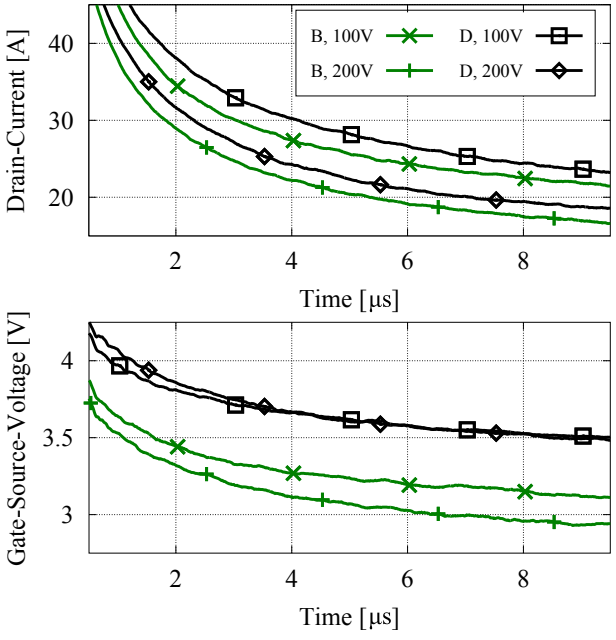


Fig. 6: Drain-current vs. time - zoom (top), gate-source voltage vs. time - zoom (bottom). Experimental results, illustrating the significant behaviour of the gate-bias dependence, by comparing conditions B and D.

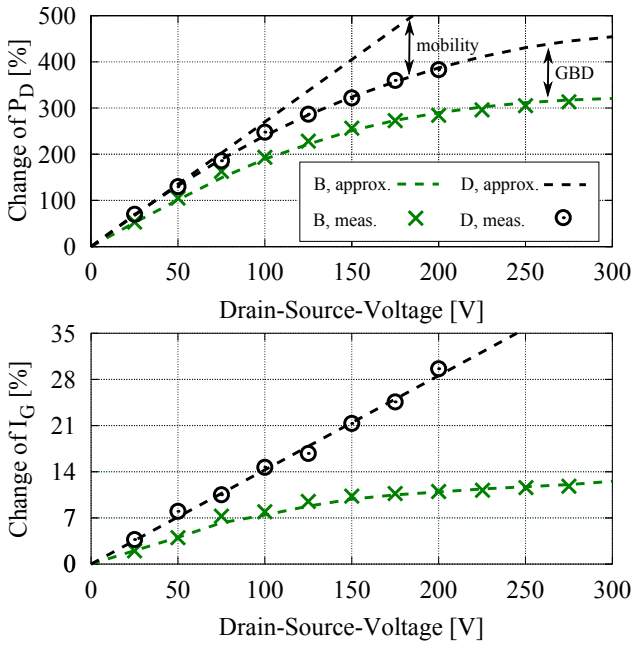


Fig. 7: Power dissipation vs. drain-source voltage (top), gate-current vs. drain-source voltage (bottom). Experimental results, illustrating the impact of the gate-bias dependence, by comparing conditions B and D. Therefore, the change is defined as e.g.: $P_{D,sat}(V_{DS})\ /\ P_{D,sat}(V_{DS} \leq 3\ V) \cdot 100\%$

## Conclusion

This paper has shown that the short-circuit withstand capability of p-Gate GaN HEMTs is mainly limited by the initial drain-current peak and the value of the gate-current. Both factors are strongly dependent on the design of the gate-drive circuit: optimised design can yield voltage robustness up to 75%, with very long pulse widths for lower values. The observed gate-bias dependence exhibits a self-protecting decrease of the current and power dissipation level during the pulse. Due to this, higher short-circuit capability is achieved if the drain-current peak and gate-current value is kept low, for increased voltages.

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