A Physical RC Network Model for Electro-Thermal Analysis of a Multichip SiC Power Module

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***Abstract*–This paper is concerned with the thermal models which can physically reflect the heat-flow paths in a lightweight three-phase half bridge, two-level SiC power module with 6 MOSFETs and can be used for coupled electro-thermal simulation. The finite element (FE) model was first evaluated and calibrated to provide the raw data for establishing the physical RC network model. It was experimentally verified that the cooling condition of the module mounted on a water cooler can be satisfactorily described by assuming the water cooler as a heat exchange boundary in the FE model. The compact RC network consisting of 115 R and C parameters to predict the transient junction temperatures of the 6 MOSFETS was constructed, where cross-heating effects between the MOSFETs are represented with lateral thermal resistors. A three-step curve fitting method was especially developed to overcome the challenge for extracting the R and C values of the RC network from the selected FE simulation results. The established compact RC network model can physically be correlated with the structure and heat-flow paths in the power module, and was evaluated using the FE simulation results from the power module under realistic switching conditions. It was also integrated into the LTspice model to perform the coupled electro-thermal simulation to predict the power losses and junction temperatures of the 6 MOSFETs under switching frequencies from 5 kHz to 100 kHz which demonstrate the good electro-thermal performance of the designed power module.**

***Index Terms*–MOSFETs, SiC power module, finite element methods, RC network, curve fitting, three-phase inverters.**

I. INTRODUCTION

The high performance of SiC power devices at high frequency, high power and high temperature applications make them attractive in avionic industry. In the present work, a three-phase half bridge, two-level SiC power module based on CREE CPMF-1200-S080B Z-FET^{TM}MOSFETs has been designed and developed specifically for avionic applications, where high gravimetric and volumetric power density and efficiency are highly desirable. In the previous publications [1, 2], the design, fabrication and electrical test of the assembled module were reported. This paper is concerned with the thermal models for electro-thermal analysis of the assembled module using the finite element (FE) method and a physical compact RC thermal network. The FE model is especially calibrated with experimental data and can be used to calculate the temperature field for further thermo-mechanical design and optimization, and collect the temperature data for extracting the R and C parameters of the compact RC thermal network model. The latter can be used to rapidly calculate the junction temperatures of the power devices for further electro-thermal design, thermal management, reliability and lifetime prediction of the power module.

There has been a wealth of work in the thermal models for electro-thermal analysis of power modules [3-15]. Finite element method (FEM) and finite difference method (FDM) were commonly employed for the detailed three-dimensional (3D) modeling and accurate simulations of the power packages and/or modules. They were further used in the model order reduction approach to generate compact thermal models by mathematical manipulation of linear matrix [11-13], or by a generalized minimized residual algorithm [10]. Fourier series based thermal models were also used for 3D transient thermal simulation of power modules, with the assumptions of perfect cuboid for each layer in the packaged structures and temperature independent material properties [7-9]. All these mentioned thermal models were developed to solve the 3D heat diffusion equation subjected to the boundary conditions of either fixed temperatures [13-15] or heat exchanges with the ambient/coolants [7-12]. However, the power modules are rarely encountered with a fixed temperature boundary condition in realistic applications. On the other hand, for all those developed thermal models with the heat exchange boundary conditions, the thermal capacitance contribution from the heat sink and/or thermal grease were ignored during the transient thermal simulations. Therefore, it is still important to experimentally evaluate the FE thermal model for any newly developed power module.

Compact thermal models expressed as thermal resistor-capacitor (RC) networks were more widely employed to rapidly predict junction temperatures or the temperatures at a few critical locations in the power modules for electro-thermal design, thermal management, reliability and lifetime prediction [15-24]. In the simplified cases, individual power device might be considered and one dimensional heat conduction was assumed to predict the junction temperatures [23-25]. The models were constructed using either Cauer cells or Foster cells, while mathematic methods have been developed and well

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known to transform these two network models from each other [24-26]. Generally speaking, the Foster networks were used as behavior models to calculate the transient junction temperatures, while the R and C parameters in the Cauer networks were taken to have true physical meanings. In most cases, multiple power devices with both self-heating and cross-heating effects were considered [15-21]. In these models, no matter whether it is self-heating or cross-heating, the heating contribution from each power device was described using a Foster network. Then the module containing m power devices employed m×m Foster networks to represent all the self-heating and cross-heating effects.

In the present paper, the FE model has first been developed to simulate the transient temperature fields of the three-phase half bridge, two-level SiC power module which was mounted on a water cooler. In comparison with the previous detailed 3D models [10-15], the present FE model has taken into account of thermal capacitance contributions from the heat sink and the voids/defects in the solder joints to attach the SiC MOSFETs. The improved accuracy of the FE simulation results was evaluated with experimentally measured junction temperatures of the MOSFETs. Then the compact RC network model consisting of 115 R and C parameters to predict the transient junction temperatures of the 6 MOSFETS has further been developed, where cross-heating effects between the MOSFETs are represented with lateral thermal resistors. Such a compact RC network model represents the real structure and heat-flow paths within the module much better than those RC network models reported in the existing literature [15-21], but there is no existing method to effectively determine the R and C parameters.

The specific objectives of this paper are: 1) to experimentally test the transient junction temperatures of the 6 MOSFETs under 3 sets of heating conditions; 2) to compare the FE simulation results with the experimentally tested transient junction temperatures of the MOSFETs; 3) to demonstrate the improved prediction accuracy of the FE models taking into account of both the thermal capacitance contribution from the heat sink and the voids/defects in the solder joints; 4) to present the compact RC network model better representing the real structure and heat-flow paths within the module; 5) to develop an effective method for reducing the challenge of curve fitting to determine the R and C parameters of the compact RC thermal network model consisting of large numbers of R and C parameters; 6) to formulate a method of coupled electro-thermal simulation to rapidly predict the steady power losses and junction temperatures of the MOSFETs under realistic switching conditions; and 7) to reveal the electro-thermal performance of the designed compact and light three-phase half bridge, two-level SiC power module using the conventional packaging technologies.

II. THE SIC POWER MODULE AND THERMAL TEST

A. Description of the SiC power module

The SiC power module has been designed to integrate three half-bridge switches onto a single base plate using the conventional solder reflow and wire bonding as the packaging technologies. As described in Fig. 1, there are 2 SiC dies (labelled as M1 and M2, M3 and M4, or M5 and M6), 6 relatively large S shape pins and 4 relatively small S shape pins sitting on one substrate to form each of the three half-bridge switches. The SiC dies are CREE 1.2 kV CPMF-1200-S080B Z-FET^{TM}MOSFETs, and the footprint of one MOSFET is 4.08 × 4.08× 0.365 mm. Both the bigger and smaller S shape pins are made of Ni-plated Cu, and they are the power and drive terminals, respectively. The substrate is 0.635 mm thick Si_3N_4 ceramic tile with 0.4 mm thick Cu tracks on the front side and 0.3 mm thick Cu plate on the back side. The interconnections between the SiC MOSFETs, Cu tracks and the S shape pins are achieved using Al wire-bonds (250 μm in diameter). The base plate is Al-SiC composite consisting of 37 vol% Al alloy and 63 vol% SiC.

During the prototyping process, the SiC MOSFETs were first attached on the substrates using the eutectic Sn-3.5Ag solder joints with a thickness of 100 μm. Then the Al wires were bonded on the MOSFETs and the corresponding Cu tracks to form the interconnections. Following this, by employing a solder reflow jig made of PEEK, the S shape pins were bonded on the top sides of the substrates, and the back sides of the substrates were bonded on the AlSiC base plate (3 mm in thickness) using Pb36Sn2Ag solder joints with a thickness of 200 μm. Finally, the assembled module is mounted under a plastic housing, filled with dielectric silicone gel and covered by a plastic lid.

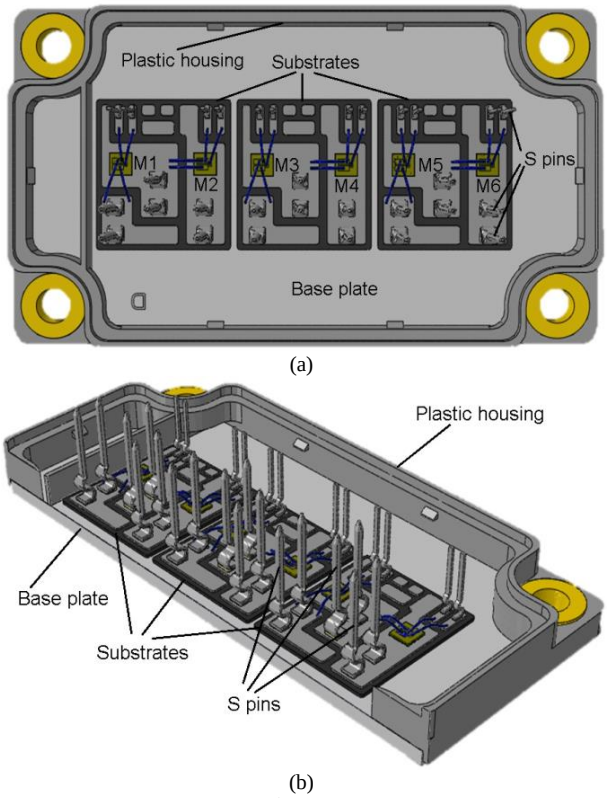


Fig. 1. The designed three-phase half bridge, two-level SiC power module with the silicone gel and plastic lid being invisible: (a) top view; and (b) cut iso view.

Figure 2 presents one X-ray projection image of one assemble SiC power module especially showing the quality of

the Sn-3.5Ag solder joints used to attach the 6 SiC MOSFETS. Significant amounts of voids with percentages of 15%, 32% and 7% can be observed in the three Sn-3.5Ag solder joints to attach the MOSFETs M1, M5 and M6, and should be avoided in real manufacturing. In the present paper, such an assembled power module had particularly been inspected with the X-Ray which is not recommended due to possible detrimental impact on the MOSFETs, and used to investigate the effect of the imperfect solder joint on the transient thermal performance. The latter can also be considered as a contribution of the present work.

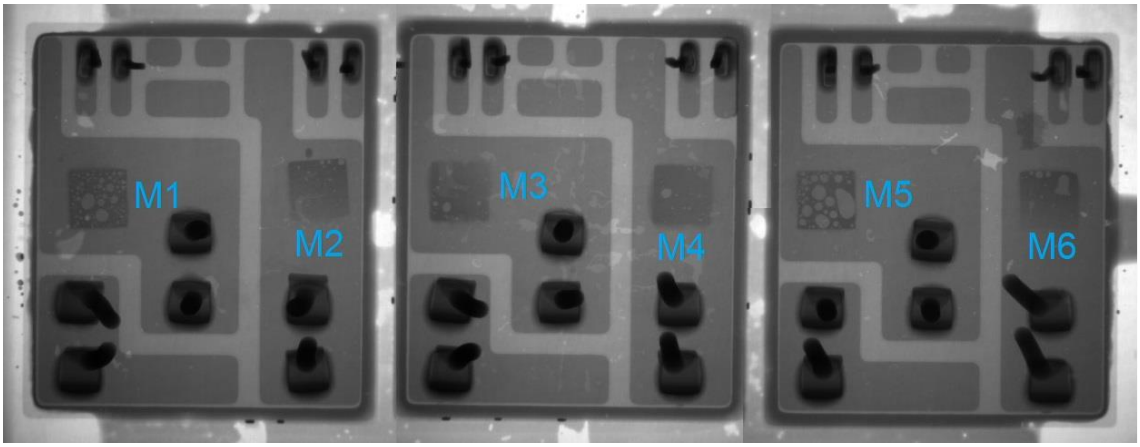


Fig. 2. X-ray projection image of one assembled three-phase half bridge, two-level SiC power module.

B. Transient thermal test

The transient thermal test of the assembled SiC power module was carried out to evaluate and calibrate the finite element (FE) model. Prior to the transient thermal test, the SiC power module was fixed on a temperature controlled hot plate to obtain the calibration curves describing the relationships between the junction temperature and the forward voltage of the body-diode, V_F, as the temperature sensitive parameter for all the 6 MOSFETs. The resulting calibration curves were obtained under a low measurement current, I_M, of 40 mA and are given in Fig. 3. Here and also in what follows, the gate was shorted to the source for each of the MOSFETs to prevent current flowing through the channel [27]. It can be seen that the junction temperature linearly decreases with increasing the forward voltage of the body diode for each of the MOSFETs.

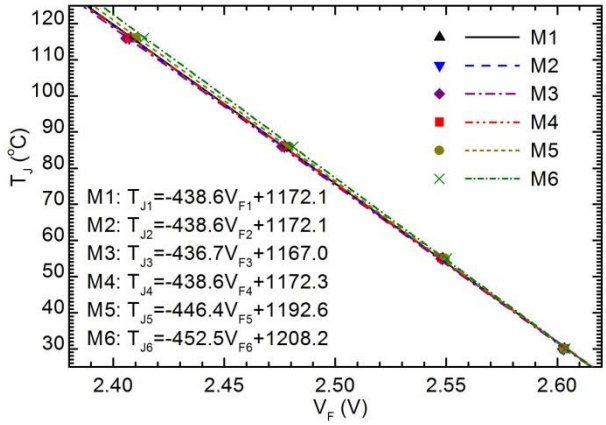


Fig.3. The calibration curves used to reconstruct the junction temperatures of the 6 SiCMOSFETs.

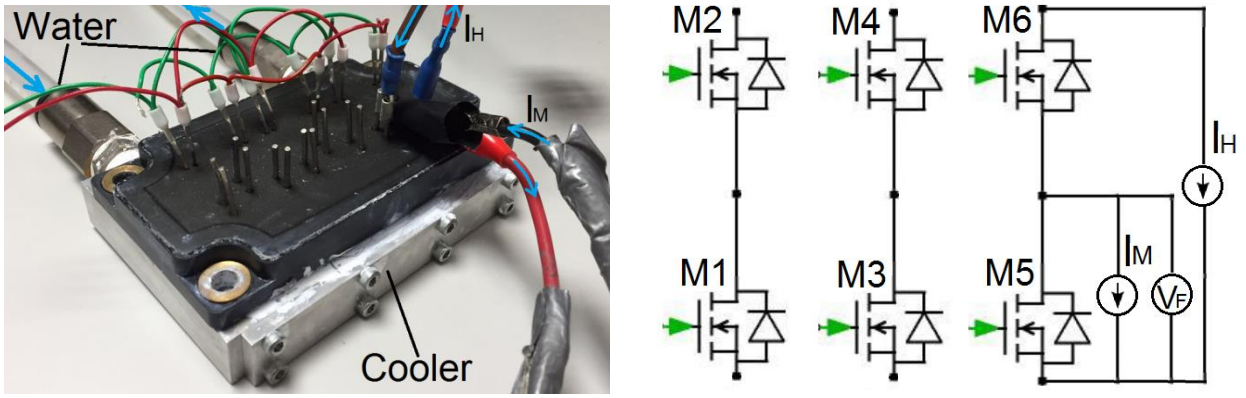
During the transient thermal test, the module was mounted on a water cooler using thermal grease as shown in Fig. 4. Three groups of the transient test which were sufficient to evaluate the FE model and convenient to connect the test cables were performed. In each group of the test, a heating current, I_H, 10 A was first passing through the body diodes of the two MOSFETs sharing the same substrate, i.e. M1 and M2, M3 and M4, or M5 and M6, for 10 minutes to reach the steady state. This corresponds to a total heating generation approximately of 65 W for 10 minutes, and hence ensures reasonably uniform average temperature of the water flowing under the 6 MOSFETs. Then the current was switched off, and immediately the forward voltages of the body diode of either a self-hearted MOSFET or a cross-heated MOSFET were collected using the measurement current 40 mA at a sampling time 1.0×10^{-4} s. The transient curve of voltage versus time for only one MOSFET were collected during each time, and thus 6 times of heating the two MOSFETs first and subsequently collecting the voltage data during the cooling stage were conducted to finalize each group of the transient test. Using the calibration curves shown in Fig. 3, all the voltage data were converted into the junction temperatures of the MOSFETs. The resulting transient curves of temperature versus time were further smoothed with adjacent averaging of 20 points.

III. FINITE ELEMENT MODEL

A. Meshing system

The FE modelling and simulation has been done using commercially available software Abaqus 6.11-3. As in the previous 3D transient thermal models [10-12], the thermal grease and heat sink were not included in the present geometric model. However their contributions to the thermal capacitance were explored by appropriately increasing and tuning the specific heat of the base plate as detailed below. The injected silicone gel was also excluded from the model

because its effect is negligible due to extremely low thermal conductivity. The meshing system consisting of 598269 elements (C3D8 linear brick elements, DC3D6 linear triangular prism elements and DC3D10 quadratic tetrahedron elements) was used to discretize the three-phase half bridge, two-level SiC power module. The elements with varied sizes were employed, where the largest element is 1× 1× 1 mm, and the smallest element is 0.25× 0.25×0.025 mm if all the elements are imagined as the equivalent brick elements. The present FE simulation has been to obtain the transient evolutions of the averaging temperatures on the top active regions of the 6 MOSFTEs as labelled in Fig. 1. Further increase in the density of the meshing system was found to have a change less than 0.1% for all the resulting temperatures.



(a) (b)

Fig.4. The set up of the transient thermal test for M5 and M6 to be heated and the junction temperatures of M5 to be measured: (a) photograph of the SiC power module mounted on a water cooler; and (b) the electrical diagram.

B. Thermal load and boundary conditions

Depending on the simulation case, the initial temperature of the SiC power module was set at 27.5 °C, 0 °C or 25 °C. Constant or switching dependent surface heating sources were applied on the top sides of one, two or six SiC MOSFETs (excluding the gate pads). The heat exchange boundary condition was placed between the bottom cooling surface of the base plate and the ambient, where the heat exchange coefficient of 2750 $W{\cdot}m^{-2}{\cdot}k^{-1}$ was determined through matching the simulated junction temperatures of the MOSFETs with those obtained from the three groups of transient thermal test. In addition, a heat exchange coefficient of 5500 $W{\cdot}m^{-2}{\cdot}k^{-1}$ was also used in 6 simulation cases for comparison. The transient time for most simulation cases lasted for 1000 seconds for ensuring to reach the steady state. These transient simulations were carried out for the heating stage, and the resulting curves of temperature versus time can easily be inverted into the corresponding curves for the cooing stage [28].

C. Properties of materials

The thermo-physical properties of the materials reported in the existing literature [29-33] or given in the datasheet of the commercially available material [34] have been used as the benchmark in the simulations, and are listed in Table I. In order to take into account of thermal capacitance from the thermal grease and heat sink as aforementioned, the specific heat of the Al-SiC composite base pate was appropriately increased. This was done by tuning the value of the specific heat until that the simulated curves of the junction temperature versus time matched best with the experimentally tested curves. The value of the specific heat determined through the tuning is listed in the parenthesis in Table I. All the data listed in Table 1 are temperature-independent, and this is commonly assumed in the electro-thermal analyses of power modules and especially in the construction of compact RC network models. As demonstrated in the work [10, 35], for temperature variations of around 60–80 °C, this assumption leads to an expected error of 2–3% for typical power module structures. For higher temperatures, it may be necessary to use nonlinear compact models and thereby time-dependent thermo-physical properties of the materials.

TABLEE I
THERMO-PHYSICAL PROPERTIES OF THE MATERIALS USED IN THE TRANSIENT THERMAL SIMULATIONS

	SiC	Si_3N_4	Cu	Al	Sn-3.5Ag	Pb36Sn2Ag	Al-SiC	Plastic
Thermal conductivity [W/(K·m)]	370	70	398	238	33	100	200	0.52
Specific heat [J/(kg·°C)]	750	691	380	880	200	167	741 (1000)	1150
Density [kg/cm^3]	3.21	2.40	8.85	2.70	7.36	8.41	3.01	1.43

D. Simulation cases and execution

A few trials of the FE simulation were first carried out to tune and select the heat exchange coefficient and the specific heat of the Al-SiC base plate. These were done by comparing

the simulation results with those from the transient test at time of 0.1 to 10 s. Then the simulation cases listed in Table II are presented in this paper. Here cases B1 to B3 were done with appropriately increased specific heat of the Al-SiC base plate and imperfect Sn-3.5Ag solder joints as shown in Fig. 2 for matching the results of the transient thermal test. The thermal loads applied on the MOSFETs were the heat dissipations of the body diodes of the MOSFETs during the transient thermal test. Cases A1 to A3 were used to compare with cases B1 to B3 for revealing the effects of the increased specific heat of the Al-SiC base plate and the imperfection of the Sn-3.5Ag solder joints. Cases C1 to C6 and D1 to D6 were done with unit heat input and zero ambient temperature, and the simulation results of junction temperatures are actually transient thermal impendence from junction to ambient. They were used to collect the data for extracting the R and C parameters of the compact RC thermal network model under two cooling conditions. In addition, another two cases E1 and E2 were employed to evaluate the established compact RC network model.

All the simulations and calculations in the present paper were executed using the parallelization computation of 8 cores in a PC with Intel[R] Core[TM] i7-3820 CPU @ 3.60 GHz processor and 64 GB RAM. With the exception of cases E1 and E2, all the other cases were simulated using logarithmic scale time increments from 10^{-5} to 10^{3} seconds, and the number of the increments within each order of the magnitude was 10. The running time was about 50 minutes if a finer meshing system was used. It could be reduced to 3 minutes and even shorter by employing relatively coarse meshing system and allowing a maximum change of 0.5% for all the resulting junction temperatures. The relatively coarse meshing system, different simulation times and time increments were employed for cases E1 and E2, and the relevant details for these two cases will be presented in the Subsection C. Evaluation of the compact RC network model in Section IV below.

TABLEE II
THE SIMULATION CASES WHICH WERE CARRIED OUT USING THE FE TRANSIENT THERMAL MODEL

Simulation case	Thermal loads	Heat exchange ($W \cdot m^{-2} \cdot °C^{-1}$)	T∞ (°C)	Specific heat of base plate (J/(kg·°C)	Sn-3.5Ag solder joints
A1	33.8 W on M1, 31.9 W on M2	2750	27.5	741	Ideally perfect
A2	32.5 W on M3, 33.0 W on M4	2750	27.5	741	Ideally perfect
A3	33.8 W on M5, 31.9 W on M6	2750	27.5	741	Ideally perfect
B1	33.8 W on M1, 31.9 W on M2	2750	27.5	1000	Real with voids
B2	32.5 W on M3, 33.0 W on M4	2750	27.5	1000	Real with voids
B3	33.8 W on M5, 31.9 W on M6	2750	27.5	1000	Real with voids
C1	1 W on M1	2750	0	1000	Real with voids
C2	1 W on M2	2750	0	1000	Real with voids
C3	1W on M3	2750	0	1000	Real with voids
C4	1W on M4	2750	0	1000	Real with voids
C5	1 W on M5	2750	0	1000	Real with voids
C6	1W on M6	2750	0	1000	Real with voids
D1	1 W on M1	5500	0	1000	Real with voids
D2	1 W on M2	5500	0	1000	Real with voids
D3	1W on M3	5500	0	1000	Real with voids
D4	1W on M4	5500	0	1000	Real with voids
D5	1 W on M5	5500	0	1000	Real with voids
D6	1W on M6	5500	0	1000	Real with voids
E1	Detailed in Section IV	2750	25	1000	Real with voids
E2	Detailed in Section IV	2750	25	1000	Real with voids

IV. COMPACT RC NETWORK MODEL

A. Construction of the compact RC network

As described in Fig. 5, the compact RC network model of the SiC power module has been constructed based on the one-dimensional 8-rung Cauer RC thermal network. The latter was selected because vertically the heat-flow paths of all the 6 MOSFETS pass through 8 physical layers in the FE model: SiC MOSFET, Sn-3.5Ag solder joint, Cu, Si_3N_4 ceramic, Cu, Pb36Sn2Ag solder joint, Al-SiC base plate and ambient. The cross-heating effects between the MOSFETs are implemented using lateral resistors. If the two MOSFETs share one substrate, 5 lateral resistors are used to interconnect the neighboring two vertical heat-flow paths. Otherwise, only 2 lateral resistors are used to interconnect the neighboring two vertical heat-flow

paths. Such a compact RC network represents a discretised image of the real structure and heat-flow paths in the SiC power module. It is not only more compact than the corresponding m×m Foster networks with 16×6×6=576 R and C parameters, but also relatively convenient to consider temperature-dependent R and C parameters when necessary.

B. Extraction of the R and C parameters

If the heat-flow paths in the SiC power module are known, the R and C parameters of the RC network can directly be calculated with the thermo-physical properties of the materials as listed in Table I. In reality, it is not a simple task to obtain the accurate dimensions of the three-dimensional heat-flow paths. In the present work, the R and C parameters are extracted from the FE simulation results of the cases C1 to C6 or D1 to D6. The R and C parameters can be extracted because in the RC network described in Fig. 5, the nodal temperatures can be calculated using the following ordinary differential equation system:

$$K \cdot T + C \cdot \frac{dT}{dt} = P \tag{1}$$

where T is the vector of nodal temperatures, K and C are the thermal conductivity and capacitance matrices, and P is the vector of thermal loads. The K and C matrices can be expresses as:

$$K = \begin{bmatrix} 1/R_{11} & -1/R_{11} & & \dots & 0 \\ -1/R_{11} & 1/R_{11}+1/R_{12} & & \dots & 0 \\ \vdots & \vdots & \ddots & & \vdots \\ 0 & 0 & \dots & & 1/R_{67}+1/R_{68}+1/R_{568} \end{bmatrix} \tag{2}$$

$$C = \begin{bmatrix} C_{11} & 0 & \dots & 0 \\ 0 & C_{12} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & C_{68} \end{bmatrix} \tag{3}$$

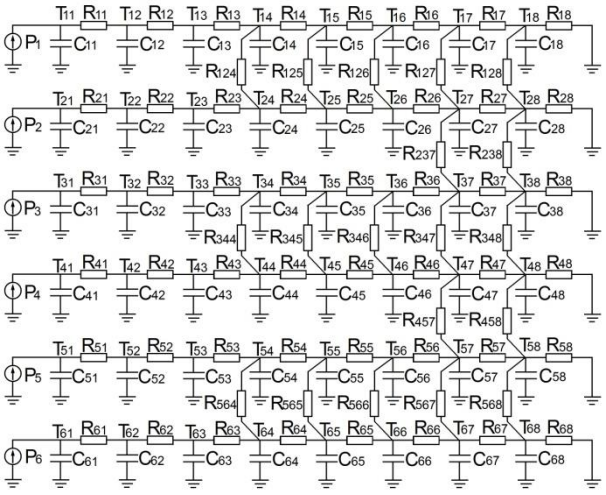


Fig.5.The compact RC network model including both self-heating and cross-heating effects of the 6 MOSFETs.

Through curve fitting of the FE simulation results to equation system (1), the R and C parameters in the RC network model could be extracted. Here the FE simulation results are the 36 self-heating and cross-heating curves of the transient temperatures for all the 6 MOSFETs in the simulation cases C1 to C6 or D1 to D6. The accuracy of the curve fitting can be evaluated by root mean square error between the RC network predictions and the FE simulation results. However, with the 115 R and C parameters in the RC network, it is very challenging and computation time consuming to achieve accurate curve fitting without good estimation of the initial values. To overcome the above challenging, a three-step curve fitting method as described in Fig. 6 has been developed and can be considered as one important contribution from the present work. This curve fitting method is further described as follows:

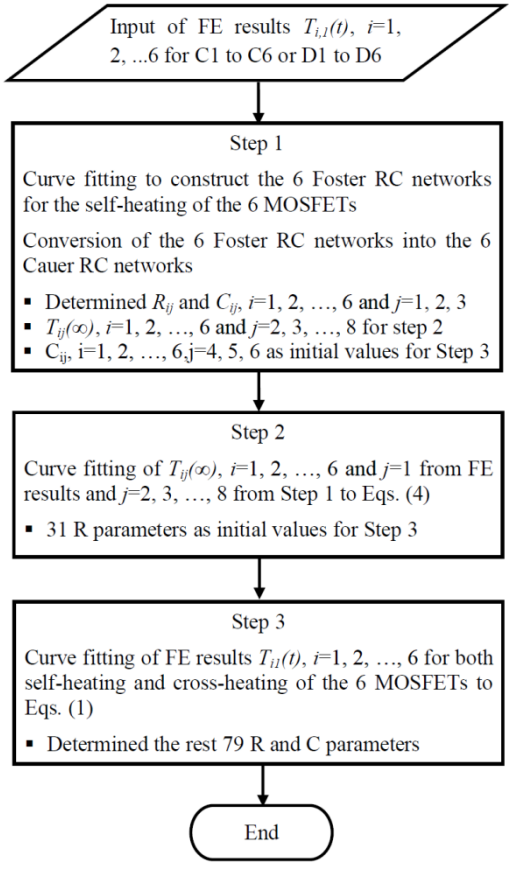


Fig. 6. The flowchart describing the three-step curve fitting method to R and C parameters of the RC network.

First, the one-dimensional 8-rung Cauer RC network as shown in Fig. 7was constructed to consider the self-heating effect only for each of the 6 MOSFETs. This was done using

the established curve fitting method which starts with the construction of the Foster RC network and then converts it into the corresponding Cauer network [24-26]. The R and C parameters of the 6 Cauer RC networks for the 6 MOSFETs were thus extracted from the FE simulation results of the transient junction temperatures, $T_{i1}(t)$, i=1, 2, …, 6, for cases C1 to C6 or D1 to D6. As shown in Fig. 5, no lateral resistor is interconnected between the nodes if their orders in the rung are lower than 4. The R_{ij} and C_{ij} parameters where i=1, 2, …, 6 and j=1,2 and 3 which were extracted in this step were thus taken as the determined values for the compact RC network shown in Fig. 5. The extracted C_{ij} parameters where i=1, 2, …, 6 and j=4, 5, and 6 would be used as the initial values for the third, i.e., the final step of the curve fitting.

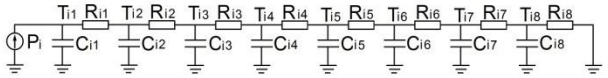


Fig. 7.The Cauer RC thermal network considering the self-heating effect only for each of the 6 MOSFETs.

The second step was carried out to estimate the initial values of all the rest 31 R parameters which would be extracted in the third, i.e., the final step of the curve fitting. In this step, the 6 one-dimensional 8-rung Cauer RC networks constructed in the first step for the self-heating effects of the 6 MOSFETs were used to calculate 42steady nodal temperatures, $T_{ij}(\infty)$ where i=1, 2, …, 6 and j=2,3, …, 8. These 42 steady nodal temperatures were assumed to be same as those in the compact RC network shown in Fig. 7 under the same power inputs and steady state. Another 36 steady nodal temperatures, $T_{i1}(\infty)$ where i=1, 2, …, 6, can directly be read from the FE simulation results of cases C1 to C6 or D1 to D6. The initial values of the 31 R parameters for the final step of the curve fitting could thus be estimated by fitting the 78 steady nodal temperatures to the following equation system (4):

$$K \cdot T = P \tag{4}$$

Finally, with the initial values estimated in the above steps 1 and 2, the values of another 79 R and C parameters were extracted by fitting the FE simulation results of cases C1 to C6 or D1 to D6 to equation system (1) as aforementioned. In both this step and the second step, additional constraints were applied to all the R and C parameters with the same rungs: the minimum value must be higher than half of the maximum value. These constraints were based on both the structure of the SiC power module and the results obtained in the first step of the data fitting.

The above three-step data fitting method was implemented using self-written codes of Matlab 2014b where the date and/or curve fittings were evaluated using function "fminsearch" and the ordinary differential equation system was solved using function "ode15s". The running time was about 2 minutes for both the 1st step and the 2nd step, and was about 2 to 10 minutes to achieve a root mean square error of 0.0024 to 0.0009 °C for the 3rd step.

C. Evaluation of the compact RC network model

The compact RC network model has been evaluated by comparing the junction temperatures of the 6 MOSFETs which were simulated using the compact thermal RC network model and the FE model for the power module to be operated under two switching frequencies of 5 kHz and 100 kHz (cases E1 and E2 in Table II). As described in the previous publications [1, 2], the three-phase half bridge, two-level SiC power module was designed for an avionic system where the input DC link voltage is 540V, full load is 6 kW, and output phase-to-neutral root mean square (RMS) voltage is 115 V with fundamental frequency of 50 Hz. The LTspice model was hence constructed based on the test setup for the full load of 6 kW as detailed in the previous publications [1, 2]. Here the SPICE model of the SiC MOSFET was adopted from the model C2M0080120D provided by CREE, where only the in-built 6 RC thermal networks in the 6 MOSFETs were replaced by the present RC network model. The power loss, i.e. heat generation from each MOSFET was a function of the simulation time, and was the absolute of the product of the collected current passing through and voltage drop across the drain and the source. Such power loss actually contained an artificial switching loss of the body diode during its reverse recovery, and hence was significantly overestimated. However, this would not weaken by any means the validity of evaluating the RC network model with the FE simulation results. In addition, the parasitic inductances of 6.76 nH and 6.32 nH which were obtained from electro-magnetic simulation were connected in series with each of the MOSFETs at the DC+ and DC- sides, respectively. The gates of the 6 MOSFETS were controlled using the sinusoidal pulse width modulation signals [36].

The junction temperatures and power losses of the 6 MOSFETs were first simulated using the simulator LTspice IV by Linear Technology. The transient junction temperatures of the 6 MOSFETs were actually calculated using the present RC network model. Then the junction temperatures of the 6 MOSFETs were further simulated using the FE model under the power losses and time increments the same as those in the LTspice simulation. For the switching frequency of 5 kHz, the running time of the LTspice model for one fundamental output cycle of 20 milliseconds, was 4 minutes. The running time of the FE model using the same 84000 increments for a transient time of 1 millisecond was approximately 53 hours. For the switching frequency of 100 kHz, the running time of the LTspice model for one fundamental output cycle of 20 milliseconds was 44 minutes. The running time of the FE model using the same 125647 increments for a transient time of 0.1 millisecond was about 79 hours.

D. Electro-thermal simulation with the RC network model

In principle, the above constructed LTspice model integrating the RC network model can be used to perform the transient electro-thermal simulation of the SiC power module starting from the initial state to the steady state. However, this is still too time-consuming for a transient time longer than 10 seconds. Therefore, in the present work, the established RC network model and the above constructed LTspice model integrating the RC network model have jointly been employed to perform the coupled electro-thermal simulation for predicting the steady power losses and junction temperatures of

the 6 MOSFTs in the SiC power module under the switching frequencies of 5, 10, 20, 40, 60, 80 and 100 kHz. Here the SPICE model of the SiC MOSFET was further modified, and the artificial switching loss of the body diode during its reverse recovery was removed from the power loss. In the RC network model, the R and C parameters for the cooling condition with a heat exchange coefficient of 2750 $W \cdot m^{-2} \cdot K^{-1}$ were taken. For each switching frequency, the electro-thermal simulation was carried out with the following steps:

(i) The LTspice model without the RC network model, i.e. by fixing the junction temperatures of all the 6 MOSFETs at 25 °C, was employed to simulate the temperature-independent response for a transient time of 100 ms, i.e. 5 fundamental output cycles. From the simulation result, the temperature-independent average power loss, P_{LA}, of each MOSFET during one fundamental output cycle was calculated with:

$$P_{LA} = \int_{t=80ms}^{t=100ms} |I_M(t)V_{DS}(t)|dt/T_P \quad (5)$$

where t is transient time, I_M is the current passing through the MOSFET but excluding the reverse recovery current of the body diode, V_{DS} is the voltage drop across the drain and source, and T_P is the fundamental output period of 20 ms.

(ii) The separate RC network model was used to simulate for a transient time of 1000 seconds to obtain the steady junction temperatures of the 6 MOSFETs in the SiC power module with the calculated power losses.

(iii) With the steady junction temperatures of the 6 MOSFETs obtained in step (ii) as the initial temperatures, the LTspice model integrating the RC network model was used to simulate the coupled electro-thermal response for a transient time of 100 ms, i.e. 5 fundamental output cycles. From this simulation result, the temperature-dependent average power loss and average junction temperature of each MOSFET during one fundamental output cycle were calculated also with Eq. (5) or an equation similar to Eq. (5) where the absolute of the product of $I_M(t)$ and $V_{DS}(t)$ was replaced by the junction temperature as a function of the transient time, $T_J(t)$.

(iv) The above steps (ii) and (iii) were repeated until the absolute iteration errors of both the temperature-dependent average power loss and average junction temperature were respectively lower than 0.1 W and 0.1 °C for all the 6 MOSFETs. Such final results presented below are referred to as the steady electro-thermal simulation results.

V. RESULTS AND DISCUSSION

A. Comparison of FE simulation and experiment

If the maximum temperatures on the MOSFETs were used as the junction temperatures, it was hard to achieve reasonable agreement between the FE simulation and the experimental results. Therefore, the junction temperatures presented in Fig. 8 were the average temperatures on the top active surface regions of the MOSFETs. As can be seen from Fig. 8 (b), (d) and (f), with the selected heat exchange coefficient applied on the cooling surface, appropriately increased specific heat of the Al-SiC composite base plate and the consideration of the voids within the Sn-Ag solder joints, the FE simulation results are in satisfactory agreement with those of the transient thermal test. Therefore, the FE thermal simulation using a proper heat exchange coefficient to simplify the interaction between the power module and the water cooler can still provide good predictions though a much more computation resource demanding co-simulation of thermal and computational fluid dynamics may provide better predictions.

Comparing Fig. 8 (a), (c) and (e) with Fig. 8 (b), (d) and (f), it can be seen that ignoring the 15% and 7% voids in the Sn-3.5Ag solder joints to attach MOSFETs M1 and M6 in the FE model, there is negligible effect on the simulation results. By contrast, ignoring the 32% voids in the Sn-3.5Ag solder joint to attach MOSFET M5, the junction temperatures of this MOSFET are underestimated about 3 °C during the early stage. These results are probably related to the resolution of the transient thermal test and relative small contribution of thermal capacitance and resistance from the Sn-Ag solder joints in the module system, which could hardly reveal the virtual effect of relatively low percentages of the voids in the Sn-3.5Ag solder joints. On the other hand, if datum provided by the supplier was taken as the specific heat of the Al-SiC base plate, the FE simulation results somewhat underestimate the junction temperatures of all the 6 MOSFETs at the transient time of 5 to 50 seconds. Thus, it is necessary to increase the specific heat of the base plate while the thermal grease and cooler are ignored for simplification.

From Fig. 8, it can be further seen that the transient thermal test did not capture the thermal response of all the MOSFETs at time of 10^{-5} to 10^{-3} s which are needed to reveal the contributions from the MOSFETs themselves and the Sn-3.5Ag solder joints to attach these MOSFETs. This agrees with what was pointed out in the existing literature: the experimental techniques exist for accurately measuring the thermal transient response of a physical device in the 100 microsecond range [37]. Therefore, in the present work, the FE simulation results from cases C1 to C6 and D1 to D6 were used to extract the R and C parameters of the compact RC thermal network model.

B. R and C parameters of the RC network model

The FE simulation results of cases C1 to C6 and D1 to D6 can be fitted to the compact RC network model described in Fig. 5 very well, and the R and C parameters extracted using the three-step curve fitting method are listed in Table III. Here the unit for the R parameters is °C/W, and the unit for the C parameters is J/°C.The extracted R and C parameters can indeed reflect the physical structure of the SiC power module which cannot be revealed using an m×m Foster network similar to the previous RC network models [15-18, 21]. For example, the values of C_{17}, C_{18}, C_{67} and C_{68} are higher than the values of C_{I7} and C_{I8} (I=2, 3, 4 and 5), and the values of R_{17}, R_{18}, R_{67} and R_{68} are higher than the values of R_{I7} and R_{I8} (I=2, 3, 4 and 5). Such a result corresponds to the fact that MOSFETs M1 and M6 at the two ends occupy more base plate and larger cooling surface than the other four MOSFETs, M2, M3, M4 and M5, as can be seen from Fig. 1. The values of R_{53}, R_{13} and R_{63} are clearly higher than those of R_{23}, R_{33} and R_{43}. This is in good agreement with 32%, 15% and 7% voids in the Sn-3.5Ag solder joints used to attach M5, M1 and M6. Under a higher heat exchange coefficient of h, the values of C_{I8} are higher, and C_{I7}, R_{I7} and R_{I8}

(I=1, 2, …, 6) are lower than the corresponding parameters under a lower heat exchange coefficient of h. This can readily be attributed to the fact that a higher h would lead to shorter heat-flow paths through the base plate and require a higher flow rate and hence more thermal mass of the water coolant. Therefore, all these results indicate that the present compact RC thermal network model can describe the structure and heat-flow paths in the SiC power module more physically meaningful.

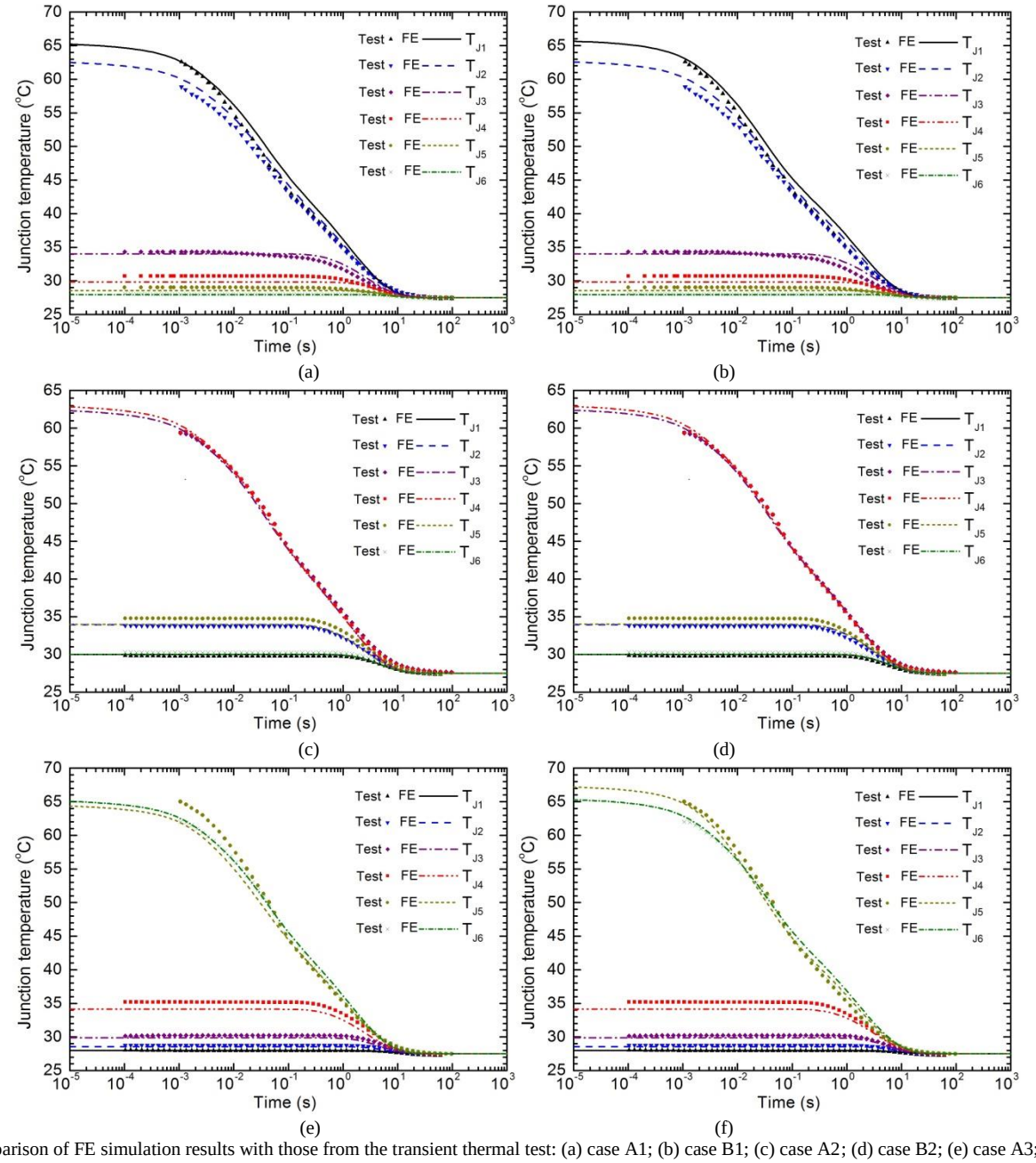


Fig. 8. Comparison of FE simulation results with those from the transient thermal test: (a) case A1; (b) case B1; (c) case A2; (d) case B2; (e) case A3; and (f) case B3.

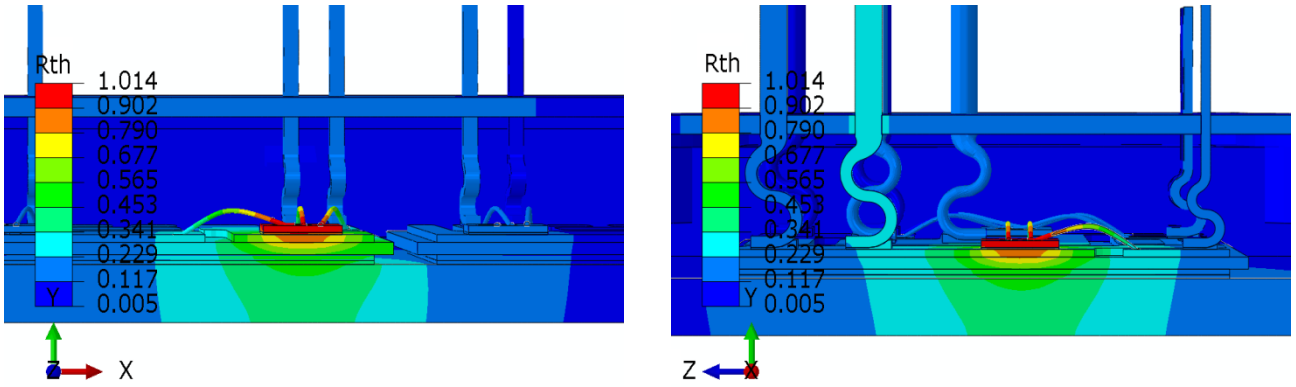
It should be noted that the Sn-3.5Ag solder joint is the second physical layer under each MOSFET while the voids in the Sn-3.5Ag solder joints mainly have effect on the values of the third-rung R_{53}, R_{13} and R_{63}. This result reveals that the rest 5-rung R and C parameters are responsible for the heat flow in the rest 6 physical layers. Therefore, the 8 physical layers are different from the 8 layers corresponding to the 8-rung R and C parameters, and the change rate of heat flow within one or a few physical layers must be larger than that at one or a few interfaces between the physical layers. A larger number of rung for each branch of the RC network would be needed to separate the contributions from all the different physical layers, as that in the structure function based on the one-dimensional Cauer RC network [25].

For all the R and C parameters listed in Table III, all the nodal temperatures predicted using the compact RC thermal network model should be either the average junction temperatures on each of the 6 SiC MOSFETs or the average temperatures within the different domains of the module. This is because as shown in Fig. 9, the temperatures (calculated from

the thermal impendence values) at any 8 locations directly under the MOSFET cannot match the predictions with the RC thermal network model. The nodal temperatures are thus the average temperatures of the domains occupied by the corresponding R and C parameters. If the nodal temperature at any point within the module is needed to predict, additional branches of the basic Cauer RC network with lateral resistors and certain pairs of R and C parameters to be inserted before and after this node would be required to ensure that the heat flow passing through this node is the true heat flow, rather than the average heat flow. Nevertheless, the temperature-dependent R and C parameters can still be incorporated into the present compact RC network model, and this will be our future work.

TABLE III
THE R AND C PARAMETERS EXTRACTED FOR THE AVERAGE JUNCTION THERMAL IMPENDENCE OF THE MOSEFETS

		C_{I1}	C_{I2}	C_{I3}	C_{I4}	C_{I5}	C_{I6}	C_{I7}	C_{I8}	$\sum C_{IJ}$	R_{I1}	R_{I2}	R_{I3}	R_{I4}	R_{I5}	R_{I6}	R_{I7}	R_{I8}	$\sum R_{IJ}$
h=2750W·m^{-2}·K^{-1}	I=1	0.0012	0.0052	0.0101	0.059	0.249	0.014	2.505	24.51	27.35	0.0114	0.0338	0.195	0.252	0.132	0.046	0.301	0.183	1.153
	I=2	0.0012	0.0052	0.0103	0.057	0.243	0.011	2.319	15.93	18.58	0.0113	0.0337	0.169	0.250	0.150	0.036	0.463	0.281	1.394
	I=3	0.0012	0.0052	0.0103	0.060	0.282	0.011	2.306	15.93	18.61	0.0114	0.0338	0.168	0.268	0.116	0.046	0.463	0.281	1.388
	I=4	0.0012	0.0052	0.0104	0.060	0.284	0.017	2.263	15.93	18.57	0.0113	0.0337	0.167	0.272	0.117	0.046	0.463	0.281	1.392
	I=5	0.0012	0.0051	0.0099	0.055	0.268	0.012	2.303	15.93	18.58	0.0113	0.0330	0.299	0.268	0.130	0.045	0.463	0.281	1.530
	I=6	0.0012	0.0052	0.0102	0.060	0.261	0.011	2.409	24.49	27.25	0.0114	0.0338	0.180	0.264	0.139	0.030	0.301	0.183	1.142
	R_{124}	R_{125}	R_{126}	R_{127}	R_{128}	R_{237}	R_{238}	R_{344}	R_{345}	R_{346}	R_{347}	R_{348}	R_{457}	R_{458}	R_{564}	R_{565}	R_{566}	R_{567}	R_{568}
	3020	26.54	12.54	0.855	46.10	0.682	0.000	1818	15.93	7.529	0.990	76.83	0.676	0.000	3031	26.55	12.53	0.858	64.42
h=5500W·m^{-2}·K^{-1}		C_{I1}	C_{I2}	C_{I3}	C_{I4}	C_{I5}	C_{I6}	C_{I7}	C_{I8}	$\sum C_{IJ=1\ to\ 8}$	R_{I1}	R_{I2}	R_{I3}	R_{I4}	R_{I5}	R_{I6}	R_{I7}	R_{I8}	$\sum R_{IJ=1\ to\ 8}$
	I=1	0.0012	0.0049	0.0101	0.058	0.320	0.0074	2.412	34.05	36.86	0.0109	0.0313	0.192	0.271	0.128	0.046	0.235	0.080	0.993
	I=2	0.0012	0.0049	0.0102	0.055	0.241	0.0094	2.086	22.13	24.54	0.0109	0.0314	0.167	0.252	0.135	0.050	0.361	0.122	1.128
	I=3	0.0012	0.0049	0.0102	0.056	0.243	0.0074	2.043	22.13	24.50	0.0109	0.0315	0.165	0.256	0.122	0.048	0.361	0.122	1.117
	I=4	0.0012	0.0049	0.0102	0.057	0.254	0.0074	1.999	22.15	24.48	0.0109	0.0314	0.165	0.264	0.114	0.053	0.361	0.122	1.122
	I=5	0.0012	0.0049	0.0099	0.050	0.243	0.0114	2.110	22.15	24.58	0.0109	0.031	0.293	0.259	0.117	0.070	0.361	0.122	1.264
	I=6	0.0012	0.0049	0.0101	0.055	0.273	0.0074	2.471	33.11	35.93	0.0109	0.0313	0.177	0.257	0.140	0.053	0.235	0.080	0.983
	R_{124}	R_{125}	R_{126}	R_{127}	R_{128}	R_{237}	R_{238}	R_{344}	R_{345}	R_{346}	R_{347}	R_{348}	R_{457}	R_{458}	R_{564}	R_{565}	R_{566}	R_{567}	R_{568}
	6872	22.09	11.58	0.991	161.1	0.746	0.000	7312	14.54	11.05	1.239	198.6	0.740	0.000	11447	24.23	10.84	1.017	154.9



(a) (b)

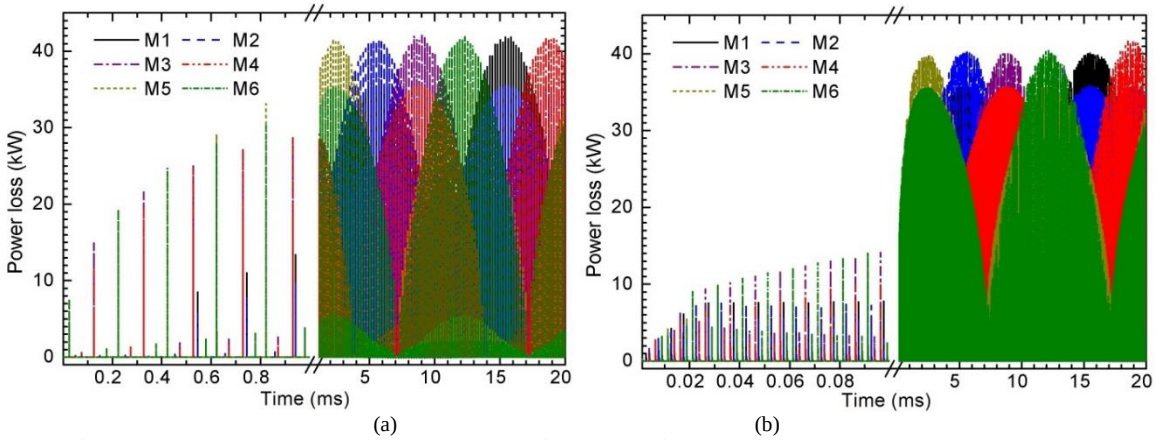
Fig. 9. The FE simulated distribution of the thermal impedance, R_{th}, surrounding MOSFET M2 for case C2 approaching the steady state: (a) X-Y cross-sectional view; and (b) Y-Z cross-sectional view.

Due to the existence of the lateral resistors, the sum of the 8 R parameters, $\sum R_{IJ}$ listed in Table III, for each of the 6 basic Cauer RC networks is actually larger than the total thermal resistance for the self-heating effect of the corresponding MOSFET. However, if all the 6 SiC MOSFETs generate similar amount of heat, the heat flow passing through the lateral resistors should be negligible. The values of $\sum R_{IJ}$ can hence be used to calculate the worst rises of the average junction temperatures. For example, the SiC power module were tested to have the following worst power loss: 95% efficiency for 6 kW output power at switching frequency of 100 kHz [1]. This corresponds to 50 W heat generation from each of the 6 SiC

MOSFETs. With the maximum $\sum R_{5J}$, 1.530 °C/W under h=2750W·m^{-2}·K^{-1}, in Table III, a maximum rise of average junction temperature of 76.5 °C above the ambient is predicted. The maximum average junction temperature would be 104 °C if the ambient temperature is 27.5 °C as in the transient thermal test. Additional FE simulation reveals that the maximum temperature is only a few degrees higher than the average junction temperature for the SiC MOSFET under a heat generation of 50 W. Under the cooling condition of h=2750W·m^{-2}·K^{-1}, the designed SiC power module can hence be operated at the maximum junction temperature below 125 °C to meet the thermal specification.

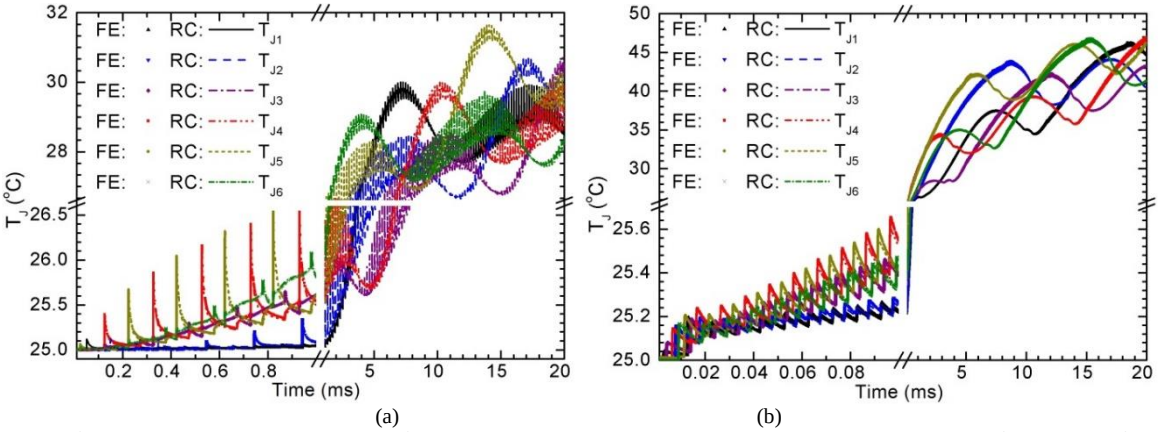
C. Evaluation of the compact RC network model

Figures 10 and 11 present the power losses and the junction temperatures of the 6 MOSFETs simulated using the LTspice model and the FE model. As aforementioned, the high instantaneous turn-on power losses of the 6 MOSFETs and hence the fluctuations about 1 °C for the junction temperatures during each switching cycle were due to the inclusion of the artificial switching losses of the body diodes. The current comparison between the LTspice and FE simulation results is concerned with the validity of the compact RC network model to calculate the electro-thermal response of the SiC module during the realistic operating conditions. The two switching frequencies of 5 kHz and 100 kHz were the two operating extrema of the designed SiC module. The electro-thermal simulation to deal with the power losses of the 6 MOSFETs shown in Fig. 10 would be more challenging than that to deal with those removing the artificial switching losses of the body diodes. The FE method has widely been demonstrated in the ability to predict the electro-thermal response of power modules, and the present FE model has experimentally been calibrated. As can be seen from Fig. 11, the junction temperatures of the 6 MOSFETs simulated using the LTspice model and FE model are in excellent agreement with each other. Therefore, these results demonstrate that the compact RC network model is valid and can be used to rapidly simulate the electro-thermal response of the SiC module under the realistic operating conditions.



(a) (b)

Fig. 10.Power losses of the 6 MOSFETs simulated using the LTspice model for switching frequencies: (a) 5 kHz, case E1; and (b) 100 kHz, case E2.



(a) (b)

Fig. 11.Comparison of the transient junction temperatures of the 6 MOSFETs simulated using the LTspice model and FE model for switching frequencies: (a) 5 kHz, case E1; and (b) 100 kHz, case E2.

D. Electro-thermal simulation with the RC network model

The results presented below have removed the effect of the artificial switching losses of the body diodes in the LTspice model. As presented in Fig. 12(a), the average power losses of the 6 MOSFETs increased almost linearly with increasing the switching frequency. Taking into account of the effect of the temperature, they were slightly (01 to 0.2 W) different among the MOSFETs, and in the order of M5 > M2, M3 and M4 > M1 and M6. They were all approximately 5% higher than the predictions ignoring the effect of the temperature. This can simply be attributed to the conducting losses of the MOSFETs

which were higher at higher temperatures [38]. The efficiency of the SiC power module was also estimated with the total average power losses of the 6 MOSFETs and the total average output powers of the three phases. The result is presented in Fig. 12(b), and compared with the experimental result which was reported in the previous publications [1, 2]. The estimated efficiencies of 1.2% to 2.1% higher can be ascribed to the following two facts. On the one hand, the junction temperatures of the MOSFETs in the previous test should be higher than those in the present predictions because it was carried on an air-based heat sink, while the present models has been developed on a water-based cooler. On the other hand, the present simulation ignored the contributions of power losses from all the connectors, cables and DC link capacitors.

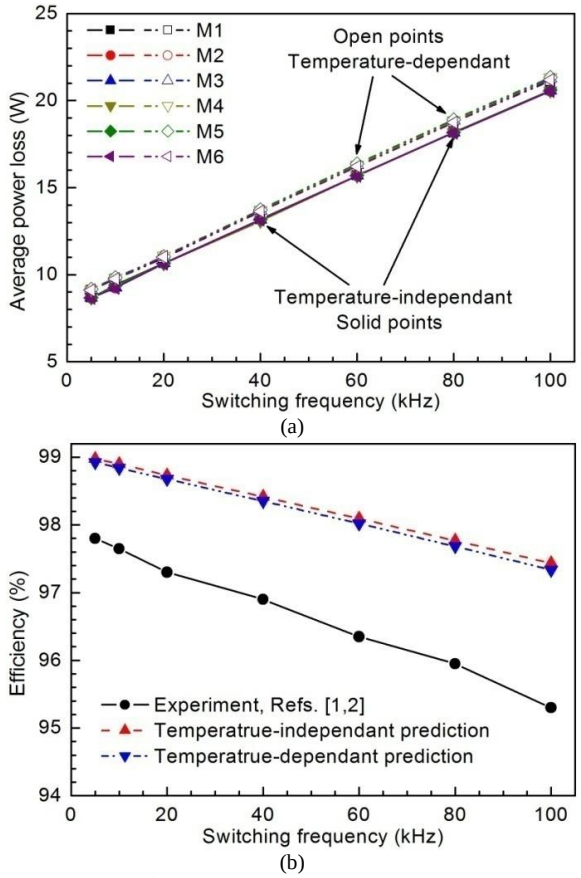


Fig. 12. Comparison of the steady simulation results using the LTspice models with (temperature-dependant) and without (temperature-independant) the RC network model: (a) average power losses of the 6 MOSFETs; and (b) efficiency of the three phase, two level power module.

As can be seen from Fig. 11(b) and Fig. 13(a), after removing the artificial switching losses of the body diodes in the LTspice model, both the fluctuations of the junction temperatures during each switching cycle and the rises of the junction temperatures during the early transient stage were significantly reduced. Fig. 13(b) presents one example of the simulated steady "sinusoidal-like" evolutions of the junction temperatures of MOSFETs M5 and M6 during two fundamental output cycles. Fig. 14 further presents the average junction temperatures and swinging amplitudes of the junction temperatures of the 6 MOSFETs during each fundamental output cycle. Both the average junction temperatures and their swinging amplitudes appeared to increase linearly with increasing the switching frequency. The average junction temperatures of MOSFET M5 were 1 to 2 °C higher than those of MOSFETs M2, M3 and M4, while the latter were 1 °C to 3 °C higher than those of MOSFETs M1 and M6. These average junction temperatures together with their swinging amplitudes would predict the lifetimes of the Al wire bonds on MOSFET M5 would probably half of those of Al wire bonds on MOSFETs M1 and M6 [39]. Therefore, the porous Sn-3.5Ag solder joint to attach M5 causing higher junction temperatures should be avoided during the assembling process.

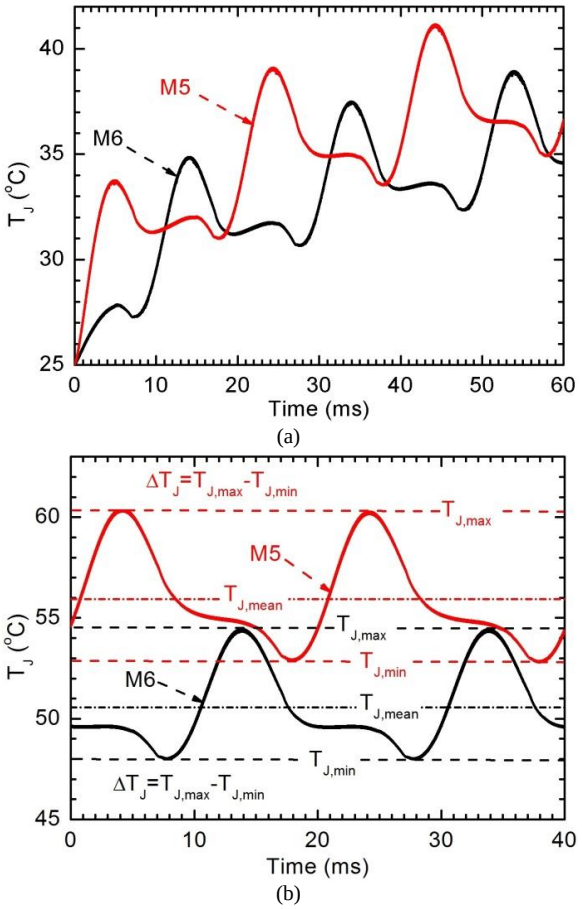


Fig. 13. The junction temperatures of MOSFETs M5 and M6 under switching frequency of 100 kHz, simulated using the LTspice models integrating the RC network model: (a) three fundamental output cycles of the initially transient state; and (b) two fundamental output cycles of the steady state.

For the switching frequencies of 5 kHz to 100 kHz, the swinging amplitudes of the junction temperatures of MOSFET M5 were 0.4 °C to 1.6 °C higher than those of the other 5 MOSFETs. Excluding M5, the "sinusoidal-like" swinging amplitudes of the junction temperatures of the other 5 MOSFETs during each fundamental output cycle were all in the range of 3.7 °C to and 6.4 °C. They are actually better than the swinging amplitude approximately of 7 °C which was predicted for the 50 Hz fundamental frequency related short-term thermal behavior of a Si IGBT-based wind power converter with switching frequency of 1950 Hz in the existing literature [40]. This result, together with the 95% to 98% efficiencies of the same SiC power module under the different switching

frequencies which were tested in the previous publication [1], indicate that even under higher switching frequencies, the presently designed and developed much more compact and lighter SiC power module can achieve the thermal performance better than or similar to the conventional Si IGBT power modules.

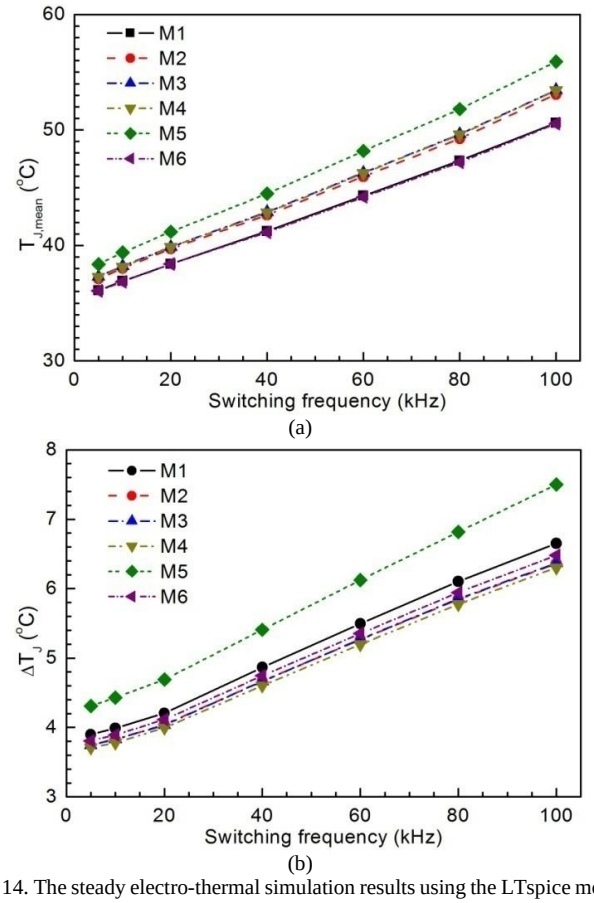


Fig. 14. The steady electro-thermal simulation results using the LTspice models integrating the RC network model: (a) average junction temperatures; and (b) swinging amplitudes of the junction temperatures of the 6 MOSFETs during each fundamental output cycle.

VI. CONCLUSIONS

Based on the above results and discussion of the transient thermal test, FE and compact RC network simulations for the lightweight three-phase half bridge, two-level SiC power module, the following conclusions are drawn:

The junction temperatures of the 6 SiC MOSFETs in three groups of transient thermal test were measured using the forward voltages of the body diodes as the temperature sensitive parameters. Through matching the FE simulation results with the experimental measurements, a constant heat exchange coefficient in the FE model was determined and used to describe the cooling condition of the module mounted on a water cooler. To achieve satisfactory agreement with the measurements, the junction temperatures are expressed as the average values of the temperatures on the top active surface regions of the MOSFETs.

By increasing the specific heat of the Al-SiC base plate appropriately, this can improve the FE prediction accuracy for the junction temperatures at the transient time range of 5 to 50 seconds. On the other hand, of the 7%, 15% and 32% voids in the Sn-3.5Ag solder joints to attach the MOSFETs, only the effect of the 32% voids on the junction temperatures can virtually be observed. This result is probably related to the resolution of the transient thermal test and relative small contribution of thermal capacitance and resistance from the Sn-Ag solder joints in the module system.

A compact RC thermal network model consisting of 115 R and C parameters to predict the transient junction temperatures of the 6 MOSFETS were constructed, where cross-heating effects between the MOSFETs are represented with lateral thermal resistors.The R and C values of the network model can be extracted from the FE simulation results of 6 transient simulation cases. A three-step curve fitting method was especially developed to extract the R and C parameters using an office desktop computer, for a total running time within 15 minutes.

The compact RC network model can physically be correlated withthe structure and heat-flow paths in the power module, as reflected by R and C parameters which were closely associated with the percentages of voids in the Sn-3.5Ag solder joints, volumes of the Al-SiC base plate and the cooling surfaces shared by each of the 6 MOSFETs. However, due to compact nature, all the nodal temperatures predicted using the RC thermal network model should be taken as either the average junction temperatures on each of the MOSFETs or the average temperatures within the different domains of the module.

Comparison with further FE simulation results demonstrates that the compact RC network model can be used to rapidly simulate the electro-thermal response of the SiC module under the realistic switching conditions. The simulation results from a few additional trial, together with the previously reported 95% to 98% efficiencies of the same SiC power module under the different switching frequencies, indicate that even under higher switching frequencies, the presently designed and developed much more compact and lighter SiC power module can achieve the thermal performance better than or similar to the conventional Si IGBT power modules.

The present work demonstrates that the up to date computation capacity and commercially available design tools can be employed to effectively design new power modules. The design tools used in the present work include a FE software Abaqus for thermal modelling and simulation, a FE software Maxwell for electro-magnetic modelling and simulation, a numerical programming software Matlab for developing the three-step curve fitting method and a circuit simulation software LTspice for the electrical and electro-thermal simulation. The experimental evaluation and calibration were used to improve the accuracy of the simulation results.

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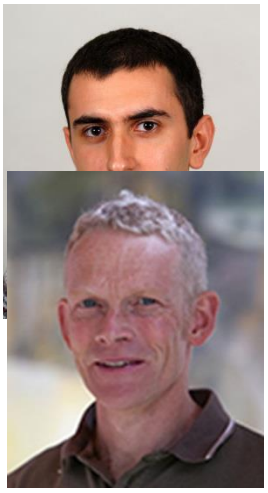

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