Digital Dead-Beat and Repetitive Combined Control for Stand-Alone Four-Leg VSI

Alessandro Lidozzi, Luca Solero, Fabio Crescimbini
Department of Engineering
Roma Tre University, Roma, Italy
C-PED, Center for Power Electronics and Drives
email: alessandro.lidozzi@uniroma3.it

Chao Ji, Pericle Zanchetta
Dept. of Electrical and Electronic Engineering
University of Nottingham, UK
email: pericle.zanchetta@nottingham.ac.uk

Abstract –**This paper deals with a newly conceived combine control topology. Dead-Beat and Repetitive controllers are proposed to operate jointly in 4-leg VSI for stand-alone applications. In such mode of operation, dedicated controller has to regulate the inverter output voltages, which are measured at the output of the power filter. Each control topology exhibits some specific features. Dead-Beat can rapidly compensate output voltage variations due to load changes; on the contrary, Repetitive Control can provide the required harmonic compensation capabilities that are mandatory to comply with the Standards, when balanced and unbalanced non-linear loads have to be fed.**

I. Introduction

The reduction of the harmonic content of current and voltage waveforms at the output of power electronic converters is of increasing interest for today's applications, with particular reference to either Distributed Generation Systems or Uninterruptible Power Supplies or active filtering, which have to comply with severe Standards. The European Standards EN-50160 and EMC EN-61000 address the power quality limits that the utilities must satisfy; however, even if the European Union has its own regulation, each country can demand for mandatory requirements that are more restrictive. In case of main grid connected utilities, the EN-50160 considers the voltage Total Harmonic Distortion (THD_V) up to the 25^{th} harmonic with respect to the fundamental component. On the other hand, when stand-alone power generation systems are considered, the reference Standard for Uninterruptable Power Supply (UPS) equipment is the IEC 62040-3, which designates that, under specific linear and non-linear load conditions, the harmonic content of the output voltages should be within the IEC 61000-2-2 limits.

The application, to which the investigated combined control strategy addresses, relates to a 3-phase 4-wire power supply unit for AC stand-alone loads, which is formed by a 4-leg VSI and its dedicated output power filter. The conceived unit and its control have to be able to support a 3ph+n isolated grid in order to provide power supply to linear and non-linear loads, with either leading or lagging power factor. With reference to the control aspects, this paper deals with a combined Dead-Beat and Repetitive controller (DB-RC) devoted to VSI output voltages regulation. Proposed parallel combination of Dead-Beat and Repetitive Control acts to fully exploit the benefit obtainable by each control structure when considered separately.

In this work, the Dead-Beat controller is designed to provide fast dynamic response during the system start-up or large load step changes, while the parallel type repetitive controller is employed to cope with the model uncertainties and load variations and hence to achieve a high performance in the steady state. A three-phase four-leg inverter prototype is utilized to verify the effectiveness of the proposed dead-bead and repetitive combined control algorithm.

Detailed description of the combined DB-RC structure is provided. Experimental campaign has been conducted to highlight the combined action and to prove the benefits of the proposed control structure.

Classical Dead-Beat (DB) control was applied to single-phase stand-alone VSI in [1] highlighting its fast response to load variations. DB control is improved with prediction features in [2] where it was applied to DC-DC converters. Predictions capabilities of the Dead-Beat regulation are illustrated also in [3] for AC-DC systems in grid-tied operation.

On the other hand, Repetitive Control (RC) has been proved to the very effective to adjust periodic signals as disturbance harmonics [4]–[7]. Main drawback of the RC is represented by its inherent learning time, which reduces the overall dynamic performance, resulting in some cases in unacceptable compensation of load changes.

II. Converter Topology and System Description

In the last decade, many researchers of both industry and academia have addressed their studies to inverter and filter topologies for either grid-connected or stand-alone systems. In stand-alone configurations, topologies with neutral wire at the inverter power output become critical when extremely general-purpose loads require to be supplied. Many different types of load can be located in autonomous grids; as a result, the single-phase, multi-phase, linear and non-linear loads affect considerably the neutral wire current, which can be of significant amplitude as well quite distorted. Additional power losses and resonance phenomena can occur and result in faults in protection devices and electrical safety circuits. With reference to DC-AC conversion, two main topologies of power electronic converters with neutral wire are present in literature, the 3-phase 4-wire inverters with split DC bus capacitors and the 3-phase 4-leg inverters.

The 3-phase 4-leg inverter configuration makes use of an additional leg with respect to the conventional 3-phase topology as it is shown in Figure 1. The additional leg requires 2 more switches and power diodes as well extra driving circuits and higher complexity in modulation techniques and control strategies. In spite of this, the 4-leg inverter, when properly modulated, can assure the efficient regulation of the output phase voltage also in case of unbalanced and distorted loads. Modulation with injection of the 3rd harmonic as well SVM techniques are possible without affecting the harmonic content in the phase-to-neutral voltage; further, the neutral current flows through the added leg and no oversizing is required for the DC-link capacitors. Prototypal realization of a 3-phase 4-leg inverter as shown in Figure 2 is used to experimentally investigate the DB-RC combined control. The prototype characteristics are listed in Table I.

Power inverter is modeled through its first order approximation, which is very simple to manage. The inverter is seen, from the control algorithm, mainly as a gain with a delay due to the discretization caused by the PWM unit as it is shown in (1), where K_m is the gain depending to the modulation strategy, V_{dc} and F_{sw} are respectively the DC-link voltage and the inverter switching frequency. Acquired phase voltages are filtered by means of a second order low-pass Butterworth filter having the transfer function as in (2), where ω_f is the filter cut-off frequency.

TABLE I - 3-PHASE 4-LEG INVERTER PROTOTYPE MAIN CHARACTERISTICS

Rated Power	40 kVA
Line-to-Line Voltage	400±10% V
Switching Frequency	12 kHz
Efficiency @ rated power (output filter included)	0.97
Power Modules	Semikron - SEMIX303GB12Vs
DC-Link Capacitors	MKP 3 x 150uF – 900Vdc
AC Output Inductors	800 uH
AC Output Main Capacitors	MKP 5 uF – 480Vac
Control Board	TI-TMS320F28335

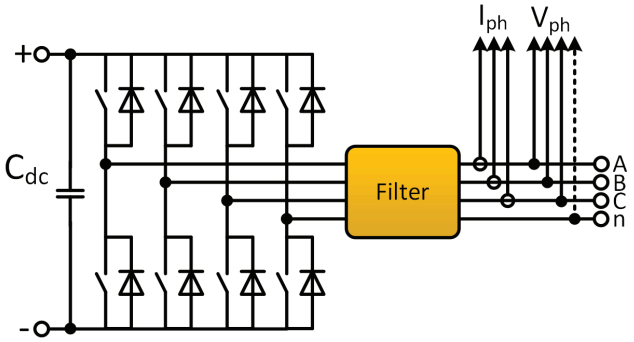

Figure 1. 3-Phase 4-Leg Inverter.

$$G_{4-leg}(s) = \frac{K_m V_{dc}}{1 + \frac{s}{2\pi F_{sw}}} \tag{1}$$

$$G_{lpf}(s) = \left(\frac{\omega^2{}_f}{s^2 + \sqrt{2}\omega_f s + \omega^2{}_f} \right) \tag{2}$$

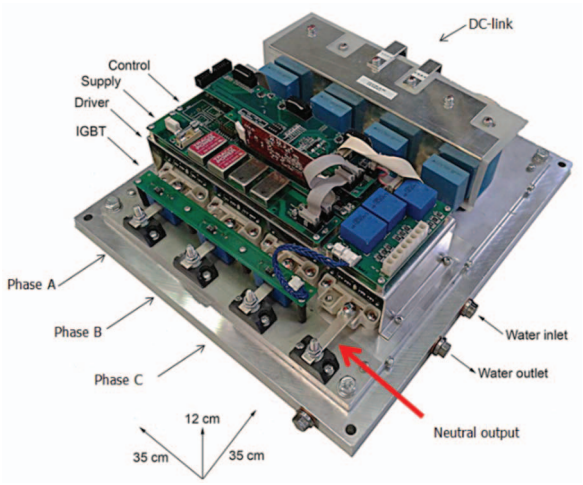

Figure 2. 3-Phase 4-Leg Inverter Prototype.

Inverter output filters are necessary to remove the switching components from the output voltages and currents. In the present study, it is considered the single-phase equivalent filter structure as shown in Figure 3, where the conventional LC second order main filter is connected to two tuned RLC branches: the trap-filter and the selective damper [8]. The selective damper is centered at the frequency of about 20% higher than the LC resonance frequency in order to damp the LC resonance peak, making the R_d resistor visible to the rest of the circuit only in a restricted range of frequencies. The trap-filter is instead tuned to resonate at the switching frequency (R_t is the sum of L_t and C_t ESRs), in order to short-circuit the switching fundamental component. Filter transfer function can be simply achieved considering the impedance of each part of the filter in the s-domain as in (3) without the load connected at the filter output.

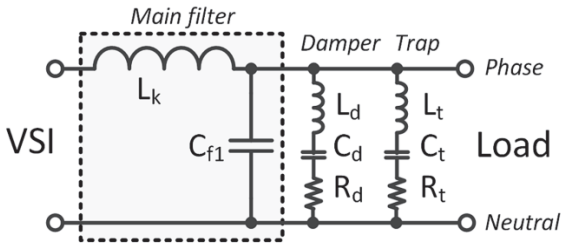

Figure 3. Scheme of the considered output power filter.

$$Z_{trap}(s) = sL_t + \frac{1}{sC_t} + R_t\,,\ Z_{dump}(s) = sL_d + \frac{1}{sC_d} + R_d\,,$$

$$G_{pwf}(s) = \frac{Z_{dump}(s)//Z_{trap}(s)//\frac{1}{sC_{f1}}}{sL_k + \left(Z_{dump}(s)//Z_{trap}(s)//\frac{1}{sC_{f1}} \right)} \tag{3}$$

III. DEAD-BEAT + REPETITIVE COMBINED CONTROL STRATEGY

For the proposed four-leg VSI system, the fourth leg is utilized to provide a neutral connection, and it is modulated without direct voltage regulation as suggested in [9]. Hence,

from the control point of view, the three-phase system can be de-coupled and each phase can be considered separately as a standard single-phase inverter. As a result, individual digital control loop can be applied to regulate the three phase-to-neutral voltages.

A. Previous Control Strategies

Several control strategies have been investigated in the previous works for the output voltage regulation of the considered 4-leg inverter. In [10], a multi-resonant control approach was first proposed. It ensures a great flexibility of tuning gain and phase of each resonant controller at voltage harmonic points, though the hardware implementation and computing requirement was an issue. In order to overcome that, a resonant + repetitive solution was developed [11]. The effort of the resonant controller was to provide the fundamental component tracking, and the use of the plug-in type repetitive controller was to compensate for all the harmonics. In spite of the fast dynamic performance and wide stability range, the high order harmonic compensation capability of the VSI system under non-linear load condition was compromised to some extent, mainly due to the filtering effort of the fundamental resonant controller. By considering the system is internally stable, [12] demonstrated the direct repetitive control method, in order to further improve the output voltage quality. With the proposed load adaptive algorithm and the dedicated zero-phase-shift compensator for different load rating, the system was capable of providing an excellent output voltage even under highly non-linear load condition. However, the nature of the direct type repetitive control implies that an empty control cycle, i.e. no control action, is always required during the converter start-up, due to the absence of the conventional controller. In addition, an open loop control cycle is needed when a large load step change applies. This is potentially dangerous for critical electrical installations such as health care facilities, as the system stability cannot be assured during the open loop cycle.

B. Proposed DB + Parallel RC

Taking all the aforementioned limitation into account, a novel parallel type dead-beat (DB) + repetitive (RC) control strategy is proposed in this work for the system output voltage regulation. Figure 4 shows a generalized control block diagram of each phase, where $G_{4\text{-}leg}(s)$, $G_{pwf}(s)$ and $G_{lpf}(s)$ represent the 4-leg VSI, the power filter, and the measurement low pass filter, respectively as given in (1), (2) and (3). A parallel type Repetitive Controller is employed in combination of a Dead-Beat controller to achieve both a fast transient regulation and high order harmonic compensation in steady state.

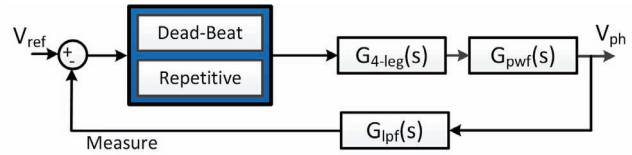

Figure 4. Generalized control block diagram of each phase.

Owing to its high control bandwidth feature, Dead-Beat control has been considered widely for digital implementations demanding fast dynamic response. For linear time-invariant (LTI) systems, it is capable of finding an actuating signal to bring the output to the steady state in the smallest number of time steps. The main drawback of the Dead-Beat controller is the high sensitivity to model uncertainties, parameter mismatches, and measurement noises. Since it is based on pole-zero cancellation, a good knowledge of the target plant is required. Otherwise, the control performance is strongly reduced in presence of unpredicted disturbances such as dead-times, as there is no inherent integral action involved [13].

Repetitive control attracts more and more interests in modern industrial applications for feedback systems that are subject to periodic reference inputs or periodic disturbances. Based on the internal model principle (IMP) [14], the repetitive controller processes the error signal of the previous period and applies the resultant signal to improve the control performance of the current cycle. Theoretically, with a suitably designed repetitive controller, the output of a stable feedback system can track the periodic reference signal or/and reject the exogenous periodic disturbance with zero steady state error even in the presence of model uncertainties.

In this work, the Dead-Beat controller is designed to provide fast dynamic response during the system start-up or large load step changes, while the parallel type repetitive controller is employed to cope with the model uncertainties and load variations and hence to achieve a high performance in the steady state.

C. Design Discussion

1) Dead-Beat Control Design

Considering a nominated 3 kW linear load per phase and one-unit delay (1/z) representing hardware sampling and modulation time, the system plant for the dead-beat controller can be obtained. Since a wide load range operation is preferred, the plant is expanded and analyzed in the discretized domain, and the corresponding pole-zero map can be evaluated as shown in Figure 5.

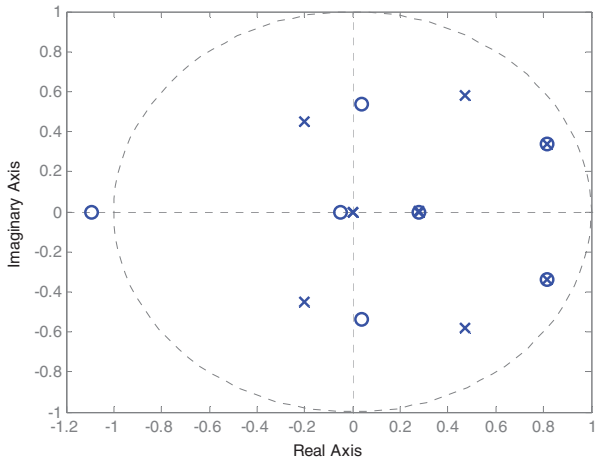

Figure 5. Pole-zero map of the original system plant with 3 kW linear load per phase.

Clearly, one pole pair of 0.82±0.34i and one pole of 0.28 are completely cancelled by associated zeros. Thereby, their influence can be neglected during the control design procedure. Also, the pole pair of -0.2±0.45i and the zero pair of 0.04±0.57i are located both at high frequency band and are close to each other. Hence, their effects can be ignored as well. By considering only the remaining low frequency dominant poles and zeros, a simplified system plant can be obtained. As shown in Figure 6, the step response of the simplified plant is very close to that of the original system.

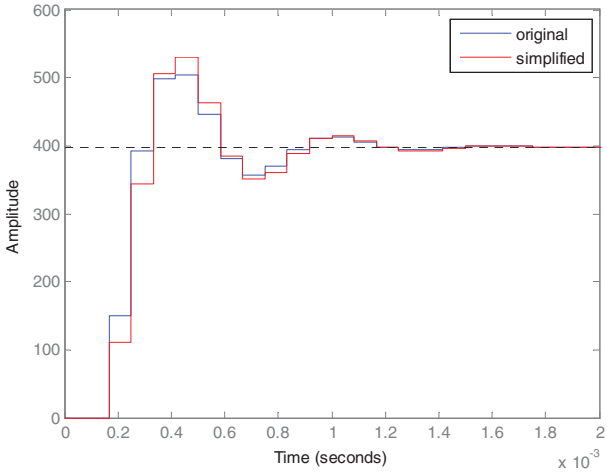

Figure 6. Step response comparison of the original plant and simplified plant.

For the dead-beat control design, the simplified plant transfer function is applied, due to the following considerations: first, it leads to a simple Dead-Beat controller structure for easy hardware implementation; second, the relatively straightforward dead-beat control loop relieves the complexity of the following repetitive control design; third, it avoids introducing the high frequency poles and zeros of the dead-beat controller, which makes the whole control system less sensitive to the load variations during transient performance. The complete dead-beat controller is expressed as in (4).

$$G_{DBC}(z)=\frac{z^4-0.94z^3+0.56z^2-0.001z}{233z^4+11.2z^3-111.3z^2-127.1z+5.84} \quad (4)$$

2) Parallel RC Design

Figure 7 shows the detailed structure of the parallel repetitive controller, where k_{RC} is the repetitive learning gain, z^{-N} is the delay line, $Q(z)$ is the robustness filter, and $G_f(z)$ is the stability filter. N is the ratio between the period time of the reference and the digital sampling time. The use of the robustness filter $Q(z)$ is to modify the internal model, which effectively increases the system stability margin.

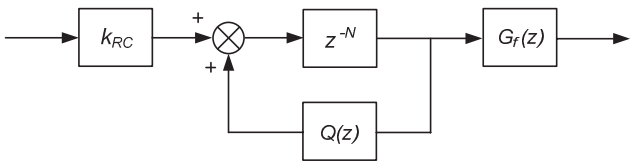

Figure 7. Detailed structure of the parallel repetitive controller.

Considering the wide load range operation, a moving average filter of $0.25z^2+0.5z+0.25/z$ has been selected in this work, in order to improve the whole system stability at high frequency band. The design of k_{RC} and $G_f(z)$ is coupled and is also correlated with the selection of $Q(z)$.

According to the small gain theorem [14], two sufficient stability conditions for the parallel RC system can be summarized as follows: (a) the control system (without the parallel RC) is inherently stable; (b) equation (4) is guaranteed for all the frequencies below the Nyquist frequency ω_{nyq}, where G_P is the system plant transfer function.

$$\left|Q(e^{j\omega T_S})-\frac{k_{RC}\,G_f(e^{j\omega T_S})G_P(e^{j\omega T_S})}{1+G_{DBC}(e^{j\omega T_S})G_P(e^{j\omega T_S})}\right|<1 \quad (5)$$

The first condition can be guaranteed, as the Dead-Beat controller has been properly designed. The second one can be proved by examining the Nyquist locus curve of equation (5). A ninth order low pass filter is proposed, based on the design approach discussed in [12], as stability filter G_f, in order to ensure equation (5) is always guaranteed for the whole operating range of the VSI inverter system.

Figure 8 shows the Nyquist locus curve of equation (5) with $G_f(z)$ implemented under 3 kW linear load condition. Clearly, the magnitude stays within in the unitary circle, which proves that the overall control system is adequately stable.

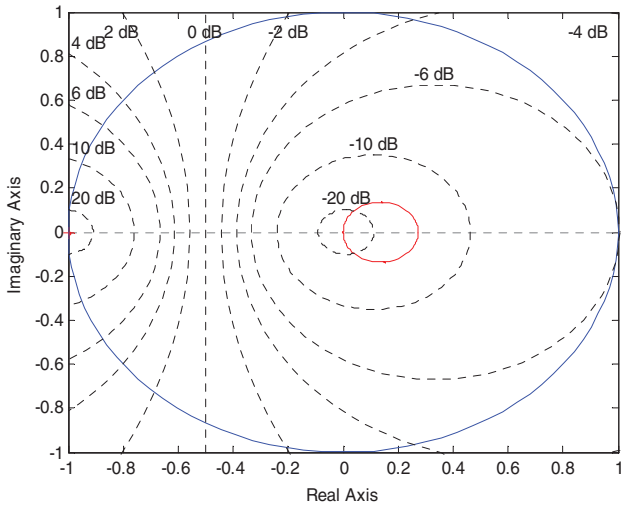

Figure 8. Nyquist locus curve of equation (5) with $G_f(z)$ and k_{RC} of 0.2 under 3 kW linear load condition for RC stability verification.

Table II summarizes the design result of the repetitive controller.

TABLE II - REPETITIVE CONTROLLER DESIGN RESULT

Symbol	Description	Value
N	Delay chain	240
k_{RC}	Repetitive learning gain	0.2
$Q(z)$	Robustness filter	$0.25z^2+0.5z+0.25/z$

IV. SIMULATION AND EXPERIMENTAL RESULTS

Figure 9 shows the voltage reference and the output voltage of Phase A during the system start-up, when a 3 kW linear load is applied on each phase. As it can be seen, a very good

tracking is achieved, due to the effort of the designed dead-beat

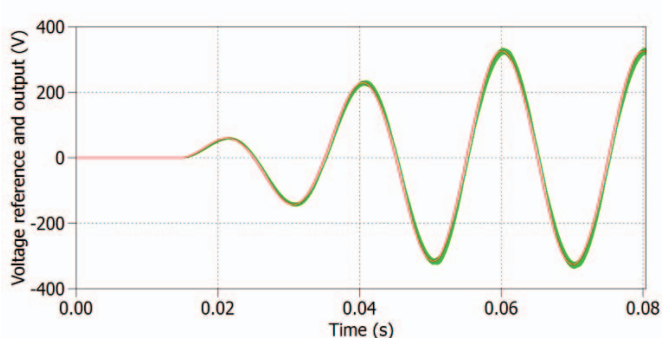

Figure 9. Voltage reference and output voltage of Phase A during system start-up, with 3 kW linear load per phase.

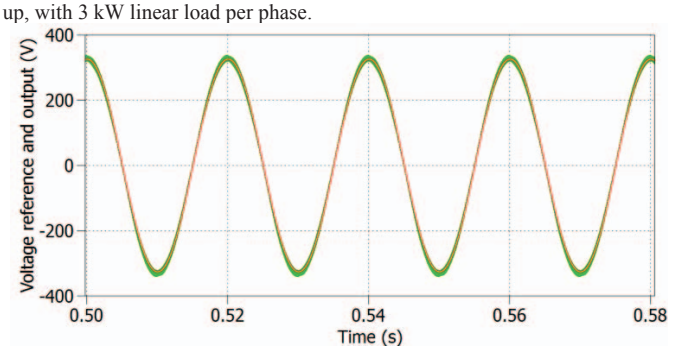

Figure 11. Voltage reference and output voltage of Phase A in steady state, with 3 kW linear load per phase.

controller, though a slight delay, which is approximately equal to two sampling delays, can be observed between the voltage reference (red trace) and the output voltage (green trace). At the time point of 0.1 s, the parallel type repetitive controller has been enabled. As shown in Figure 10, the periodic error signal starts to converge very quickly to a very small level (less than 1 V), and whole system is firmly stable. Figure 11 presents the voltage reference and the output voltage of Phase A in the steady state mode of operation. A large load step change test is then applied to examine the system control performance.

At the time point of 1 s, the load is changed from 3 kW to 6 kW. Figure 12 highlights the corresponding three-phase output voltage. It can be noted that the system is firmly stable and the error converges quickly for the large load step change.

Inverter prototype shown in Figure 2 has been used in the experimental campaign to validate the illustrated control strategy. Proposed DB-RC has been implemented on the TMS320F28335 DSP from Texas Instruments, which is assembled on a dedicated board. Single-precision 32-bit floating-point numeric representation has been used for both the Dead-Beat and the Repetitive controls.

At first, DB-RC is tested in the no-load condition to demonstrate the correct operation being the inverter output filter response completely undamped. Phase voltages and currents are highlighted in Figure 13 where a good regulation is obtained. Additionally, a 3-phase linear balanced load test has been performed where each phase was loaded by 4 kW resistive rack. It can be noticed from Figure 14 that the load-side voltages exhibit a very low THD with negligible dead-time distortion.

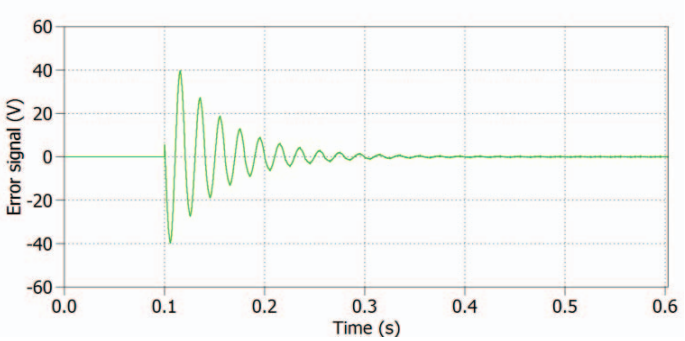

Figure 10. Voltage error signal of Phase A seen by the repetitive controller.

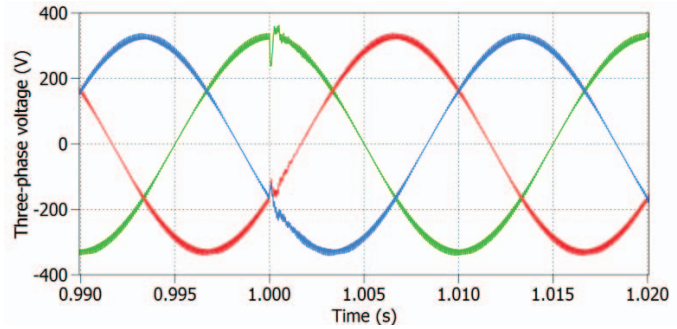

Figure 12. Three-phase output voltage during load step change, from 3 kW to 6 kW occurring at 1 s.

Steady-state control behavior is shown also when non-linear loads have to be fed. Non-linear load configuration is illustrated in Figure 15. In the case shown in Figure 16 a single-phase diode rectifier is connected to the output of the VSI power filter. Phases B and C are at no-load condition. It can be recognized the very low voltage distortion that is achieved mainly thanks to the Repetitive part of the proposed controller. A similar test has been performed using a single-phase non-linear load, which was directly connected between phase A and the neutral wire. Results are shown in Figure 17, where the validity of the proposed controller can be documented looking to the V_{an} and V_{bn} voltages. Also in this case, voltage drop is within the maximum allowed by the standard.

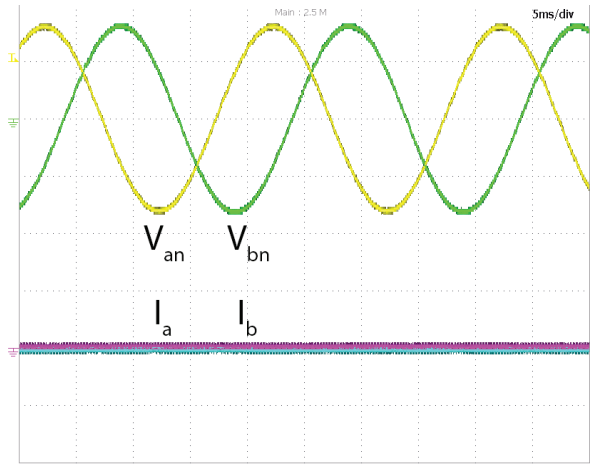

Figure 13. Experimental results under no load conditions, undamped condition. (Voltage 200 V/div).

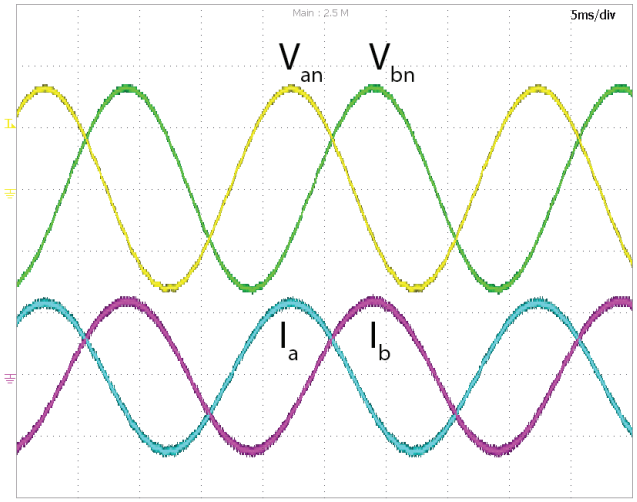

Figure 14. Experimental results under linear a 12 kW balanced load, (Voltage 200 V/div, Current 20 A/div).

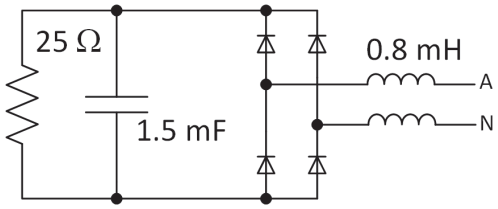

Figure 15. Single phase non-linear load

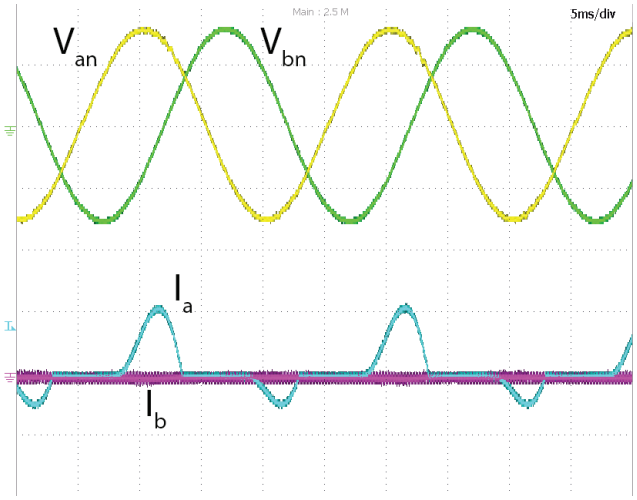

Figure 16. Steady-state behavior for single-phase non-linear load, 4 kW. (Voltage 200 V/div, Current 50 A/div).

CONCLUSIONS

The combined control action provided by the digital Dead-Beat and Repetitive controllers is proposed and tested. DB-RC resulting controller is being able to take characteristic benefits of each control strategy. DB acts primarily to compensate load variations, whereas RC provide the necessary harmonic regulation. Illustrated experimental results performed both in steady-state and transient conditions were used to emphasize the control action of either the Repetitive Control or the Dead-Beat algorithm.

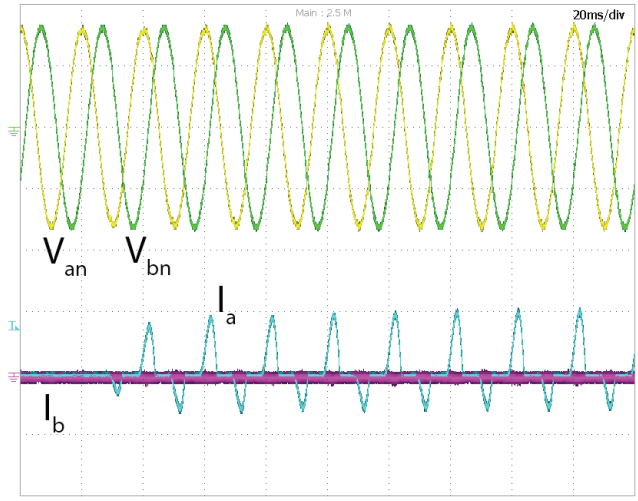

Figure 17. Single-phase non-linear load step test from 0 kW to 4 kW. (Voltage 200 V/div, Current 50 A/div).

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