Body diode reliability investigation of SiC power MOSFETs

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Abstract

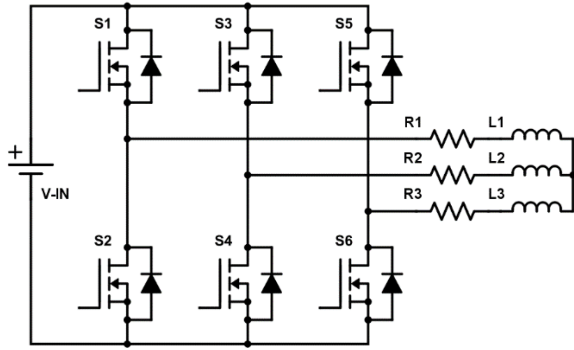
A special feature of vertical power MOSFETs, in general, is the inbuilt body diode which could eliminate the need of having to use additional anti-parallel diodes for current freewheeling in industrial inverter applications: this, clearly, subject to their demonstration of an acceptable level of reliability. Recent improvements in Silicon Carbide (SiC) power MOSFET device manufacturing technology has resulted in their wider commercial availability with different voltage and current ratings and from various manufacturers. Hence, it is essential to perform characterisation of its intrinsic body diode. This paper presents the reliability assessment of body diodes of latest generation discrete SiC power MOSFETs within a 3-phase 2-level DC-to-AC inverter representing realistic operating conditions for power electronic applications.

1. Introduction

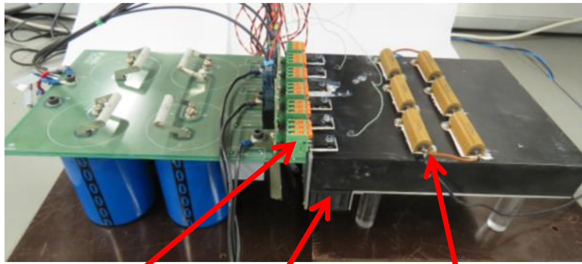
Silicon carbide (SiC) power MOSFET device manufacturing technology has significantly improved over the last few years, which has resulted in their wide commercial availability with different voltage and current ratings from various vendors [1, 2]. The creation of metal oxide semiconductor (MOS) devices using SiC has been greatly favoured than any other wide bandgap (WBG) semiconductor material due to the presence of its stable native oxide (SiO_2). Power MOSFET is a normally OFF voltage controlled transistor switch with bi-directional current flow. On top of that, it also offers an intrinsic body diode which eliminates the need of using anti-parallel diode for current freewheeling in an inverter. These features also make power MOSFETs a famous choice for synchronous rectification within inverters [3]. Therefore, it is really important to assess the reliability of the body diode of SiC power MOSFETs which is an important requirement prior to their implementation within industrial as well as commercial power electronics applications.

2. Inverter test setup, operation and waveforms

The test circuit designed for body diode characterisation is a 3-phase 2-level inverter with inductive load ($L_1 = L_2 = L_3 = 20mH$). The schematic of the implemented inverter is shown in Fig. 1 (a). The inverter was operated with star connected inductive load. The series resistors in Fig. 1 (a) represent the equivalent series resistance of each inductor. The experiments were designed so that the inverter would operate for 1000 hours for a given set of test conditions. During that time, the body diode test was stopped at regular intervals in between to monitor if any degradation of the body diode had occurred by measuring electrical parameters of the DUTs, namely body diode forward voltage drop (V_f) and drain leakage current (I_{LEAK}).



(a)



Connectors ***Fans*** ***Power Resistors***

(b)

Fig. 1. (a) – Schematic of three-phase Inverter test circuit; (b) – Implemented Inverter Hardware

The implemented hardware test circuit based on the schematic in Fig. 1 (a) is included in Fig. 1 (b). The designed power plane PCB was a double sided PCB with 4 oz copper and the gate drivers were mounted vertically onto the power plane PCB directly without using wires in order to avoid voltage overshoot by reducing parasitic inductance. The rating of capacitor bank is 900V to allow (V_{IN}) characterisation up to 900V and the DUTs were horizontally screwed onto the heatsink to allow characterisation at different case temperatures (T_{CASE}) up to 150°C. A dedicated heat sink, as seen in Fig. 1 (b), was designed using power resistors and fans for heating up and cooling down respectively in order to be able to maintain the desired T_{CASE} temperature for DUTs during operation as well as measurements. The spring type connectors were used for connecting the DUTs which allowed easy disconnecting of DUTs from the power PCB during parameter measurements.

An open loop pulse width modulation (PWM) control was implemented to control the switching pattern of 6 DUTs. In an ordinary 3-phase inverter, the gate signals of the 2 switches in one leg should be complementary with an insertion of dead-time (t_{dead}) between the commutations to avoid any shoot-through. During the dead-time, the body diode of the MOSFET is used for current flow. After the dead-time, the MOSFET is turned ON and then, the current flows through the channel and hence the technique synchronous rectification. The switching commutation in each leg is also phase-shifted by 120°. The switching frequency of the carrier signal (f_{SW}) was 10 kHz and the modulating frequency was set to 50 Hz with a modulation index (M) of 0.6. The test conditions are summarised in Table 1.

Table 1: Summary of test conditions

V_{IN}	T_{CASE}	V_{GS}	t_{dead}	I_{PH}	*f_{SW}	*M
(V)	(°C)	(V)	(ns)	(A)	(Hz)	
600	90	+20/-5	400	21	10000	0.6

*f_{SW} = switching frequency; *M = modulation index;

The sinusoidal output phase currents of the inverter at 50Hz are shown in Fig. 2.

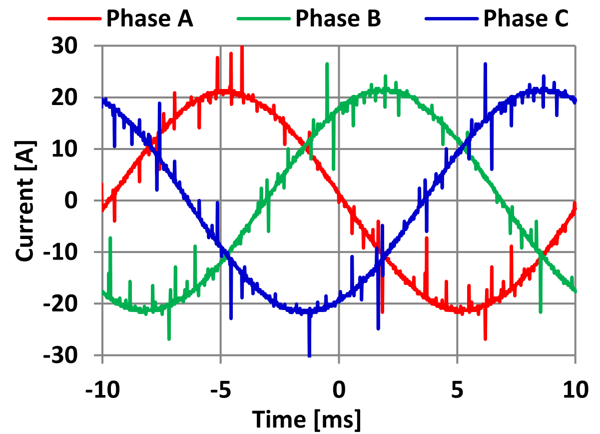


Fig. 2. Three-phase inverter sinusoidal output current at 50Hz

The gate signals of two DUTs in one leg are shown below in Fig. 3 to demonstrate the dead-time.

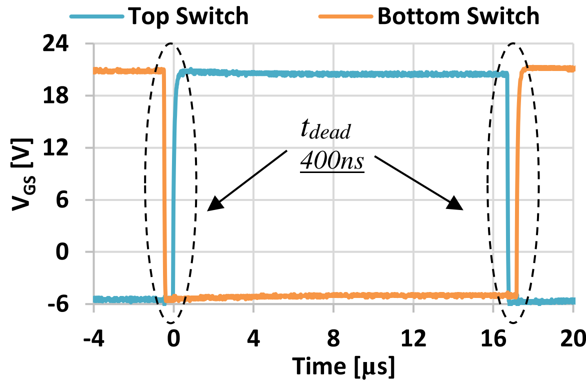


Fig. 3. Gate Signal waveforms for top and bottom switch – (S1 and S2)

3. Experimental Results and Discussion

The cross sectional structure of a typical SiC power MOSFET is illustrated in Fig. 4 below. The lightly doped n- drift layer between the p- body and n+ substrate is used to support the blocking voltage of the MOSFET during the OFF state. Therefore, the inherent body diode of a MOSFET basically forms a PiN diode.

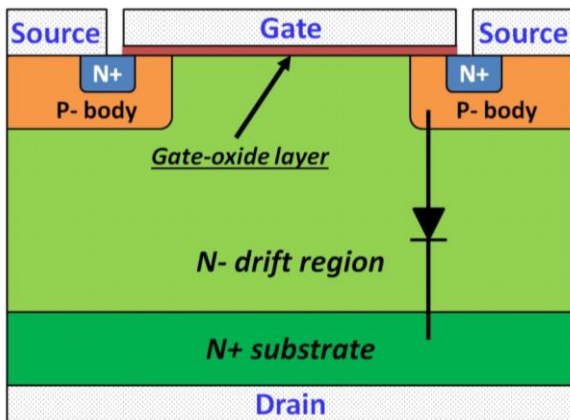


Fig. 4. Cross section of a typical SiC power MOSFET structure

3.1. Measurement test setups

The measurement circuit for V_f (measured at diode current [I_D] equal 500mA) and I_{LEAK} (measured at V_{DS} = 960V; 80% of the rated breakdown voltage of the device) are shown in Fig. 5 (a) and (b) respectively. Keithley 2635A SourceMeter was used for I_D and I_{LEAK} current measurements. It has the capability to measure dc current as small as 1pA and hence ensuring accurate I_{LEAK} current measurements.

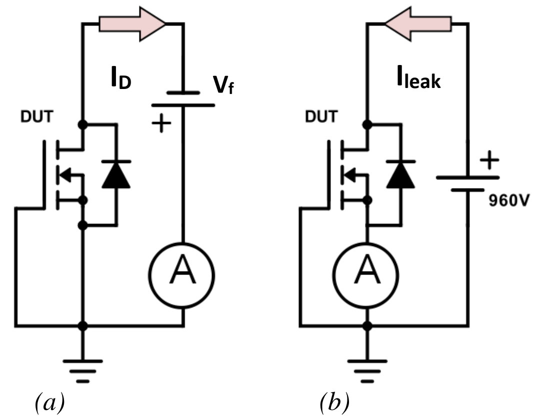


Fig. 5. Schematics for parameter measurements; (a) – Body diode forward voltage drop (V_f); (b) – Drain leakage current (I_{LEAK})

3.2 Experimental Results

As mentioned earlier, the above mentioned parameters were being measured at regular intervals and their behaviour are presented in Fig. 6 – 9 below. The results below for Dev_A and Dev_B (both with 80mΩ on-state resistance and TO-247 package) are for latest generation discrete SiC MOSFET devices from two different manufacturers.

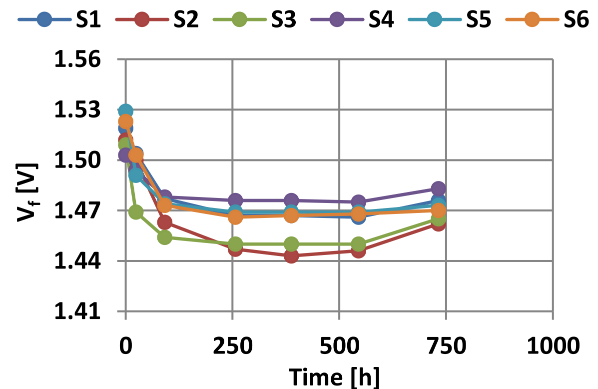


Fig. 6. Body diode forward voltage drop (V_f) evolution – ***Dev_A***

For Dev_A, Fig. 6, the V_f initially decreased slightly but then became quite stable afterwards. For the Dev_A DUTs, no significant increase in V_f has been observed with the stress.

As shown in Fig. 7, however, the drain leakage current I_{LEAK} increased for all the DUTs, with one device manifesting clear signs of degradation (S3).

During the body diode test of Dev_A DUTs, 2 of the devices had destroyed and hence, it was not possible to complete the test for the complete 1000 hours as initially mentioned. However, the obtained results for up to approximately 750 hours overall show a reasonable qualitative overview of their behaviour due to the applied stress.

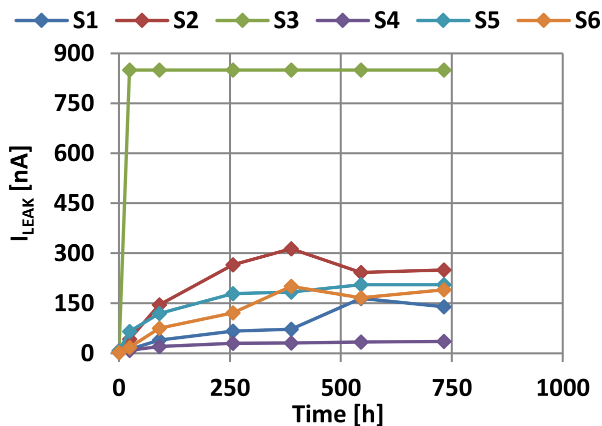


*Fig. 7. Drain leakage current (I_{LEAK}) evolution – **Dev_A***

For Dev_B, a more pronounced positive shift in V_f was observed for all DUTs as can be seen from Fig. 8. After the initial positive shift, the V_f stabilised for all DUTs.

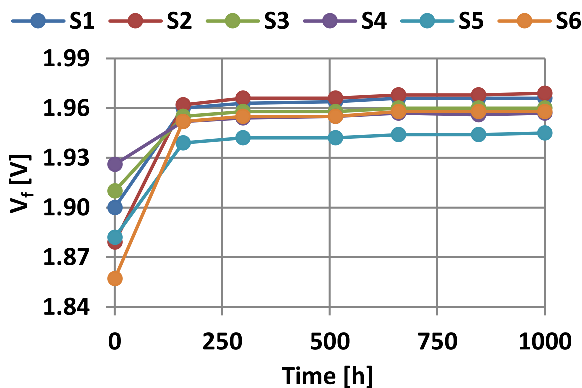


*Fig. 8. Body diode forward voltage drop (V_f) evolution – **Dev_B***

It is however interesting to note that the drain leakage current I_{LEAK} in this case remains almost constant for all six Dev_B DUTs, as shown in Fig. 9.

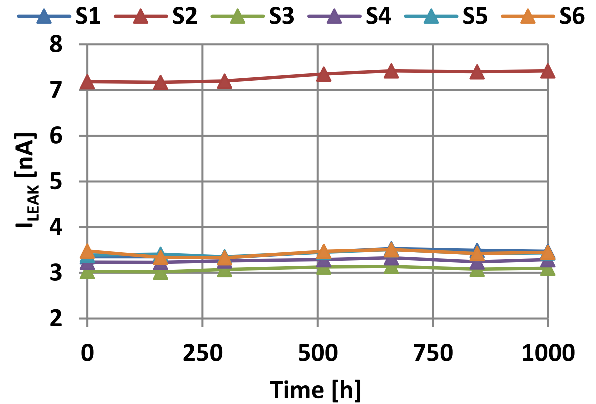


*Fig. 9. Drain leakage current (I_{LEAK}) evolution – **Dev_B***

Static tests were also performed on Dev_A and Dev_B DUTs where the body diode of the MOSFET was forward biased with 10A continuous current at T_{CASE} = 90°C. A total of 4 DUTs for Dev_A were stressed for a total of 100 hours. During the stress, the test was stopped at regular intervals to plot the body diode forward characteristics (I_D vs. V_f) as included in Fig. 10. Only one DUT is presented and the other 3 devices also showed similar behavior.

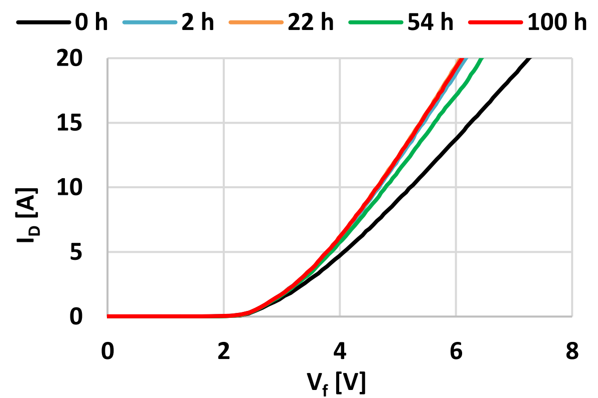


*Fig. 10. Body diode forward characteristics – **Dev_A***

The general trend observed for all 4 Dev_A DUTs tested during static test is that the body diode forward characteristics curve moves towards the left (decrease of V_f for a given current value) confirming the results obtained in Fig. 6. Some temporary relaxation of the forward characteristics in Fig. 10 is observed when the curve for 54h (green) moves back slightly towards the right. At 100h, the (red) curve shifts back to the left overlapping the curves for stress

at 2h (light blue) and 22h (orange).

On the other hand, the Dev_B DUTs showed a completely different behavior. Out of the 4 devices tested for 20 hours, 2 showed no signs of degradation i.e. no shift in body diode forward characteristics, however, for other 2 devices, the forward characteristics curve shifted towards the right and then became stable (increase in V_f for a given current value). Fig. 11 shows the forward characteristics for one of the Dev_B DUT which showed the V_f shift.

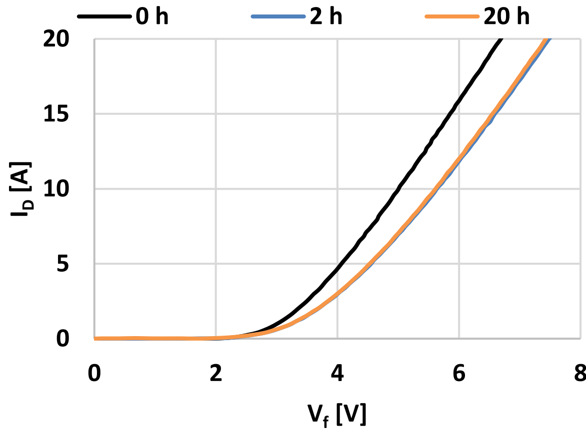


*Fig. 11. Body diode forward characteristics – **Dev_B***

3.3 Discussion

During the operation of an inverter, four different types of stresses that the DUTs undergo could be identified. High $\frac{dV}{dt}$ when the devices are switching is one of them. The other two being the body diode forward current conduction and reverse blocking periods. Last but not least, is the stress when the body diode forward current has to be diverted when the device is turned ON (upon formation of the channel) since this is the case in synchronous rectification. Fig. 12 presents how the typical drain source current flow lines within the MOSFET at 3 different time instances would look like. The 3 different time instances are as follows: 1) forward current conduction of the body diode; 2) body diode forward current diversion to the channel and 3) current conduction through channel when device is fully ON and diode completely OFF. For case 2, though small in the case of SiC, reverse-recovery current still flows internally in the device. Such current forms a loop through the channel and hence, device sees high current spike at that instance.

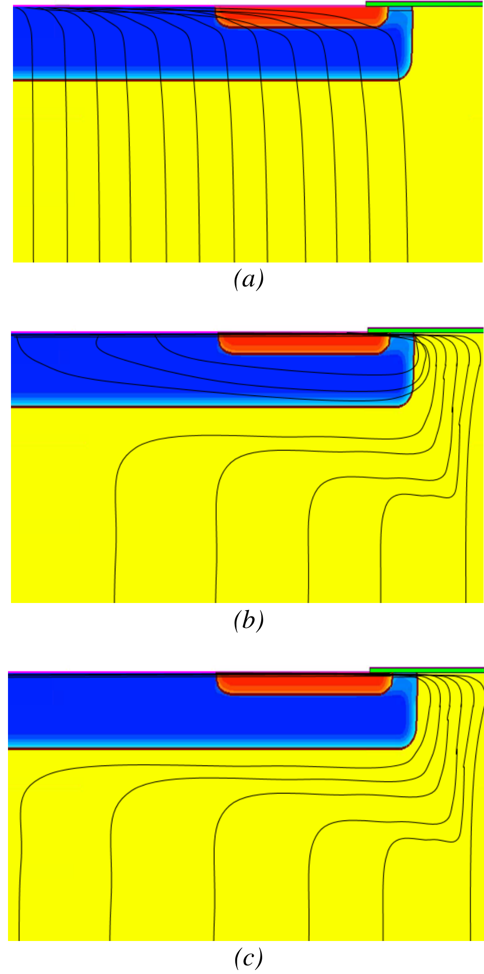


Fig. 12. Current flow lines for a MOSFET within inverter
(a) – body diode forward current conduction
(b) – body diode current diversion to the channel
(c) – current conduction through the channel

An increasing V_f is attributed in some literatures to the basal plane dislocations (BPDs) in the epitaxial layer, which results in formation of stacking faults (SF) upon forward biasing of SiC PiN diode [4, 5]. Positive change in V_f is undesirable as it can adversely affect the inverter's performance and efficiency. However, the measured initial decrease in the V_f values for Dev_A DUTs in Fig. 6 and Fig. 10 would require further investigations for a thorough physical explanation.

Authors interpret that the increase in I_{LEAK} for Dev_A, Fig. 7, is contributed not only by the stress of the body diode structure, but also by the stress

imposed when the device undergoes the reverse-recovery and the reverse bias stress during the MOSFET's forward voltage blocking periods. One possible physical mechanism for increased drain leakage current is the recombination-induced SFs. The SFs which are caused as a result of forward biasing of the body diode act as recombination centers. These recombination centers introduce electronic states in the middle of the bandgap, which, in turn, behave as generation centers when the body diode is reverse biased, causing a higher leakage current [4]. In [6], another possible mechanism is discussed for MOSFETs with thin gate oxide layer: is gate-induced I_{LEAK} due to band-to-band tunneling taking place within the depletion region in the gate/drain overlap region when the MOSFET is in the blocking state.

Results for Dev_B, Fig. 8, are in line with the interpretations formulated in [4, 5]. Results in Fig. 9, can be best understood when reference is made to results already presented about the avalanche capability and unclamped inductive switching (UIS) performance of the devices, in particular the interpretation given about the Dev_B devices having a higher breakdown voltage (i.e., probably lower values of electric field in the drift region) than their Dev_A counterparts [7].

It is of interest to note that the body diode degradation becomes significant for higher current values as depicted in Fig. 10 and 11 for static stress. It is really important to take this into account since the body diode of a MOSFET deployed in an inverter is forward biased under a wide spectrum of current values. Since all the V_f measurements for DUTs stressed within the inverter were carried out for I_D = 500 mA (see definition of V_f in section 3.1), which is quite close to the knee voltage of the body diode, therefore, it might be that the real impact of the stresses on DUTs may be somewhat underestimated. Going forward, it would be beneficial to plot I_D vs. V_f characteristics at timely intervals for the devices stressed within the inverter instead to have a much better understanding of the V_f degradation due to the stresses applied.

Various technological advances have been reported in order to improve the device technology so that the body diode reliability of SiC power MOSFET is enhanced [8 – 10]. From the results obtained, clearly there is still room for improvements. An external schottky barrier diode (SBD) with smaller diode forward voltage drop (V_D) than the V_f of the body diode could instead be used in parallel with the SiC power MOSFET so the current during dead-time does not flow through the body diode. Although, using SBDs provides a better substitute; however, the concept of using the body diode of the MOSFET is lost and this would also increase the associated cost and size of SiC device [4, 11]. As proposed in [11], novel SiC MOSFET structure such as the diode-integrated SiC power MOSFET (DioMOS) structure could be explored and investigated so that the body diode reliability issue of the conventional SiC MOSFET could be solved.

4. Conclusion

Body diode reliability tests on SiC power MOSFETs are being performed. Overall aim is to compare different SiC MOSFETs of similar ratings from various manufacturers and also study the effect of body diode conduction time by varying dead-time on its reliability. Improvements at technology levels are crucial to minimize the shift in V_f. Novel MOSFET structure such as DioMOS could be an alternative to avoid the reliability issues of the conventional body diode of SiC power MOSFET.

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