Model Predictive Control for a Dual Active Bridge Inverter with a Floating Bridge

Shajjad Chowdhury, *Student Member, IEEE*, Patrick W. Wheeler, *Senior Member, IEEE*, Chris Gerada, *Member, IEEE* and Chintan Patel, *Member, IEEE*

***Abstract*—This paper presents a Model Predictive Control technique applied to a dual active bridge inverter where one of the bridges is floating. The proposed floating bridge topology eliminates the need for isolation transformer in a dual inverter system and therefore reduces the size, weight and losses in the system. To achieve multilevel output voltage waveforms the floating inverter DC link capacitor is charged to the half of the main DC link voltage. A finite-set Model Predictive Control technique is used to control the load current of the converter as well as the floating capacitor voltage. Model predictive control does not require any switching sequence design or complex switching time calculations as used for SVM, thus the technique has some advantages in this application. A detailed analysis of the converter as well as the predictive control strategy is given in this paper. Simulation and experimental results to validate the approach are also presented.**

***Index Terms*—Dual inverter, model Predictive control, open end winding induction motor, floating bridge.**

I. INTRODUCTION

THIS paper describes a power converter topology for use with an open-ended three phase load. This converter topology is considered due to its higher fault tolerance capacity, which may be useful in some applications such as EV or HEV applications [1, 2]. The use of a dual inverter bridge allows the converter to emulate the waveforms seen in three-level Neutral Point Clamped (NPC) converters [3]. Recently the dual bridge topology has received attention from researchers due to the simplicity of power stage. The circuit implementation requires fewer capacitors than the flying capacitor topology [4], fewer isolated DC supply than H-bridge converters [5] and fewer diodes than NPC converters [6]. For example, a three-phase three-level NPC converter has 6 extra diodes, the flying capacitor converter requires an additional capacitor control and H-bridge converters require two additional isolated supplies. The other advantages of dual bridge inverter with respect to single ended multi-level inverters includes fault tolerant capability [7] and reduction in the voltage blocking requirement for some of the power semiconductor devices. This topology also maintains the distribution of switching events, leading to a lower device commutation frequency and thus reducing the losses in the system for given output waveform quality. Dual inverter topologies have been considered in numerous papers for different applications.

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Traditional dual inverter topologies (using two isolated dc sources) have been analyzed [8-10], with different space vector modulation schemes used to generate multilevel output voltage waveforms. A block diagram of a traditional open phase load and associated converters is shown in Fig. 1. It is possible to use a single supply for the dual inverters with common mode elimination technique [8, 11]. These topologies use specific switching combinations that produce equal common mode voltages which cancel at load terminals. Reduction in the number of voltage levels and lower dc bus utilization are the main disadvantages of this type of topology.

A modulation technique to balance power between the two inverters in a dual inverter system has been proposed [12, 13]. This topology still uses an isolation transformer; the size of this transformer can be reduced at the expense of reduced modulation index. The floating capacitor bridge topology along with a control scheme to allow the supply of reactive power was introduced in [14]. Other authors [15] have presented methods to compensate for supply voltage droop in order to keep the drive operational in constant power mode. This topology uses a floating capacitor bridge to offset the voltage droop in high speed machines.

To remove the isolation transformer and achieve multilevel output voltage waveforms, a dual inverter with a floating capacitor bridge is considered in this paper. The charging and discharging switching sequences are identified along with the limitation of the available states to allow proper control of the floating capacitor voltage. This paper also presents a model predictive control (MPC) scheme to control the load current and floating dc link voltage independently. MPC consider the model of the system in order to predict the future behavior of the system utilizing all available voltage vectors, thus calculation time will be higher. Identification of the available states limitation will allow the controller to choose between 25 states instead of 64, therefore the calculation time will be lower.

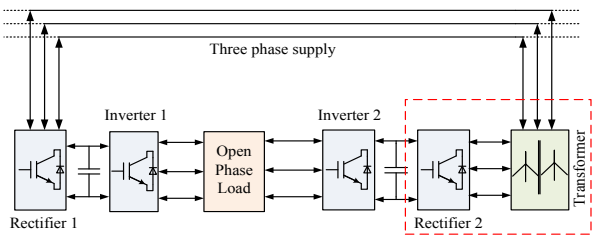

Fig. 1. Conventional Dual Active Bridge Topology.

II. PROPOSED DUAL INVERTER SYSTEM

A. Floating capacitor bridge inverter

The floating bridge capacitor dual inverter based topology has previously been analyzed for different applications [14-16]. The circuit can be used to supply

reactive power to a machine and to compensate for any supply voltage droop. In both cases the possibility of multilevel output voltage waveforms were not considered. A control scheme to charge the floating capacitor bridge along with multilevel voltage output has been presented [17]. In this reported method the main converter works in six step mode and the floating converter is called conditioning inverter which is improving the waveform quality. In this paper the capacitor in the floating inverter bridge is charged using redundant switching combinations to remove the need for any isolation transformer and to achieve multilevel output voltage waveforms. Fig. 2 shows a block diagram of the dual inverter with a floating bridge and associated capacitor. The use of a dc link voltage ratio of 2:1 allows the dual bridge inverter to produce up to a four-level output voltage waveform [18]. A circuit diagram of proposed system is presented in Fig 3.

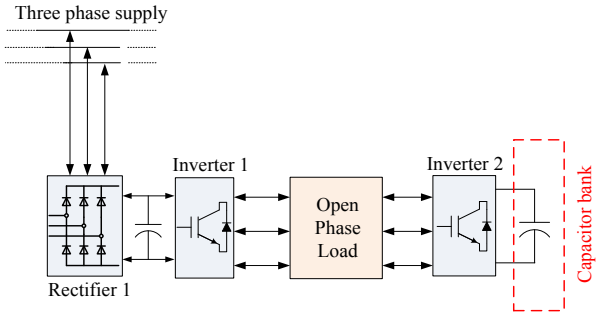

Fig. 2. Block diagram of proposed floating bridge topology.

B. *Principles of operation*

The floating bridge capacitor voltage can be controlled by directing the load current through the floating capacitor in either direction. To consider the direction of the load current through the floating capacitor, switching combinations produced by the dual two-level inverter have been analyzed. The dual two-level inverter produces 64 switching states as shown in fig. 4, which is a representation of three phase quantity utilizing a single vector in the α-β co-ordinates. The space vector diagram is obtained considering that both the converters are fed by isolated voltage sources with a voltage ratio of 2:1.

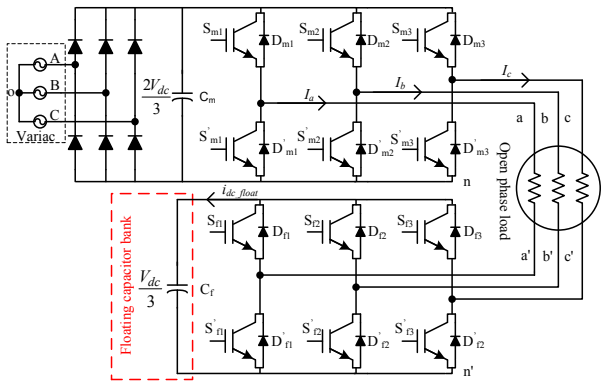

Fig. 3. Circuit diagram of proposed floating bridge topology (Capacitor bank is charged to half of the main DC link voltage).

In the state diagram red numbered switching combinations discharge the floating capacitor, while the green numbered switching combinations charge the floating capacitor. The blue numbered switching combinations hold the last state of capacitor and are therefore neutral in terms of the state of charge of the floating capacitor [19, 20]. As an example state (74) in Fig.4 gives the switching sequences for both converter's top switches 7 (1 1 1) represents the top three switches for main inverter and 4(0 1 1) represents the switching states for top three switches of the floating converter. A circuit diagram of charging and discharging switching states are presented in Fig. 5. It can be seen from the Fig. 5 that combination (11) charges the floating capacitor by directing the current from the positive to negative terminal of the floating capacitor. Combination (74) will result in a current in the opposite direction and will therefore act to discharge the capacitor whilst giving the same output voltage. Combinations ending with 7 (111) or 8 (000) are zero states and will therefore have no impact of floating capacitor's voltage.

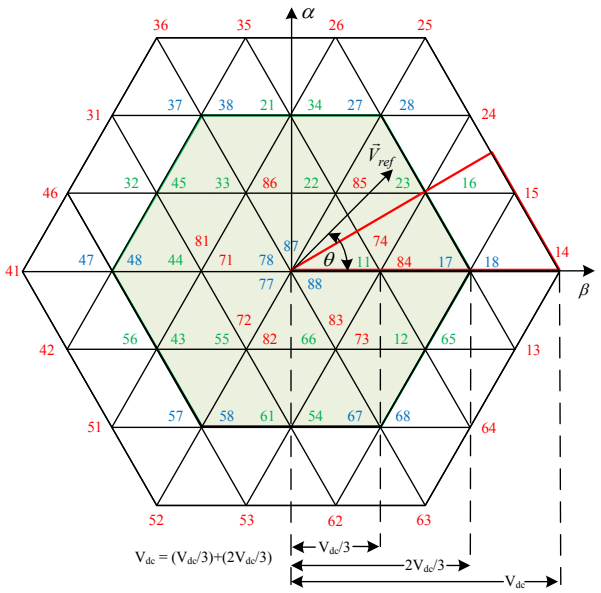

Fig. 4. Space vector of dual two-level inverter (source ratio 2:1).

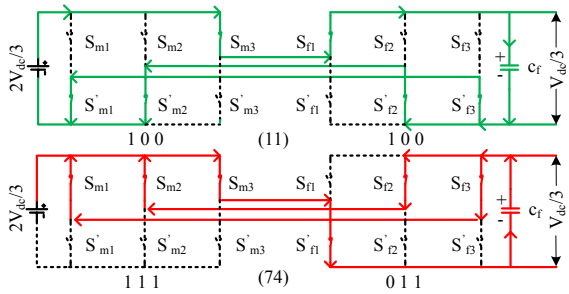

Fig. 5. Current flow for different switching states.

From Fig. 4 it is evident that if the reference voltage resides in outer hexagon then there are only two switching combinations in each sector to charge the floating capacitor. This is insufficient to maintain the charge under all operating conditions; therefore a restriction has to be imposed. As a result the achievable number of voltage levels is reduced to three along with lower than ideal DC bus utilization. Therefore the floating capacitor can charge to half of the main DC link capacitor voltage only if the reference voltage resides inside the green hexagon [Fig. 4].

III. PREDICTIVE CONTROL

A. *Control Procedure*

A model predictive control scheme can be used to control the load current and floating capacitor voltage. Predictive control can be achieved by predicting the future load current and DC link voltage at each sample time. To

achieve accurate control good quality load and converter modeling is necessary. Predictive control uses the finite number of possible switching states generated by the converter and in this case evaluates the load current and floating capacitor voltage for each state. The predicted value is then compared to reference value at each sample time and the control selects the next switching states to minimize the predicted error. A block diagram of control strategy for the proposed system with an *R-L* load is shown in Fig. 6 and the control algorithm can be summarized as

- The values of current and floating DC link voltage reference are defined and the actual values are measured.
- For each valid switching state of the converter the load current and floating DC link voltage for the next sampling instant are predicted.
- A cost function is used to evaluate the error between references and the predicted values for each switching state.
- A weighting factor is applied to the floating capacitor voltage term in the cost function to match the error magnitude with current error reference.
- The switching state that generates the minimum cost function value is selected and applied to the converter for the next sampling period.

B. Modeling of the converter and load for predictive control

For the proposed converter topology shown in Fig.3, each of the two-level converters has eight possible switching states and when they are connected as shown the total number of states increases to sixty-four. All sixty-four states are presented in the vector diagram shown in Fig. 4. It can be seen that there are a lot of redundant states which can be ignored to make the calculation time smaller. To charge the capacitor and to achieve three-level voltage output only twenty-five states are selected. All the vectors of the outer hexagon are ignored.

The converter state combinations are selected so that the average generated voltages across the load are 180° phase shifted from each other. This phase shift is necessary to achieve maximum available converter voltage across load terminal. Using Clarke's transformation the balanced three phase system can be represented as two phase (α-β) system using equation (1). In the equation X represents either the current or the voltage, as appropriate.

$$X_\alpha = \frac{1}{3}\left[2X_a - \left(X_b + X_c\right)\right]$$
$$X_\beta = \frac{1}{\sqrt{3}}\left[X_b - X_c\right] \quad (1)$$

The output voltage of the converters can therefore be synthesized as a function of DC link voltage and the state of the switching devices S_α and S_β.

$$V_{\alpha\_main} = S_{\alpha\_m} V_{dc\_main}$$
$$V_{\beta\_main} = S_{\beta\_m} V_{dc\_main} \quad (2)$$

$$V_{\alpha\_float} = S_{\alpha\_f} V_{dc\_float}$$
$$V_{\beta\_float} = S_{\beta\_f} V_{dc\_float} \quad (3)$$

$$V_\alpha = V_{\alpha\_main} - V_{\alpha\_float}$$
$$V_\beta = V_{\beta\_main} - V_{\beta\_float} \quad (4)$$

Subscript *a, b, c* represents the three phase system, α-β represents the two phase system after using Clarke's transformation. Components of main inverter and floating inverters are denoted by subscript '*main*' and '*float*'. Now the continuous model of the load can be modeled in α-β coordinates using equations (5 - 8).

$$V_{\alpha\beta} = Ri_{\alpha\beta} + L\frac{di_{\alpha\beta}}{dt} \quad (5)$$

The equation (5) is then used to get the predicted current value

$$\frac{di_{\alpha\beta}}{dt} = \frac{V_{\alpha\beta}}{L} - \frac{Ri_{\alpha\beta}}{L} \quad (6)$$

$$\frac{i_{\alpha\beta}^{k+1} - i_{\alpha\beta}^{k}}{Ts} = \frac{V_{\alpha\beta}^{k}}{L} - \frac{Ri_{\alpha\beta}^{k}}{L} \quad (7)$$

$$i_{\alpha\beta}^{k+1} = \left(1 - \frac{RTs}{L}\right) i_{\alpha\beta}^{k} + \frac{Ts}{L} V_{\alpha\beta}^{k} \quad (8)$$

Here, R and L are the load resistance and inductance, $i_{\alpha\beta}^{k}$ and $V_{\alpha\beta}^{k}$ are the load current and voltage at current sample time in α-β coordinates. Ts is the sample time and $i_{\alpha\beta}^{k+1}$ is one sample ahead predicted current value. To control the capacitor voltage the charging and discharging switching combinations are identified the green and red switching sequences in Fig. 4 respectively. Then DC link current for the floating DC link is identified.

$$i_{dc\_float} = S_{\alpha\_float} i_\alpha + S_{\beta\_float} i_\beta \quad (9)$$

The prediction for floating capacitor voltage can be found by evaluating:

$$i_{dc\_float} = C\frac{dv_{dc\_float}}{dt} \quad (10)$$

$$v_{dc\_float}^{k+1} = \frac{Ts * i_{dc\_float}^{k}}{C} + v_{dc\_float}^{k} \quad (11)$$

Here, i_{dc_float} is the floating DC link current, C is the capacitance, $v_{dc\_float}^{k}$ and $v_{dc\_float}^{k+1}$ is the current and predicted capacitor voltages respectively. The calculation time for the control is high and the control action will delay the output by one sample period. To compensate for these delay the prediction of current and capacitor voltage will simply be two samples ahead of the current values [21]. This is achieved first calculating the one sample ahead current values by using the currently applied voltage vectors as shown in equation (8). Then this one sample ahead current value is used to predict two sample ahead current values by utilizing all the available converter voltage vectors to minimize the predicted error, shown in equation (12). Same technique is used to predict two samples ahead predicted value of floating capacitor voltage as shown in equation (13).

$$i_{\alpha\beta}^{k+2} = \left(1 - \frac{RTs}{L}\right) i_{\alpha\beta}^{k+1} + \frac{Ts}{L} V_{\alpha\beta}^{k+1} \tag{12}$$

$$v_{dc\_float}^{k+2} = \frac{Ts * i_{dc\_float}^{k+1}}{C} + v_{dc\_float}^{k+1} \tag{13}$$

Here, *(k+2)* refers to the predicted value at two sample periods ahead. As the DC link voltage does not change considerably in one sample period thus, $v_{dc\_float}^{k+1}$ is assumed to be the current floating DC link value in this paper. The reference *α-β* currents are generated as sine and cosine functions which are 90° phase shifted from each other. The reference floating DC link voltage is calculated from main inverters DC link voltage magnitude; by simply dividing the main inverters DC link voltage amplitude by two. To achieve proper control over the floating capacitor voltage a table is created to identify the floating inverters DC link current along with its direction related to the switching states. Identification of the floating DC link current is achieved using the states shown in Fig.5. The floating DC link voltage is then predicted using these current values and then compared with the reference value. The control is included in the cost function to minimize the error at the end of the next sampling period.

To predict the reference current value two sample periods ahead a Lagrange extrapolation method is used [22]. The reference current value becomes:

$$i^{*}{}_{k+2} = 6i^{*}{}_{k} - 8i^{*}{}_{k-1} + 3i^{*}{}_{k-2} \tag{14}$$

(k+2) is two step ahead predicted value, *k* is the current value, *(k-1)* is the previous value and *(k-2)* is two step behind value. The reference for the floating DC link voltage is generally constant at all times. The two cost functions are defined separately for the current and voltage, all the values used in these calculations are two sample periods ahead of the sample time.

$$g_i = \sqrt{\left(i_{\alpha}^{*k+2} - i_{\alpha}^{k+2}\right)^2 + \left(i_{\beta}^{*k+2} - i_{\beta}^{k+2}\right)^2} \tag{15}$$

$$g_{v\_float} = \lambda \sqrt{\left(V_{dc\_float}^{*} - v_{dc\_float}^{k+2}\right)^2} \tag{16}$$

$$g = g_i + g_{v\_float} \tag{17}$$

Here,

$$\lambda = \frac{\left|i^{*}\right|}{v_{dc\_float}^{*}} \tag{18}$$

Here g is the total cost function and λ is the weighted factor to normalize the floating voltage error in contrast with the current errors.

Finally, to demonstrate the performance of the converter an open end winding induction motor is used as a load. The predictive control algorithm used in this paper is based on well-known Indirect Rotor Flux Oriented (IRFO) induction motor control [23]. The speed loop of the IRFO control will generate the torque producing current reference (i^{*}_{sq}) and the field current (i^{*}_{sd}) reference will be a constant value. Rotor flux oriented stator voltage *d-q* equations (19 and 20) are used [23] to predict the *d-q* axis current shown in equations (21) and (22).

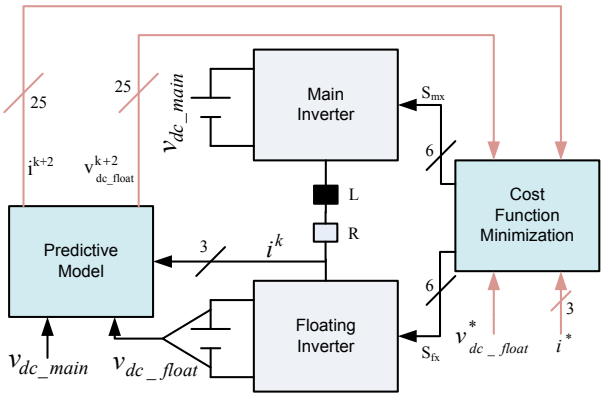

Fig. 6. Predictive current control of dual two-level inverter with one bridge floating with a R-L load.

To achieve two steps ahead current values first, one step ahead current values are calculated using previously applied voltage vector along with present current values. These one step ahead current value is then used to calculate the two step ahead current values using all available voltage vectors to minimize the predicted errors.

$$V_{sd}^{*} = R_s i_{sd} + \sigma L_s \left(\frac{d}{dt} i_{sd} - \omega_e i_{qs}\right) + \frac{L_m}{L_r} \frac{d}{dt} \psi_{rd} \tag{19}$$

$$V_{sq}^{*} = R_s i_{sq} + \sigma L_s \left(\frac{d}{dt} i_{sq} + \omega_e i_{ds}\right) + \omega_e \frac{L_m}{L_r} \psi_{rd} \tag{20}$$

$$i_{sd}^{k+2} = i_{sd}^{k+1} + T_s \left(\frac{V_{sd} - R_s i_{sd}^{k+1}}{\sigma L_s} + \omega_e i_{sq}^{k+1}\right) \tag{21}$$

$$i_{sq}^{k+2} = i_{sq}^{k+1} + T_s \left(\frac{V_{sq} - R_s i_{sq}^{k+1}}{\sigma L_s} - \omega_e i_{sd}^{k+1} + \frac{\omega_e L_m^2 i_{sd}^{k+1}}{\sigma L_r L_s}\right) \tag{22}$$

Here, V_{sd}^{*} and V_{sq}^{*} are the reference *d* and *q* axis stator voltages, R_s, L_s, L_r *and* L_m are the stator resistance, stator inductance, rotor inductance and magnetizing inductance respectively. Terms i_{sd}, i_{sq}, ω_e and ψ_{rd} are the stator *d* and *q* axis currents, electrical speed and rotor d-axis flux correspondingly. Here, sigma (σ) is the leakage factor of the machine and can be described using equation (23).

$$\sigma = 1 - \left[\left(L_m^2\right) / \left(L_s L_r\right)\right] \tag{23}$$

As the controller is in d-q plane the converter voltages and currents can be transferred to d-q plane, using equation (24).

$$\begin{aligned} X_d &= X_\alpha \cos\left(\theta_{\psi r}\right) + X_\beta \sin\left(\theta_{\psi r}\right) \\ X_q &= X_\beta \cos\left(\theta_{\psi r}\right) - X_\alpha \sin\left(\theta_{\psi r}\right) \end{aligned} \tag{24}$$

$$\theta_{\psi r} = \int \left(\frac{i_{sq}^{*}}{i_{sd}^{*} \tau_r} + \omega_{re}\right) \tag{25}$$

$$\tau_r = \frac{L_r}{R_r} \tag{26}$$

Here, subscript *d,q* and $\theta_{\psi r}$ represents the d-q axis components and rotor flux angle. If the machine is operating in constant flux region then the rotor flux angle can be calculated using equation (25). In equation (25), ω_{re} represents the rotor electrical speed in rad/sec, τ_r is the rotor

time constant which can be described as equation (26) and superscript '*' denotes the reference values. The floating DC link capacitor voltage is predicted using equation (13). The controller will generate different *q*-axis current reference for different operating conditions of the machine. To normalize the errors all three cost functions will require three separate weighing factors. The cost functions with different weighting factors are presented in equation (27 - 29).

$$g_i = \lambda_d \sqrt{\left(i_{sd}^{*k+2} - i_{sd}^{k+2}\right)^2} + \lambda_q \sqrt{\left(i_{sq}^{*k+2} - i_{sq}^{k+2}\right)^2} \tag{27}$$

$$g_{v\_float} = \lambda_{dc} \sqrt{\left(V_{dc\_float}^{*} - v_{dc\_float}^{k+2}\right)^2} \tag{28}$$

$$g = g_i + g_{v\_float} \tag{29}$$

Here, λ_d, λ_q and λ_{dc} are the weighting factor for *d-q* axis current and floating DC link voltage. The weighting factors are calculated using reference values, the stator d-axis reference current and floating capacitor voltage references are kept constant. The only variable is the reference torque producing (q-axis) current, which varies depending on loading conditions. To provide equal weight to all these three controllers the error of control variables is normalized using equation (30). The normalizing factor will update automatically depending on the load. The calculation of the weighting factors are provided in equation (30).

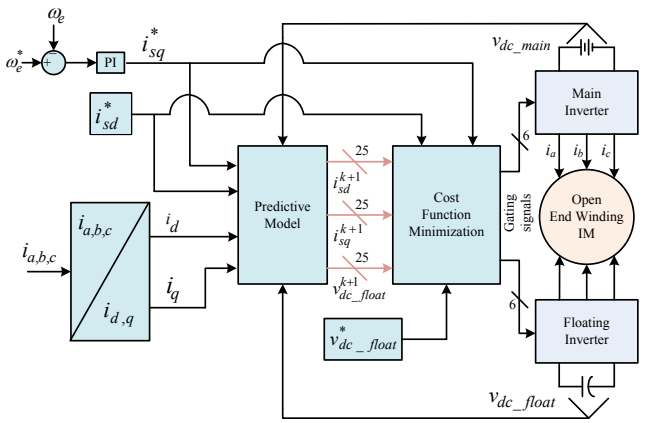

Fig. 7. Block diaram of inducton motor drive using predictive current control of dual two-level inverter with one bridge floating.

$$\lambda_d = \frac{\left|i_q^*\right|\left|V_{dc\_float}^*\right|}{\left(\left|i_d^*\right|\left|i_q^*\right|\right)+\left(\left|i_d^*\right|\left|V_{dc\_float}^*\right|\right)+\left(\left|i_q^*\right|\left|V_{dc\_float}^*\right|\right)}$$

$$\lambda_q = \frac{\left|i_d^*\right|\left|V_{dc\_float}^*\right|}{\left(\left|i_d^*\right|\left|i_q^*\right|\right)+\left(\left|i_d^*\right|\left|V_{dc\_float}^*\right|\right)+\left(\left|i_q^*\right|\left|V_{dc\_float}^*\right|\right)} \tag{30}$$

$$\lambda_{dc} = \frac{\left|i_q^*\right|\left|i_d^*\right|}{\left(\left|i_d^*\right|\left|i_q^*\right|\right)+\left(\left|i_d^*\right|\left|V_{dc\_float}^*\right|\right)+\left(\left|i_q^*\right|\left|V_{dc\_float}^*\right|\right)}$$

A simplified block diagram of a motor drive using predictive control algorithm to control the d-q axis current is shown in Fig. 7. This is a hybrid control where fast inner current control loops are replaced with predictive control algorithm. The control requires the additional PI controller to generate the reference torque producing current. The floating DC link voltage reference is set using a constant value which is equal to half of the main inverters DC link voltage to reduce calculation time for drive operation.

C. *Simulation results*

The proposed system has been simulated using both PLECS and SIMULINK to compare losses between three different converter topologies. After the losses are compared, the converter performance with predictive control algorithm is demonstrated for static R-L load and with an induction machine.

Three converter types were selected to compare losses of the proposed power converter topology, a single sided three-level NPC, a dual two-level inverter with equal DC link voltage ratio and the proposed dual inverter topology. All these three topologies provide three-level output voltages and therefore it is important to compare them in terms of losses. To calculate the losses the NPC and the main converter of the floating dual inverter was supplied with 970 volts DC and the secondary of floating topology was charged to 485 Volts. Dual inverter with equal DC link voltage was supplied with 485 volts DC on both sides. These DC link voltage levels were selected to achieve the rated fundamental load voltage of 690 Volts RMS. The dead-time was set to $4.1\mu s$. The device losses were calculated using semiconductor device characteristics selected according to required blocking voltage and current requirements of the topology.

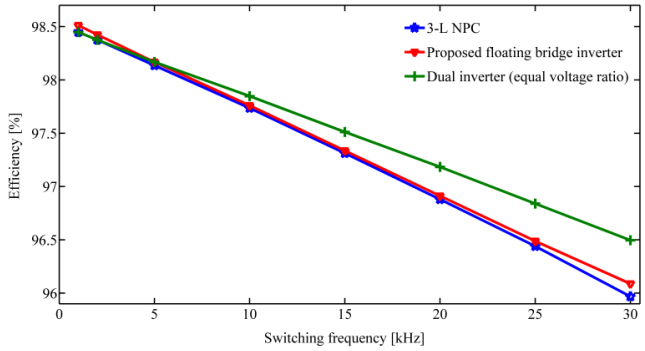

Fig. 8. Loss comparison in different power converter topologies.

The loss calculations are in terms of switching and conduction losses for the power converters and in this comparison all other circuit losses were ignored. Fig. 8 shows the efficiency at full load (12 KW) with varying average switching frequency. It can be seen from the figure that, for this particular load, dual inverter with equal dc link voltage ratio has better efficiency than the other topologies. The three-level NPC has six extra clamping diodes, thus the losses are higher. Proposed floating bridge dual inverter has slightly better efficiency than three-level NPC but less efficient than dual inverter with equal dc link voltage. The reason for using a dual inverter compared to single sided inverters are redundancy and to modulate high frequency fundamental. To achieve the results with R-L load the main converter was supplied by a DC source of 200 Volts and the floating converter voltage maintained at 100 Volts to achieve the required multilevel voltage output waveforms. Initial charging of the capacitor was achieved by injecting a small reference current and the full reference DC link voltage. The charging transients were slowed down by using ramped reference values. All the parameters set in the simulation are similar to experimental system to compare the results and the dead-time was set to 4 μs.

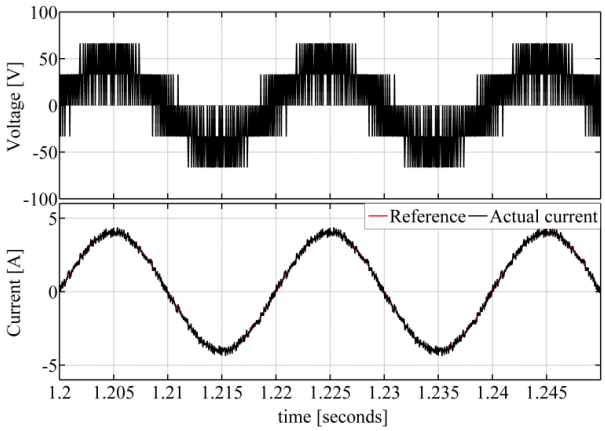

Fig. 9. Phase voltage ($V_{AA'}$) and current (I_a) when the reference is set to 4 Amps.

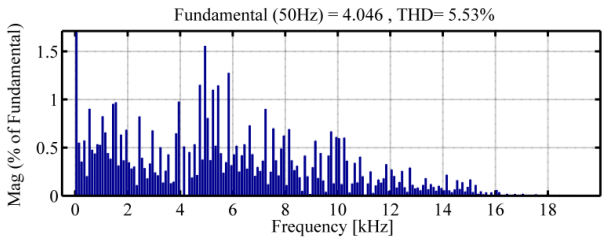

Fig. 10. FFT of phase current.

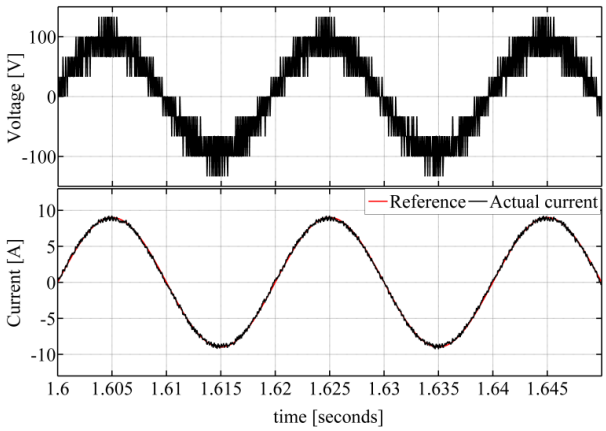

Fig. 11. Phase voltage ($V_{AA'}$) and current (I_a) when the refernce is set to 9 Amps.

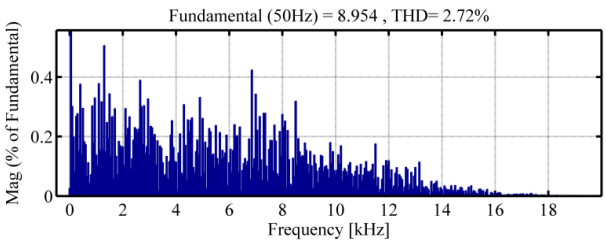

Fig. 12. FFT of phase current.

Snubbers and parasitic inductors were ignored in this simulation. The output pulses were slightly altered to eliminate the dead-time interval effect inherent in this family of converter topologies [24]. Fig. 9 shows the phase voltage and current when the system demands peak current of 4 Amps. This result shows the two-level operation of the converter and the phase current follows the reference value with a small error as expected. Fig. 11 shows the same results for a reference of 9Amps, and show operation with a three-level output voltage waveform. It can be seen that the actual current is closely following the reference current and that the converter can achieve a multilevel voltage output waveform. Frequency spectrums of both the currents are presented in Fig. 10 and Fig. 12, in both cases harmonics are spread all over the frequency range.

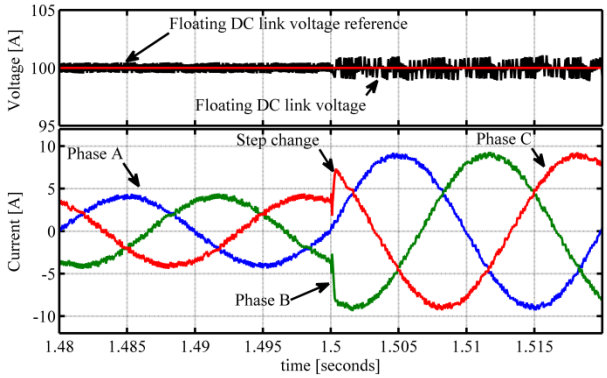

Fig. 13. Step response of the controller from top to bottom: Floating DC link voltage and three phase currents.

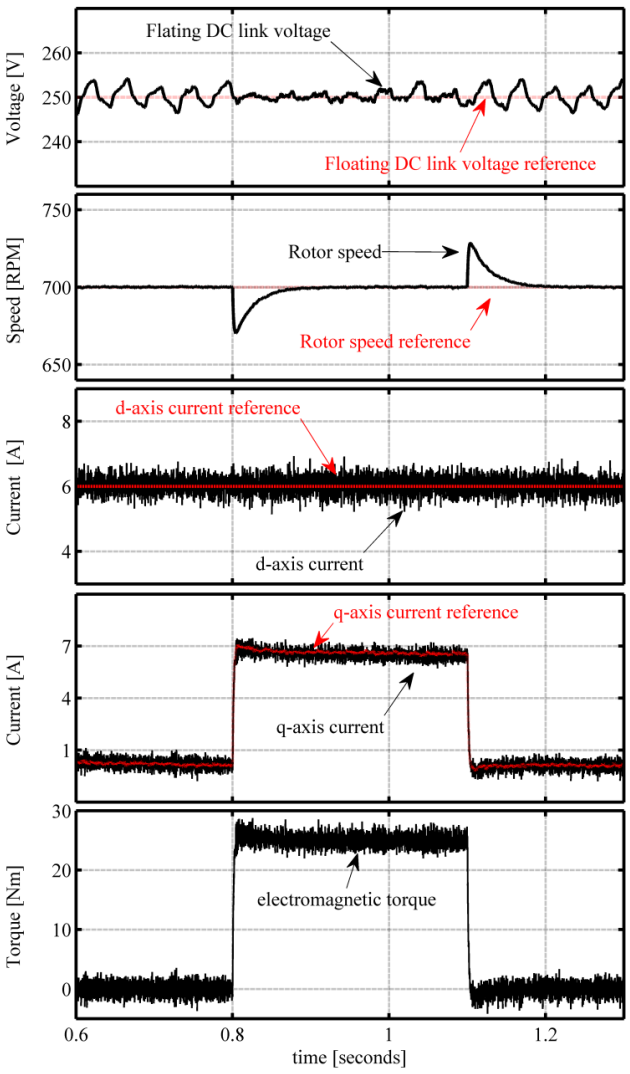

Fig. 14. Controller response to a step load applied after speed reaches steadystate. Top to bottom: floating capacitor voltage, rotor speed, d-axis current, q-axis current and electromagnetic torque.

To check the control dynamics a change in current reference from 4Amps to 9Amps was applied. It can be seen

from the Fig. 13 that the output current magnitude changes immediately according to the change in reference and there is no effect on the floating capacitor voltage.

Finally, an open end winding induction motor was used to verify the performance of the converter. To achieve the results the main converter was supplied by a 500 Volts DC source and the floating capacitor voltage was charged at 250 Volts. The sampling frequency was set to 12.5 kHz. The performance of the drive is presented in Fig. 14. In the figure the machine is in steady state at 700 rpm when a step load is applied to the machine at t = 0.8 seconds and back to zero at t=1.1 seconds. The torque producing q-axis current quickly increases to counter the load torque. It can be seen from the simulation results in Fig. 13 and in Fig.14 that at no time does the capacitor voltage overcharge or collapse.

The phase voltage and current are shown in Fig. 15 for the operation when the machine was loaded along with the frequency spectrum of the phase current shown in Fig.16.

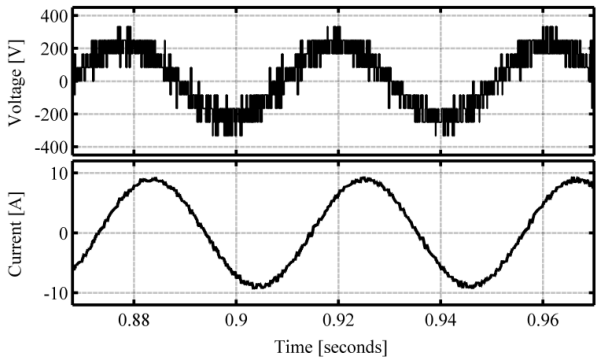

Fig. 15. Phase voltage ($V_{aa'}$) and current (I_a) when the machine is loaded.

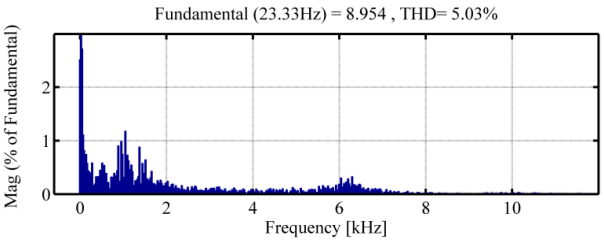

Fig. 16. FFT of phase current.

It can be conclude from the simulation results that the proposed system can maintain the capacitor charge under all operating conditions and achieve multilevel output voltage waveform.

D. Experimental results

To validate simulation results an experimental converter has been built and tested, as shown in Fig. 17. The power converters used for this experiment is one of the 'off the shelf' converters manufactured by SEMIKEON [27]. These two-level converters have R-C snubbers and input and output common mode inductors. The converter also has onboard defined dead-time that varies from 4 – 4.1 µs along with propagation delay which varies from 0.1 to 0.2 µs and thus becomes very difficult to align the pulses for dead-time voltage spike removal algorithm. The power circuit of the experimental converter is shown in Fig.18. The system has been tested with an R-L load and the parameters are shown in table I. To demonstrate the behavior of the dual inverter system with predictive control, a demand reference current of 4Amps sinusoidal reference with a 50 Hz frequency was applied. The results are shown in Fig. 19 and can be compared to the simulation results in Fig 9. Fig. 20 shows the frequency spectrum of phase current and it can be seen that the harmonic distortion is high and the harmonics are spread over the frequency range, as expected from model predictive control due to the inherent variable switching frequency. To demonstrate the multilevel operation of the converter, a 50 Hz and 9Amps current reference was applied to the control system. The results are presented in Fig.21. In the figure the converter achieves multilevel voltage output waveform as expected. Fig. 22 shows the frequency spectrum of the phase current waveform for multilevel voltage output. The current distortion is reduced from 8.66% to 4.05%. One way to control the frequency spectrum is to use modulated model predictive control [25, 26], but this is beyond the scope of this paper. A step change in current reference from 4Amps to 9Amps was demanded from the system to check the transient behavior of the control scheme. Results are presented in Fig. 23. It can be seen that the load current tracks the change in reference and it has no impact on floating capacitor voltage.

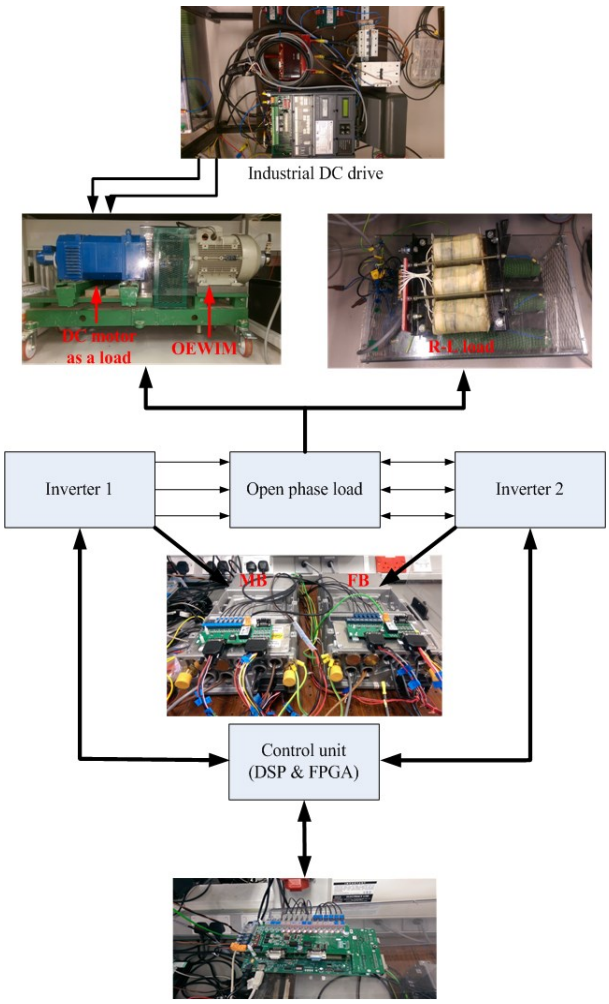

Fig. 17. Experimental Converter and Contorl Platform.

Fig. 24 shows the execution time for MPC algorithm. To evaluate the MPC execution time the interrupt was set to 10 kHz (100 µs), it can be seen from the top plot of Fig. 24 that the sampling time is 70.5µs if all 64 states are utilized to predict the current, which is not necessary in this case. The calculation time reduces to 38.1µs when only 25 states are considered. To achieve the experimental results for open end

winding induction motor drive, the main converter was supplied by a 500 Volt DC source. The floating capacitor was initially charged using reference d-axis current. After the floating capacitor was charged to the required value a speed command was set at 700 rpm. The results presented show the steady state and dynamic performance of the motor drive. It can be seen form Fig. 25 that, at steady state no load operation the floating capacitor voltage fluctuates but it is less than 3% of the steady-state value. A step load was applied at t = 1.45 seconds, reference q-axis current steps up immediately to counter the load torque. It can be seen that the floating DC link voltage is more stable when the machine is loaded, this is because the machine is drawing real power and the capacitor voltage can be charged and discharged quickly. It can be seen from Fig. 23 and Fig. 25 that the controller is robust enough to maintain the floating DC link voltage and currents to the required value for both static R-L load and induction motor drive. The phase voltage and current for the machine are presented in Fig. 26. It can be seen that the converter achieves multilevel output voltage.

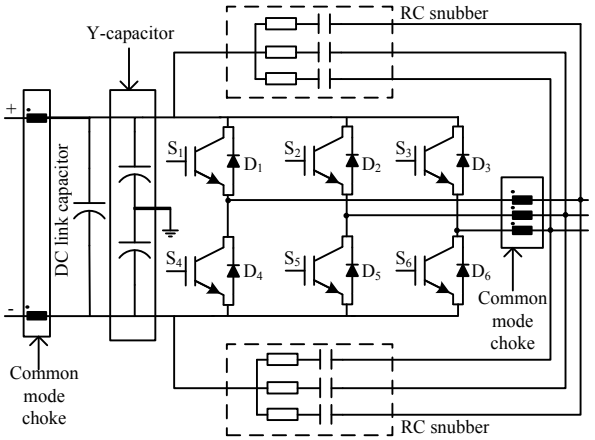

Fig. 18. SEMIKRON's SKAI module.

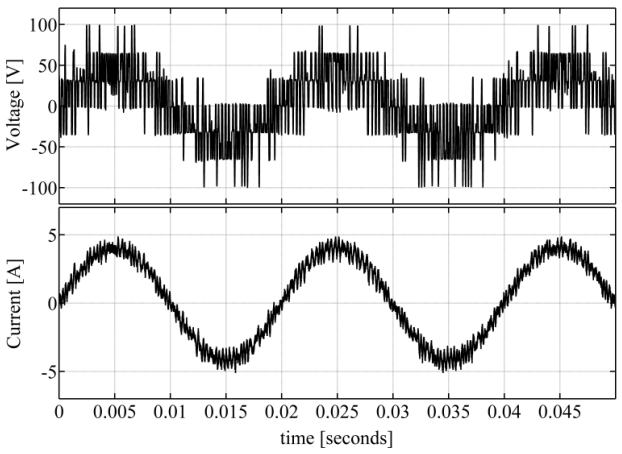

Fig. 19. Current reference is set to 4 amps. Top to bottom : phase voltage $V_{AA'}$, and phase current I_a.

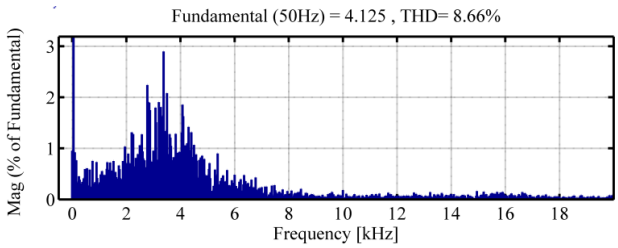

Fig. 20. FFT of the phase current.

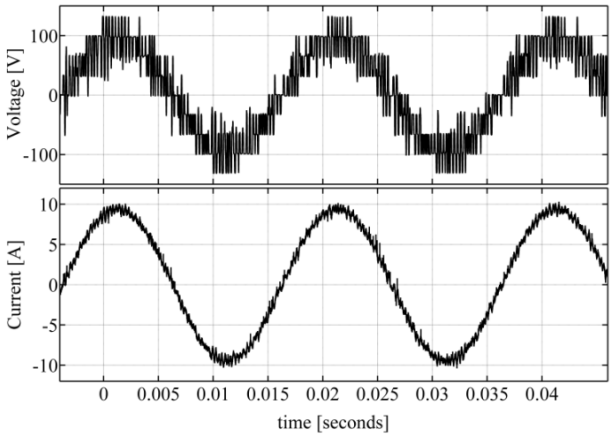

Fig. 21. Current reference is set to 9 amps. Top to bottom : phase voltage $V_{AA'}$, and phase current I_a.

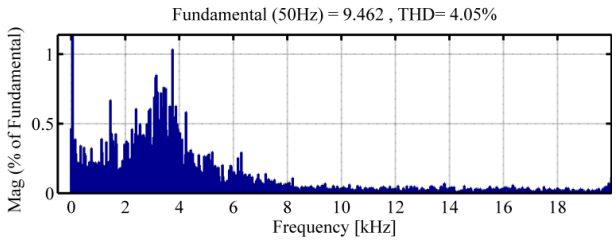

Fig. 22. FFT of phase current.

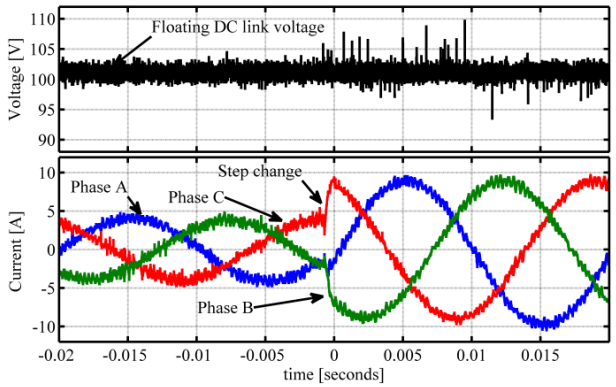

Fig. 23. A step change in current reference from 4 to 9 amps. Top to bottom : floating capacitor voltage and three phase currents.

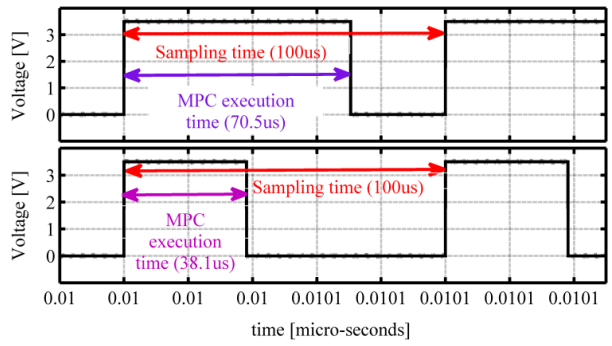

Fig. 24. MPC exicution time for utilizing 64 states (top), utilizing 25 states (bottom) for R-L load operation.

Frequency spectrum of phase voltage and phase current are presented in Fig.27 and in Fig. 28 respectively. In all the FFT analysis, current harmonic distortions of experimentally achieved results are higher than the simulation results; this is because ideal switches are considered in simulation.

Furthermore, the snubber circuits are absent in simulation. The snubber circuits present in the experimental rig forms an L-C resonant circuit and cause oscillation in the current waveform thus increases the current harmonic distortion in experimental results.

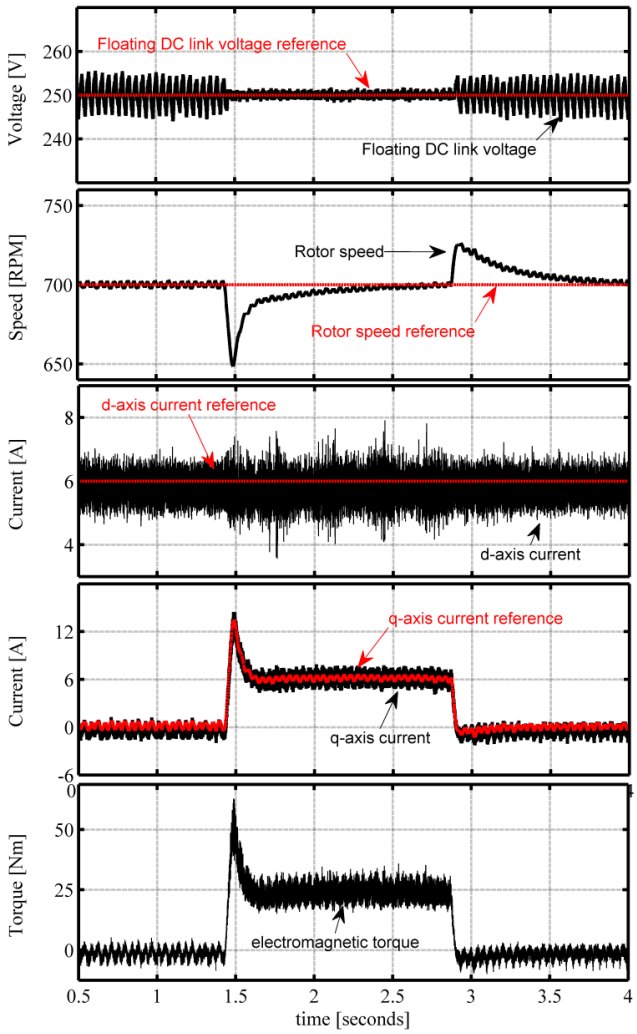

Fig. 25. Controller response to a step load applied after speed reaches steadystate. Top to bottom: floating capacitor voltage, rotor speed, d-axis current, q-axis current and electromagnetic torque.

TABLE I. PARAMETERS

R-L Load			
Resistance	R	10.6	Ohm
Inductance	L	3.8e-3	H
DC link capacitance	C	3250	µf
Main DC link	Vdc_main	200	Volts
Floating DC link	Vdc_float	100	Volts
Sampling frequency	f_s	20	kHz
Switching frequency (average)	f_{sw}	4	kHz
Induction motor			
Stator resistance	R_s	1.4	Ohm
Rotor resistance	R_r	1.02	Ohm
Stator leakage inductance	Ll_s	0.01151	H
Rotor leakage inductance	Ll_r	0.00926	H
Magnetizing inductance	L_m	0.22580	H
DC link capacitance	C	3250	µf
Main DC link	Vdc_main	500	Volts
Floating DC link	Vdc_float	250	Volts
Sampling frequency	fs	12.5	kHz
Switching frequency (average)	f_{sw}	3	kHz

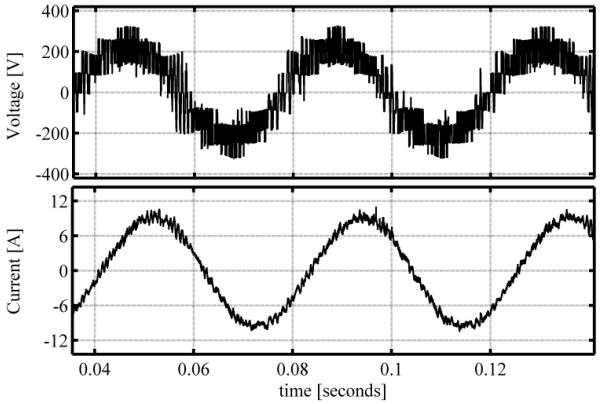

Fig. 26. Phase voltage ($V_{aa'}$) and current (I_a) when the machine is loaded.

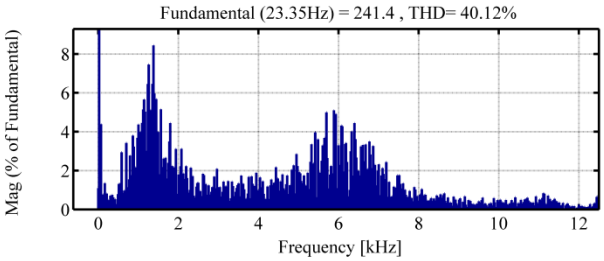

Fig. 27. FFT of the phase voltage.

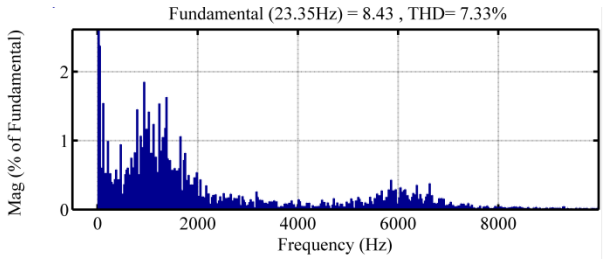

Fig. 28. FFT of the phase current.

IV. CONCLUSIONS

A dual active bridge converter with a floating inverter has been proposed and analyzed in this paper. A set of charging and discharging switching sequences have been identified to enable the control of the floating capacitor bridge voltage to half of the main DC link voltage. This particular ratio is used to achieve multilevel output voltage waveforms. A model predictive control scheme is used to control the load current and floating capacitor voltage. The proposed system has been simulated and an experimental setup has been used to validate the results. It has been shown that the proposed system can charge the capacitor to the required value under all operating conditions and that the converter can achieve multilevel output voltage waveforms.

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