

Common-mode Voltage Reduction for Matrix Converters Using All Valid Switch States

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Abstract—This paper presents a new space vector modulation (SVM) strategy for matrix converters to reduce the common-mode voltage (CMV). The reduction is achieved by using the switch configurations that connect each input phase to a different output phase, or the configurations that connect all the output phases to the input phase with minimum absolute voltage. These two types of configurations always produce lower peak CMV than the others, especially the former ones that result in zero CMV at the output side of matrix converters. In comparison with the existing SVM methods, this strategy has a very similar software overhead and calculation time. Simulation and experiment results are shown to validate the effectiveness of the proposed modulation method in reducing not only the peak value but also the root mean square value of the CMV.

Index Terms—Common-mode Voltage, Matrix Converters, Singular Value Decomposition, Space Vector Modulation.

I. INTRODUCTION

THE matrix converter (MC) has been a promising power converter topology during the past decades [1], [2]. The main reason for this interest lies in the potential advantages of MCs, such as direct conversion, controllable input displacement factor, bi-directional power flow and high power density.

The modulation algorithm is one of the important factors in determining the performance of MCs. The existing modulation algorithms for MCs are intrinsically based on the well-known pulse-width modulation (PWM) [3]. As a result of the PWM switching pattern, MC generates a series of staircase-like high frequency common-mode voltage (CMV) waveforms. Similar CMV also appears in three-phase inverters [4]–[6]. Large magnitude and high frequency variation of CMV, unfortunately, have been known as the root causes of early motor winding failure and machine bearing deterioration [7].

Different methods have been reported to mitigate the detrimental influences of the CMV for MCs. An intuitive idea is

using only the rotating vectors that correspond to the switch configurations with zero CMV in dual structure converters [8]–[16]. This technique has been applied to direct and indirect MC fed open-end winding AC drives to reduce or even eliminate the CMV. However, it is not considered in this paper owing to the increased costs and control complexities introduced by additional power semiconductor devices.

Methods exist that modify modulation strategies to reduce the magnitude of the CMV issues [17]–[30]. Since the CMV is brought about by the input voltages together with different switch configurations, it is preferable to choose those with low peak CMVs and low voltage transitions whenever possible. In the space vector modulation (SVM) algorithms for MCs [31]–[33], switch configurations are selected under the criterion of minimizing the switching count. Therefore, four active switch configurations and one zero switch configuration (ZSC) are selected in each sampling period. In order to reduce the CMV, two active vectors with opposite directions or three nearest-state vectors were chosen instead during the time intervals for the zero vectors in [17]–[23]. Unfortunately, these methods use more than five switch configurations in each sampling period, thus increase the switching power losses. Besides, the latter method can be applied only when the voltage transfer ratio (VTR) is larger than 0.667 [23]. When the VTR is smaller than 0.5, Hong-Hee Lee *et al.* also put forward several CMV-reduced strategies using two adjacent vectors with 120°-phase shift to reduce the duty cycles for zero vectors [20]–[25]. From the perspective of CMV reduction, however, it is unnecessary to exclude all ZSCs, because the CMV peak of the zero vector connecting to the input phase that is with the medium voltage value is lower than those of active vectors [26]–[30].

Note that for a three-phase-to-three-phase direct MC, the switch configurations that connect each input to one different output phase have zero CMV. The corresponding voltage vectors of these switch configurations have been often referred to as the “rotating vectors”. In this context, the perhaps more appropriate name is given for this type of switch configurations, i.e. “Orientation Switch Configuration” (OSC). Nevertheless, they are regarded to be trivial in the literature [31]–[33]. It is difficult to calculate their duty cycles and arrange them in the switching sequence [34]–[42]. For example, Yugo Tadano *et al.* tried to use these switch configurations though at the cost of complex switch pattern selection [39], [40]. Jordi Espina *et al.* proposed an SVM method to replace the three ZSCs by three OSCs with same rotating direction and equal duty cycle [41]. However, it is difficult to arrange proper switching sequences to achieve safe commutation by using three ZSCs.

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Without the need of modulation, Rene Vargas *et al.* added a term in the quality function of the predictive model to suppress the CMV [43]–[46]. However, this method has a high computational overhead.

To use the OSCs in the modulation, we first investigate all valid switch configurations by applying the singular value decomposition (SVD) on their space vector representations [47]. The geometrical meaning of SVD can reveal how each switch configuration transforms a column vector between different reference frames. Thus, it provides an insight on the intrinsic properties of the switch configurations. These switch configurations are then categorized into three types according to their SVD results. The relationships between different switch configurations are also found so that the OSCs can be used easily by equivalent decomposition and combination.

We further propose a CMV-reduced modulation algorithm for MCs, taking advantage of all valid switch configurations, especially the OSCs. The proposed algorithm is divided into two VTR regions. For high VTRs, one OSC is incorporate in each sampling period by replacing its equivalent switch configurations. For low VTRs, one ZSC connecting to the input phase that is with the medium voltage value is used instead of the OSC. Therefore, by using the switch configurations with lower CMV amplitude, not only the peak value but also the root mean square (RMS) of the output CMV are reduced. Also worth mentioning is that the transition between the high and low VTR regions is smoothly achieved according to the comparison of the calculated duty cycles.

Although our proposed method is based on the traditional SVM method, it does not increase the computation burden noticeably. The calculation time increases by less than 6% from $82.84\mu s$ to the $87.64\mu s$. This is because that the inclusion of the OSCs and ZSCs in our CMV-reduced SVM method is introduced by equivalent substitution. Once the duty cycles utilized in the traditional SVM algorithms are calculated, only minor comparison and addition operations are required for the proposed method. In addition, unlike the other algorithms in [34]–[46] that also use the OSCs, our proposed method can synthesize the reference variables without the measurement of output currents. Hence, no extra components are involved.

II. MATRIX CONVERTER SYSTEM MODEL

A three-phase-to-three-phase direct MC consists of a nine-switch array, as shown in Fig. 1. By modeling each switch as an ideal switching function whose value is one when the switch is conducting and zero when the switch is blocking, the voltage relationship between the input and the output of the MC can be expressed as follows [48],

$$\mathbf{V}_o = \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \mathbf{S}\mathbf{V}_i, \quad (1)$$

where the switch state matrix (SSM) \mathbf{S} represents the connecting configuration within the MC array. Similarly, the current relationship can be formulated as $\mathbf{I}_i = \mathbf{S}^T \mathbf{I}_o$, where the superscript “ T ” means the transpose operation. The input voltages and output currents are considered as the input variables of the MC. Typically, the input side source is a voltage type since the

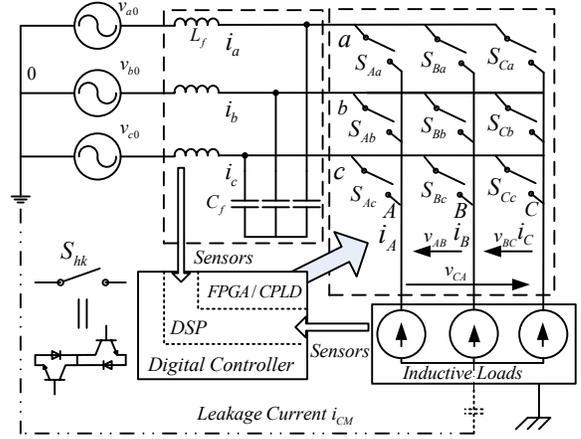


Fig. 1. Three-phase direct matrix converter topology.

MC is connected to the grid or LC filter, while the output is a current source because the MC is feeding an inductive load. Due to the nature of different sources that the MC is connected to, short circuits between the input terminals meanwhile open circuits at the output ports are prohibited. As a consequence, only 27 different switch configurations are allowed under the constraints for safe operations, which can also be represented as $S_{Ka} + S_{Kb} + S_{Kc} = 1$, for $K = \{A, B, C\}$.

In order to simplify the analysis, (1) is transformed from the abc coordinate into the $\alpha\beta$ reference frame, represented in the space vector form as $\mathbf{V}_{o,\alpha\beta 0} = \mathbf{T}\mathbf{S}\mathbf{T}^{-1}\mathbf{V}_{i,\alpha\beta 0}$, using the modified Clark Transformation [33]–[38]

$$\mathbf{T} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}. \quad (2)$$

The zero sequence current does not exist in the three-phase three-wire systems. Therefore, the voltage relationship can be expressed in matrix form by ignoring the zero component [47],

$$\begin{bmatrix} v_{o\alpha} \\ v_{o\beta} \end{bmatrix} = \begin{bmatrix} S_{1\alpha} & S_{1\beta} \\ S_{2\beta} & S_{2\alpha} \end{bmatrix} \begin{bmatrix} v_{i\alpha} \\ v_{i\beta} \end{bmatrix} = \mathbf{S}_{xyz} \begin{bmatrix} v_{i\alpha} \\ v_{i\beta} \end{bmatrix}, \quad (3)$$

where \mathbf{S}_{xyz} is the space vector representation of the transfer matrix \mathbf{S} in (1), and xyz stands for the input phases that are connected to the output ones. For example, when the output phases ABC are linked in order to the input phases abb , \mathbf{S}_{xyz} can be written as \mathbf{S}_{abb} . The input and output voltage space vectors can also be expressed as $\vec{v}_i = V_{i\alpha} + jV_{i\beta}$ and $\vec{v}_o = V_{o\alpha} + jV_{o\beta}$ respectively.

III. SINGULAR-VALUE-DECOMPOSITION-BASED SPACE VECTOR MODULATION

To show how the SSM transforms the input voltage between the input and output coordinates, \mathbf{S}_{xyz} in (3) is factorized by the SVD into the multiplication of three matrices, representing as $\mathbf{S}_{xyz} = \mathbf{U} * \mathbf{D} * \mathbf{V}^T$, where \mathbf{U} and \mathbf{V} are unitary matrices and \mathbf{D} is a diagonal matrix with σ_d and σ_q being the diagonal elements. Geometrically, matrix \mathbf{V} denotes a rotation or reflection operation to the input space vector with respect to the real axis of input side, while \mathbf{D} indicates scaling operation along

the orthonormal coordinate axes with σ_d and σ_q representing the axis gains. Subsequently, matrix \mathbf{U} rotates the intermediate vector that results from the product of input column vector, \mathbf{V}^T and \mathbf{D} , by another angle to obtain the output voltage space vector. Note that the transpose of a rotation matrix means rotating in reverse.

With the output phases ABC connected to the input phases abb respectively as an example, the space vector represented transfer matrix S_{abb} can be calculated and decomposed:

$$S_{abb} = \begin{bmatrix} 1 & -\frac{\sqrt{3}}{3} \\ 0 & 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \frac{\sqrt{3}}{2} & \frac{1}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}^T. \quad (4)$$

All valid switch configurations can be categorized into three types according to the SVD results of their space vector representation, as listed in Table I.

- *Type I: Zero Switch Configuration (ZSC).* The ZSCs connect all output lines to the same input phase and hence result in zero voltage space vectors since the output line voltages are zero. For this type of switch configurations, the diagonal elements in the matrices \mathbf{D} s are all zero.
- *Type II: Rotation Switch Configuration (RSC).* The RSCs connect two output lines to a common input phase, and connect the remaining output line to one of the other input phases. All their factorized \mathbf{U} s and \mathbf{V} s are special unitary matrices, i.e. rotation matrices. Besides, the secondary diagonal elements in matrices \mathbf{D} s are zero. It is important to point out that the rotation angles of \mathbf{U} s and \mathbf{V} s are determined only by the switch configurations, but independent of the MC inputs. If these rotation matrices are represented as their equivalent rotation vectors with same angles, two unit hexagons depicting \mathbf{U} s and \mathbf{V} s respectively can be found, as shown in Fig. 2. Both hexagons are different from those in the traditional SVM, where the switch configurations are considered together with the input voltages or output currents, and thus the resultant output voltage and input current space vectors have fixed angles but variable amplitudes [49]. Type II switch configurations are also summarized in Table II, with the rotation angles of their decomposed \mathbf{U} s and \mathbf{V} s matching the positions of their equivalent rotation vectors in different hexagons of Fig. 2.
- *Type III: Orientation Switch Configuration (OSC).* For the aforementioned OSCs, one of their factorized matrices (\mathbf{V} in this paper) determines the orientation, i.e. clock-wise or counter-clock-wise, or the positive rotation direction of the resultant rotating output voltages. In three-phase systems, this means to determine whether the coordinate is left-handed or right-handed. Corresponding to the traditional SVM, they result in rotating output voltage space vectors with fixed amplitudes since unitary matrices are isometry, but with variable angles depending on both the switch configurations and the input voltages. In addition, the matrices \mathbf{D} s for OSCs are Identity Matrices.

All the q -axis gains of the ZSCs and RSCs are equal to zero. This feature brings facilitation to synthesize the reference output voltage and input current vectors. Suppose that the desired transfer function is

TABLE I
SINGULAR VALUE DECOMPOSITION RESULTS OF ALL VALID SPACE VECTOR REPRESENTED TRANSFER MATRICES

		SVD			
		S_{SM}	U	D	V
I	S_{xxx}	$\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$
II	S_{abb}	$\begin{bmatrix} 1 & -\frac{\sqrt{3}}{3} \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ \sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} \frac{\sqrt{3}}{2} & \frac{1}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}$
	S_{cbb}	$\begin{bmatrix} 0 & -\frac{2\sqrt{3}}{3} \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ \sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$
	S_{caa}	$\begin{bmatrix} -1 & -\frac{\sqrt{3}}{3} \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ \sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} -\frac{\sqrt{3}}{2} & \frac{1}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$
	S_{baa}	$\begin{bmatrix} -1 & \frac{\sqrt{3}}{3} \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ \sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} -\frac{\sqrt{3}}{2} & -\frac{1}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$
	S_{bcc}	$\begin{bmatrix} 0 & \frac{2\sqrt{3}}{3} \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ \sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$
	S_{acc}	$\begin{bmatrix} 1 & \frac{\sqrt{3}}{3} \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ \sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ \frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}$
	II	S_{bab}	$\begin{bmatrix} -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$
S_{bcb}		$\begin{bmatrix} 0 & \frac{\sqrt{3}}{3} \\ 0 & -1 \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$
S_{aca}		$\begin{bmatrix} \frac{1}{2} & \frac{\sqrt{3}}{6} \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} -\frac{\sqrt{3}}{2} & \frac{1}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$
S_{aba}		$\begin{bmatrix} \frac{1}{2} & -\frac{\sqrt{3}}{6} \\ -\frac{\sqrt{3}}{2} & \frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} -\frac{\sqrt{3}}{2} & -\frac{1}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$
S_{cbc}		$\begin{bmatrix} 0 & -\frac{\sqrt{3}}{3} \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$
S_{cac}		$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{6} \\ \frac{\sqrt{3}}{2} & \frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ \frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}$
III		S_{bba}	$\begin{bmatrix} -\frac{1}{2} & \frac{\sqrt{3}}{6} \\ -\frac{\sqrt{3}}{2} & \frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$
	S_{bbc}	$\begin{bmatrix} 0 & \frac{\sqrt{3}}{3} \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$
	S_{aac}	$\begin{bmatrix} \frac{1}{2} & \frac{\sqrt{3}}{6} \\ \frac{\sqrt{3}}{2} & \frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} -\frac{\sqrt{3}}{2} & \frac{1}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$
	S_{aab}	$\begin{bmatrix} \frac{1}{2} & -\frac{\sqrt{3}}{6} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} -\frac{\sqrt{3}}{2} & -\frac{1}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$
	S_{ccb}	$\begin{bmatrix} 0 & -\frac{\sqrt{3}}{3} \\ 0 & -1 \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$
	S_{cca}	$\begin{bmatrix} -\frac{1}{2} & \frac{\sqrt{3}}{6} \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{2}{\sqrt{3}} & 0 \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ \frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}$
	III	S_{abc}	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$
S_{cab}		$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$
S_{bca}		$\begin{bmatrix} -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$
S_{acb}		$\begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$
S_{bac}		$\begin{bmatrix} -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & \frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$
S_{cba}		$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & \frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$

¹ xxx stands for aaa , bbb or ccc .

$$\bar{\mathbf{U}} * \bar{\mathbf{D}} * \bar{\mathbf{V}}^T = \begin{bmatrix} \cos \alpha & -\sin \alpha \\ \sin \alpha & \cos \alpha \end{bmatrix} \begin{bmatrix} g_d & 0 \\ 0 & g_q \end{bmatrix} \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix}^T, \quad (5)$$

it is easy to synthesize these continuous modulation matrices using only the first two types of switch configurations, according to the high-frequency synthesis [50]. Here $\bar{\mathbf{U}}$, $\bar{\mathbf{D}}$ and $\bar{\mathbf{V}}$ are the local averaged values of \mathbf{U} , \mathbf{D} , and \mathbf{V} respectively with respect to their duty cycles within one switching period. Since $\sigma_q \equiv 0$, the q -axis averaged gain g_q equals to zero. Hence, the output voltage reference \vec{v}_o is always located in the d -axis of the rotation matrix $\bar{\mathbf{U}}$, while the input current reference \vec{i}_i is always placed in the d -axis of the rotation matrix $\bar{\mathbf{V}}$, as shown in Fig. 3. The rotation angle θ of $\bar{\mathbf{V}}$ is exactly the angle of

TABLE II
TYPE II SWITCH CONFIGURATIONS ARRANGED ACCORDING TO FIG. 2

\bar{U} \ \bar{V}	①	②	③	④	⑤	⑥
(1)	S_{acc}	S_{bcc}	S_{baa}	S_{caa}	S_{cbb}	S_{abb}
(2)	S_{aac}	S_{bbc}	S_{bba}	S_{cca}	S_{ccb}	S_{aab}
(3)	S_{cac}	S_{cbc}	S_{aba}	S_{aca}	S_{bcb}	S_{bab}
(4)	S_{caa}	S_{cbb}	S_{abb}	S_{acc}	S_{bcc}	S_{baa}
(5)	S_{cca}	S_{ccb}	S_{aab}	S_{aac}	S_{bbc}	S_{bba}
(6)	S_{aca}	S_{bcb}	S_{bab}	S_{cac}	S_{cbe}	S_{aba}

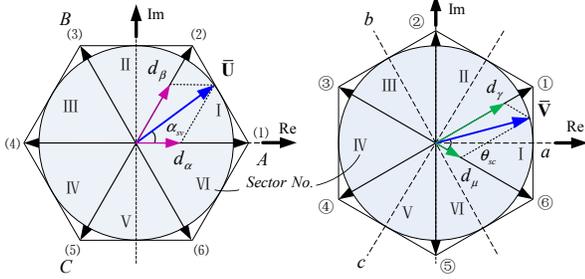


Fig. 2. Space vector syntheses using two adjacent vectors.

\vec{i}_i , while the rotation angle α of \bar{U} determines the frequency of \vec{v}_o . As a result, the output frequency and the input power factor can be controlled by the angles α and θ respectively.

To synchronously synthesize the matrices of \bar{U} , \bar{V} and \bar{D} , four Type II switch configurations are selected in accordance with the vectors used. For example, when both the input and output reference quantities lie in the Sector I, since the vectors pointing to (1), (2) and ⑥, ① are used, taking account of the mutual relationship between the vectors in Fig. 2 and the switch configurations in Table II, SSMs S_{abb} , S_{aab} , S_{acc} and S_{aac} are selected. Then their duty cycles can be calculated by

$$\begin{aligned}
 d_{\alpha\mu} &= m \cdot \sin(60^\circ - \alpha_{sv}) \sin(60^\circ - \theta_{sc}), \\
 d_{\beta\mu} &= m \cdot \sin(\alpha_{sv}) \sin(60^\circ - \theta_{sc}), \\
 d_{\alpha\gamma} &= m \cdot \sin(60^\circ - \alpha_{sv}) \sin(\theta_{sc}), \\
 d_{\beta\gamma} &= m \cdot \sin(\alpha_{sv}) \sin(\theta_{sc}).
 \end{aligned} \quad (6)$$

The modulation index m is used to adjust the amplitude of the output voltages. The remaining time interval within a sampling period is the duty cycle for the Type I switch configurations,

$$d_0 = 1 - m \cdot \cos(\alpha_{sv} - 30^\circ) \cdot \cos(\theta_{sc} - 30^\circ). \quad (7)$$

A simple method to determine m is setting it to a constant, which leads to the same results as presented in [31]. The only limitation for m is to maintain the duty cycles in (6) and (7) as nonnegative.

To complete the modulation process, the switching sequence among different switch configurations has to be arranged. To minimize the switching number, the strategy in [32], [33], with one ZSC in the centre of switching sequence, is employed as shown in Fig. 4. When the sum of two sector numbers is even a “u” shape pattern is utilized in the arrangement of the switching sequence. If the sum of two sector numbers is odd an “n” shape pattern is used.

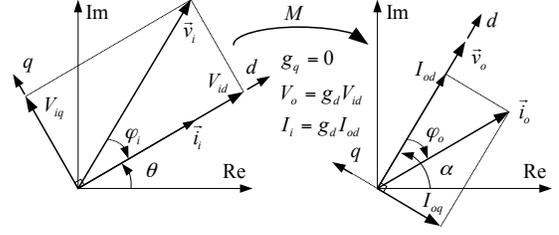


Fig. 3. Geometrical relationships between the input and output quantities.

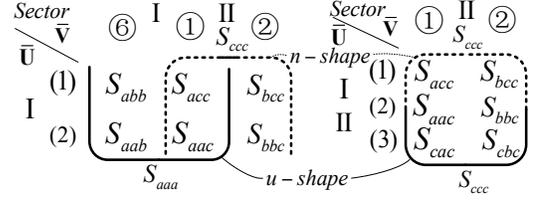


Fig. 4. Switching sequence selection with minimum commutation count.

IV. COMMON-MODE VOLTAGE REDUCED MODULATION USING ALL VALID SWITCH CONFIGURATIONS

For motor drive systems it is important to reduce the CMV generated by power converters. Since it is common to connect the motor frame to the ground, the leakage current due to the CMV flows through the parasitic capacitor coupling to the rotor. High leakage currents can lead to early failures of winding insulation and motor bearings. Since no path exists for the zero-sequence current in a three-phase three-wire system, by assuming the sum of output currents $i_A + i_B + i_C \approx 0$, the CMV becomes,

$$v_{cm} = \frac{v_A + v_B + v_C}{3}. \quad (8)$$

The instantaneous value of CMV depends on the switch states of the converter and the input voltages. The peak values of the CMV for all three types of SSMs can be calculated by [30]:

$$v_{cm} = \begin{cases} v_{im} & \text{for } ZSCs, \\ v_{im}/\sqrt{3} & \text{for } RSCs, \\ 0 & \text{for } OSCs, \end{cases} \quad (9)$$

where v_{im} is the amplitude of the input phase voltages. The OSCs should be given priority over the others in suppressing the CMV, although they are not well explored in most of the existing modulation algorithms. Generally, the ZSCs have higher CMV peak value than that of the RSCs. That is why the traditional CMV-reduced SVM methods in [17]–[23] use two active vectors with opposite directions, or three nearest vectors of RSCs to replace or reduce the time intervals for the zero vectors of ZSCs. Nevertheless, in the sense of reducing switching power losses, these methods are not favorable as they increase the device switching frequency. On the other hand, among three ZSCs, the one which connects all output phases to the same input phase carrying intermediate voltage provides a CMV peak up to $v_{im}/2$, which is lower than those of RSCs [26]–[30]. In terms of instantaneous CMV, such ZSC should take priority over the other Type I and II switch

configurations. Obviously the CMV can be decreased by using such ZSC and the OSCs.

A. Principle of decomposition and combination

In this section, a CMV-reduced SVM algorithm is proposed with uses of all valid switch states, especially the OSCs. It is important to note that there exists an interesting relationship between the last two types of switch configurations listed in Table I, as shown in the following equations:

$$\begin{aligned}
 S_{abc} &= S_{abb} + S_{bbc} = S_{acc} + S_{cbc}, \\
 S_{cab} &= S_{caa} + S_{aab} = S_{cbb} + S_{bab}, \\
 S_{bca} &= S_{bcc} + S_{cca} = S_{baa} + S_{aca}, \\
 S_{acb} &= S_{abb} + S_{bcb} = S_{acc} + S_{ccb}, \\
 S_{bac} &= S_{bcc} + S_{cac} = S_{baa} + S_{aac}, \\
 S_{cba} &= S_{caa} + S_{aba} = S_{cbb} + S_{bba}.
 \end{aligned} \tag{10}$$

Each OSC is equivalent to two different switch combinations, each of which contains two RSCs. These two RSCs are always coupled, locating at the end points of a ‘‘L’’ shape in Table II. One of the coupled switch configurations can be found by going two columns horizontally and one line vertically, or two lines vertically and one column horizontally from the other one. If both switch configurations can be obtained, it is possible to substitute them by their equivalent OSC to reduce that part of the CMV to zero.

The key idea of the decomposition principle is that any rotation vector in either the input or output hexagons of Fig. 2 can be synthesized by its two neighbor vectors. This corresponds to that any switch configuration in Table II can be formed by its two neighbors in the same line or column, with the same duty cycle. With S_{bbc} as an example, this relationship can be expressed in a mathematical form by using SSMs as

$$S_{bbc} = S_{aac} + S_{bba} = S_{bcc} + S_{cbc}. \tag{11}$$

By using this decomposition principle, two equivalent RSCs of any OSC can be acquired for substitution. To begin with, the OSCs used have to be determined. It is worth noting that the switching power losses are proportional to the number of switch configurations used and the commutating voltages and currents. To reduce power losses, only one OSC among the last six SSMs in Table I is selected in every sampling period, so that the device switching frequency will not increase. The one that rotates the input voltage space vector \vec{v}_i to the sector of the output voltage space vector \vec{v}_o is selected, as summarized in Table III. Here the sector division for the \vec{v}_i is the same as that for the \vec{v}_o in traditional SVMs, rather than that for the input current space vector \vec{i}_i . Therefore, the range from 0 to 60° in the complex plane is the first sector for \vec{v}_i . It is important to remember that the axis where the voltage space vector lies in, a , b or c , the voltage amplitude at that phase will reach its maximum. Thus, this sector division is also beneficial in judging which phase is with the medium voltage value. For instance, when the input voltage space vector \vec{v}_i lies in position (1) (note that the input voltage plane is not drawn but is the same as its output counterpart in Fig. 2), a -phase voltage v_a is the largest phase voltage among all three ones. Similarly, when \vec{v}_i points to position (2), c -phase voltage reaches its negative

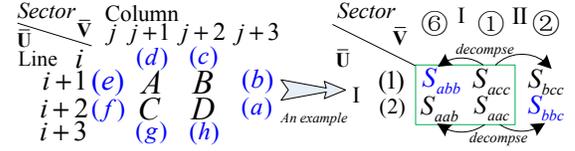


Fig. 5. The principle of selecting the Type III switch configuration.

maximum. During the whole Sector I, b -phase is the one with the intermediate voltage value.

TABLE III
SELECTION OF THE TYPE III SWITCH CONFIGURATIONS

$\vec{v}_i \backslash \vec{v}_o$	I	II	III	IV	V	VI
I	S_{abc}	S_{bac}	S_{cab}	S_{cba}	S_{bca}	S_{acb}
II	S_{bac}	S_{abc}	S_{cba}	S_{cab}	S_{acb}	S_{bca}
III	S_{bca}	S_{cba}	S_{abc}	S_{acb}	S_{cab}	S_{bac}
IV	S_{cba}	S_{bca}	S_{acb}	S_{abc}	S_{bac}	S_{cab}
V	S_{cab}	S_{acb}	S_{bca}	S_{bac}	S_{abc}	S_{cba}
VI	S_{acb}	S_{cab}	S_{bac}	S_{bca}	S_{cba}	S_{abc}

Once the OSC is chosen, within its two switch combinations, only one couple of equivalents will be used to ensure minimum power losses. As can be seen from (10), one switch configuration within each couple is always contained in the four ones that are selected by the traditional SVM discussed in Section III. But the other one within the couple, named as the supplementary switch configuration here, is not. Hence, direct substitution is impossible. Nevertheless, if the supplementary switch configuration can be found within the eight adjoining ones of those four already chosen, it is possible to get both coupled equivalents of that OSC by decomposing the switch configuration which is among those four chosen ones and next to the supplementary switch configuration. Subsequently, this couple can be used for equivalent combination.

B. Example

For convenience, an example with the situation that the input voltage space vector \vec{v}_i , the reference rotation vectors \vec{U} and \vec{V} are all located in Sector I is given to elucidate the substitution process. Firstly, four switch configurations S_{abb} , S_{aab} , S_{aac} and S_{acc} whose vectors are adjacent to the desired \vec{U} and \vec{V} are chosen by the traditional SVM from Table II. Since both the input and the output voltage vectors are situated at the same Sector I, S_{abc} of the OSCs is selected. Then two switch combinations $S_{abc} = S_{acc} + S_{cbc}$ and $S_{abc} = S_{abb} + S_{bbc}$, are available for substitution. Although both of them have one switch configuration within the four selected ones, i.e., S_{acc} and S_{abb} respectively, only the latter combination is chosen since its supplementary switch configuration S_{bbc} lies at the position (a), as shown in Fig. 5, whereas for the former one, i.e., S_{cbc} , is not closely next to the four already selected switch configurations. To include S_{abc} in the switching sequence, the switch configuration S_{aac} which is among the four selected ones and contiguous to the supplementary switch configuration is decomposed into S_{aab} and S_{bbc} with the same duty cycle. The latter together with S_{abb} can then be combined as S_{abc} .

It is important that one portion duty cycle of S_{abb} plus one portion of S_{bbc} is equal to one portion of S_{abc} . Therefore, the duty cycle for the OSC depends upon the minimum duty cycle between its two equivalent switch configurations.

Before the substitution is carried out, the zero vector has to be excluded. This is because when the input voltages are taken into account, the resultant voltage space vectors for the ZSCs and the OSCs exhibit the largest differential in magnitude among all the valid switch configurations due to the different scaling gains in their diagonal matrices \mathbf{D} s. Thus, these two types of switch configurations are not utilized in the same sampling period to avoid large instantaneous output voltage transition. Although it is not mandatory, this treatment will facilitate the switching sequence arrangement, reduce the device switching frequency and the output voltage ripples.

The exclusion of the zero vector is achieved by decomposing the switch configurations which are among the four and the line or column next to the supplementary switch configuration, i.e. S_{acc} and S_{aac} in this example. Thus, it is important to compare the duty cycles for the ZSC and RSCs S_{abb} , S_{acc} and S_{aac} , i.e. d_0 , $d_{\alpha\mu}$, $d_{\alpha\gamma}$ and $d_{\beta\gamma}$ respectively.

1) $d_{\alpha\gamma} > d_0$: If the duty cycle for S_{acc} is larger than that for the ZSC, d_0 part of S_{acc} can be decomposed into switch configurations S_{abb} and S_{bcc} . In other words, the first line switch configurations in Fig. 5, whose equivalent \mathbf{U} vectors point to the position (1), synthesize their continuous $\bar{\mathbf{V}}$ using three switch configurations, whereas the second line switch configurations do that using only two switch configurations. Subsequently, S_{aac} is decomposed to acquire the switch configuration S_{bbc} . Equivalently the OSC S_{abc} can replace the active switch configurations S_{abb} and S_{bbc} with a duty cycle up to their minor amount. Their switching sequences can be arranged as shown in Tables IV and V respectively, with the OSC S_{abc} placed in the centre.

TABLE IV
SWITCHING SEQUENCE WHEN $(d_{\alpha\mu} + d_0) \geq d_{\beta\gamma}$

S_{aab}	S_{abb}	S_{abc}	S_{acc}	S_{bcc}
$d_{\beta\mu} + d_{\beta\gamma}$	$d_{\alpha\mu} + d_0 - d_{\beta\gamma}$	$d_{\beta\gamma}$	$d_{\alpha\gamma} - d_0$	d_0

TABLE V
SWITCHING SEQUENCE WHEN $(d_{\alpha\mu} + d_0) < d_{\beta\gamma}$

S_{aab}	S_{aac}	S_{abc}	S_{acc}	S_{bcc}
$d_{\beta\mu} + d_{\alpha\mu} + d_0$	$d_{\beta\gamma} - d_{\alpha\mu} - d_0$	$d_{\alpha\mu} + d_0$	$d_{\alpha\gamma} - d_0$	d_0

2) $d_{\alpha\gamma} < d_0 \leq (d_{\alpha\gamma} + d_{\beta\gamma})$: In this situation, all S_{acc} and part of S_{aac} are decomposed into their neighboring switch configurations to eliminate the duty cycle for the ZSC. The first line switch configurations in Fig. 5 use the vectors with 120° phase differential to synthesize their $\bar{\mathbf{V}}$ in the input side hexagon. The duty cycle for the part of S_{aac} used to exclude the zero vector is $d_Z = d_0 - d_{\alpha\gamma}$. The remaining of S_{aac} can be decomposed in order to synthesize, together with S_{abb} , the OSC S_{abc} . Based on the comparison results between the duty cycles for the coupled switch configurations, the switching sequences can then be arranged according to Tables VI and VII respectively.

TABLE VI
SWITCHING SEQUENCE WHEN $(d_{\alpha\mu} + d_{\alpha\gamma}) < (d_{\beta\gamma} - d_Z)$

S_{aab}	S_{aac}	S_{abc}	S_{bbc}	S_{bcc}
$d_{\beta\mu} + d_0 + d_{\alpha\mu}$	$d_{\beta\gamma} - d_0 - d_{\alpha\mu}$	$d_{\alpha\mu} + d_{\alpha\gamma}$	d_Z	$d_{\alpha\gamma}$

TABLE VII
SWITCHING SEQUENCE WHEN $(d_{\alpha\mu} + d_{\alpha\gamma}) \geq (d_{\beta\gamma} - d_Z)$

S_{aab}	S_{abb}	S_{abc}	S_{bbc}	S_{bcc}
$d_{\beta\mu} + d_{\beta\gamma}$	$d_{\alpha\mu} + d_0 - d_{\beta\gamma}$	$d_{\beta\gamma} + d_{\alpha\gamma} - d_0$	$d_0 - d_{\alpha\gamma}$	$d_{\alpha\gamma}$

3) $d_0 \geq (d_{\alpha\gamma} + d_{\beta\gamma})$: When the duty cycle for the ZSC is larger than the sum duty cycle for S_{acc} and S_{aac} , all these two switch configurations are decomposed into their neighboring ones. It means that two adjacent vectors with 120° phase shift are employed to synthesize the continuous reference vector $\bar{\mathbf{V}}$ in both lines in Fig. 5. But there still remains duty cycle for the ZSC after the decomposition. In this circumstance, ZSCs are inevitable. No time interval is left for the supplementary switch configuration and thus the OSC is not used. The ZSC bearing the medium input voltage value, i.e. S_{bbb} is used instead to reduce the CMV. The switching sequence can be arranged in Table VIII.

TABLE VIII
SWITCHING SEQUENCE WHEN $d_0 > (d_{\alpha\gamma} + d_{\beta\gamma})$

S_{aab}	S_{abb}	S_{bbb}	S_{bbc}	S_{bcc}
$d_{\beta\mu} + d_{\beta\gamma}$	$d_{\alpha\mu} + d_{\alpha\gamma}$	$d_0 - d_{\alpha\gamma} - d_{\beta\gamma}$	$d_{\beta\gamma}$	$\alpha\gamma$

C. Remarks

As can be seen in Section IV-B, the proposed CMV-reduced SVM divides into five parallel branches.

- $d_0 \leq d_{\alpha\gamma}$ and $d_{\alpha\mu} + d_0 < d_{\beta\gamma}$;
- $d_0 \leq d_{\alpha\gamma}$ and $d_{\alpha\mu} + d_0 \geq d_{\beta\gamma}$;
- $d_{\alpha\gamma} < d_0 \leq d_{\alpha\gamma} + d_{\beta\gamma}$ and $d_{\alpha\mu} + d_0 < d_{\beta\gamma}$;
- $d_{\alpha\gamma} < d_0 \leq d_{\alpha\gamma} + d_{\beta\gamma}$ and $d_{\alpha\mu} + d_0 \geq d_{\beta\gamma}$;
- $d_0 > d_{\alpha\gamma} + d_{\beta\gamma}$.

In each sampling period, the algorithm goes into one and only one branch according to the duty-cycle comparison. The sum of the duty cycles remains unchanged or unity before and after the equivalent decomposition and combination in each branch.

1) *Voltage transfer ratio regions*: As can be seen, these five branches cover all the possible comparison results, or in other words the full range of VTR. The former four branches are used for the case when the duty cycle for the ZSS is small. Small d_0 corresponds to the high VTR region. In contrast, the last branch is used for large d_0 , which corresponds to the case of low VTR region. The transience of both high and low VTR regions can be smoothly achieved by checking whether or not $d_0 > d_{\alpha\gamma} + d_{\beta\gamma}$. This condition leads to the critical line for dividing the high and low VTR regions, which can be expressed as

$$q < \frac{\cos \varphi_i}{2 \cos(\alpha_{sv} - \frac{\pi}{6}) \sin(\theta_{sc} + \frac{\pi}{6})}, \quad (12)$$

where φ_i is the input power factor angle.

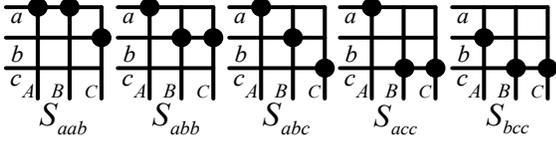


Fig. 6. An example of the switching sequence in Table IV.

2) *Computation overhead*: The proposed algorithm does not actually need to calculate Eq. (12). In comparison with the traditional SVM method, only some more comparison and addition operations are required by the proposed method, as shown in Tables IV-VIII. Therefore, the proposed method has similar computation overhead as the traditional method.

3) *Safe commutation*: In each sampling period, at the most five different switch configurations are used, the same number as the traditional SVM algorithm. Their switching sequences have been properly arranged in Tables IV-VIII to guarantee safe commutation operation. With the situation of Table IV as an example, the switching sequence is shown in Fig. 6. At each commutation instant, the switch configurations change at only one of the output phases. This can also be observed from the subscript changes of the switch configurations.

4) *Voltage and current levels*: Before equivalent substitution, if all switch configurations are chosen from two rows and three columns in Table II, the waveforms of the output voltages consist of two voltage levels, while those of input currents are made of three current levels. Similarly, if all the switch configurations are selected from two columns and three rows, the waveforms of the output voltages and input currents comprise three and two levels respectively. For the former case, the waveforms of the CMV are composed of five voltage levels while the latter three. With the trade-off of the input and output performance, both cases are feasible. It should be emphasized that in some case, for instance when the input and output voltage space vectors are situated in Sector I while the reference input current space vector is in Sector II, two supplementary switch configurations can be found in both the positions (e) and (h). Thus, both switch combinations of S_{abc} can be utilized for equivalent substitution. In this work the switch combination with larger duty cycle for the OSC is used in order to maximize the reduction on the CMV.

5) *Comparison with other CMV-reduced SVM algorithms*: The method using nearest-three-state [23] is valid for VTRs above 0.667, while the method using two vectors with 120° phase shift [20]–[25] decreases the maximum VTR to 0.5. For the VTR gap between 0.5 – 0.667, other methods have to be incorporated for full VTR range applications. Conversely, the proposed algorithm alone covers the whole VTR range.

Further, the method using nearest-three-state [23] uses more switch configurations and needs more complex calculation than the proposed method. By using fewer switching configurations, the switching power losses might be reduced.

Even though the proposed method before equivalent substitution looks similarly with the near-state PWM method [51]–[53], there exist at the least two major differences. The most conspicuous difference is that after equivalent substitution the

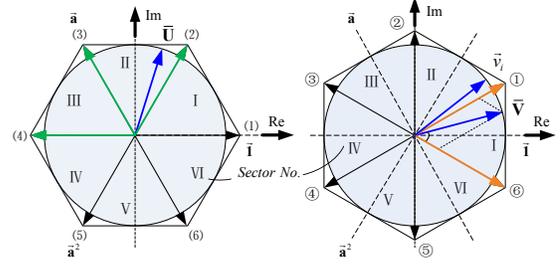


Fig. 7. Another example of vector syntheses with the proposed method.

proposed method might use the OSCs which the near-state PWM never uses. The second difference is that the proposed method chooses the equivalent rotation vectors of switch states according to the comparison of their duty cycles, rather than their vector positions.

To make it clear, another example when the input voltage space vector \vec{v}_i and the direction reference vectors \vec{U} and \vec{V} locate in the sectors shown in Fig. 7 is given. Four RSCs whose equivalent vectors are adjacent to \vec{U} and \vec{V} are chose by the traditional SVM, i.e. S_{aab} , S_{aac} , S_{bab} and S_{cac} . Further, the OSS S_{bac} is chose according to Table III. Therefore, S_{bab} has to be decomposed into S_{aab} and S_{baa} so that S_{baa} together with S_{aac} can combine as the OSS S_{bac} .

If the sum of duty cycles for S_{bab} and S_{cac} is larger than the duty cycle for ZSCs, the S_{bab} is decomposed to its neighbors within the same column. Therefore, three vectors directing to end points (2), (3) and (4) respectively in the output hexagon are used. These vectors are NOT the nearest three vectors of the reference \vec{U} , as can be seen from Fig. 7. On the contrary, the near-state PWM method will choose the nearest three vectors of the reference \vec{U} , i.e. the vectors directing to end points (1), (2) and (3).

If the sum duty cycle for S_{bab} and S_{cac} is smaller than the duty cycle for ZSCs, all S_{bab} is decomposed to its neighbors. Then the proposed method uses two vectors with 120° phase shift to synthesis the reference \vec{U} . These two vector direct to end point (2) and (4) in the output hexagon. As can be seen, the proposed method is different from both the near-state PWM method and the SVM method using two adjacent vectors with 120° phase shift.

V. SIMULATIONS AND EXPERIMENTS

In this section, we study the performance of the proposed proposed CMV-reduced SVM and the traditional SVM via both simulations and experiments. Since we focus on the CMV reduction in this work, the modulation index is set fixed to avoid the interference of constant power loads which will be introduced by the fast feed-forward compensation of the modulation or control strategies [54]. The system parameters used are listed bellow unless otherwise noted:

- three-phase supply with a voltage (RMS) of $110V$ at $50Hz$;
- input filter with capacitors $C_f = 3\mu F$ in delta connection and inductors $L_f = 1mH$;
- output frequency $f_o = 30Hz$;

- three-phase RL load in Y -type connection with $R_o = 50\Omega$ and $L_o = 15mH$;
- sampling period $T_s = 100\mu s$.

For simplicity, the modulation strategies for both the conventional and the proposed methods are set to achieve unit input power factor at the input terminals of the MC [55].

A. Simulation results

The simulations are carried out in *Matlab/Simulink*. The switch array of the MC is constructed using Insulated Gate Bipolar Transistor (IGBT) switches and diodes. The parameters for the IGBTs and diodes are set according to the data-sheet of the real switch module SK60GM123 used in the laboratory prototype.

The performance metrics in terms of CMV peak, RMS and THD for the MCs modulated by both methods are explored and compared. The modulation index is first set as $m = 0.9$ to verify the analysis. As shown in Fig. 8, both methods can maintain a set of sinusoidal and balanced input and output currents. The last subfigures in Fig. 10(a) and Fig. 10(b) shows the CMV waveforms when two SVM methods are applied, where the input phase voltage v_{sa} is also given by red color for easy comparison. The peak value of CMV when the MC is modulated by the proposed method is reduced to 89.8V, in comparison with that of 155.6V when the traditional SVM is used. Therefore, a 42.3% reduction on the peak value of CMV can be achieved. In addition, the RMS of the CMV decreases from 156V for the traditional SVM to 61.5V for the proposed SVM. With closer look at the waveforms, parts of the instantaneous CMV in every switching period are reduced to zero when the proposed method is employed, as can be seen in Fig. 9(b). This phenomenon is not seen in Fig. 9(a) where the traditional SVM is employed. The OSCs are utilized in the former but not in the latter, which explains why the RMS of the CMV is decreased.

For the low VTR applications, the waveforms with the modulation index $m = 0.5$ for both methods are quite similar to their counterparts when $m = 0.9$ is applied, as shown in Fig. 10. In comparison with the traditional SVM, the proposed method reduces the peak value of CMV by the same extent as it is with $m = 0.9$. The RMS of the CMV is decreased by 45.4%, from 114.8V to 62.6V. For the proposed method, the major difference between the situations when $m = 0.9$ and $m = 0.5$ are applied can be seen from the detailed CVM waveforms in Fig. 11, where the OSCs are not used in the latter case and thus zero CMV cannot be seen in each switching period.

The spectra of the CMVs are also shown in Fig. 12. As can be seen, The proposed method has lower fundamental value of CMVs and major harmonic frequencies than the traditional SVM for both $m = 0.9$ and $m = 0.5$.

To compare the performance of both methods for full range of VTR, Fig. 13 shows the THD contents of the input and output currents. The simulations were carried out with the modulation index m varied from 0.3 to 1. The proposed method has lower THD than the conventional SVM method in the output currents, but this situation is reversed in the input currents.

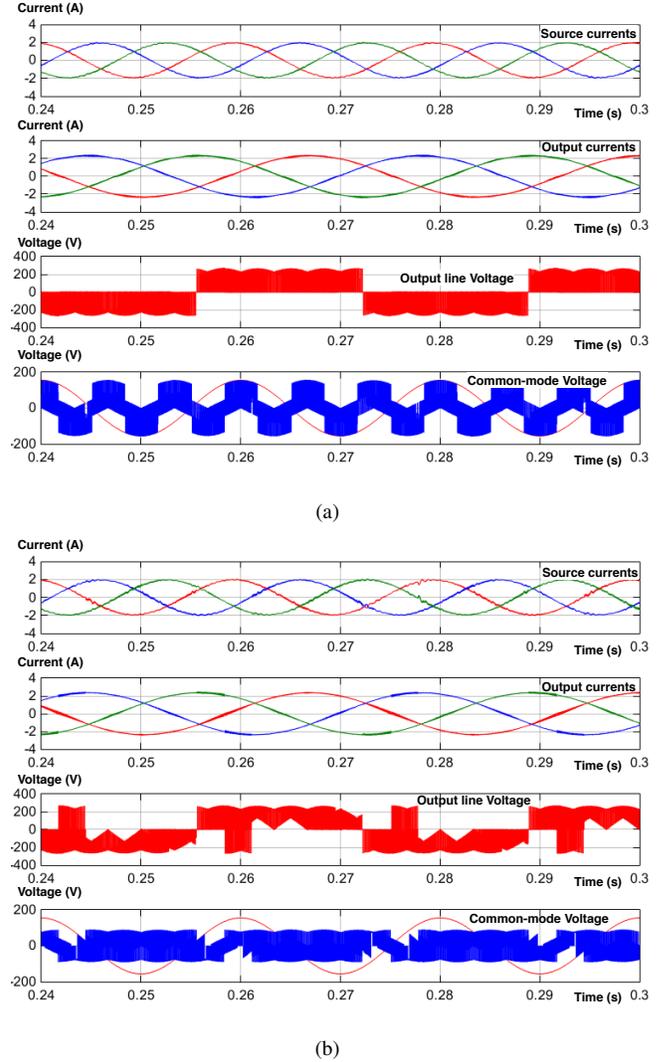


Fig. 8. Simulation waveforms for the MC with (a) the traditional SVM, (b) the proposed SVM employed. Modulation index $m = 0.9$. From top to bottom: the source currents, the output currents, the output line-to-line voltages v_{AB} , the common-mode voltages v_{cm} .

B. Experimental results

Experimental tests are also carried out in a three-phase four-leg MC prototype using its three output legs as shown in Fig. 14. The switch array of the MC consists of 12 bi-directional switch modules SK60GM123 from SEMIKRON. The control platform is composed by a digital signal processor (DSP) TMS320C6713 from Texas Instruments and a field-programmable gate array (FPGA) from Actel. The SVM algorithms are implemented using a development starter kit (DSK) 6713 from Spectrum Digital. The FPGA is used to implement the four-step current commutation [56] and generate the gate drive signals for the insulated-gate bipolar transistors (IGBT). The delay time for each step is set as $T_d = 0.4\mu s$. Ten analog-to-digital channels of 12-bit are also included in the FPGA board for data acquisition. These channels are used to receive the measurement results from the Hall-effect transducers to calculate the instantaneous input voltages, the clamp voltage and the output currents. The input voltage values are captured

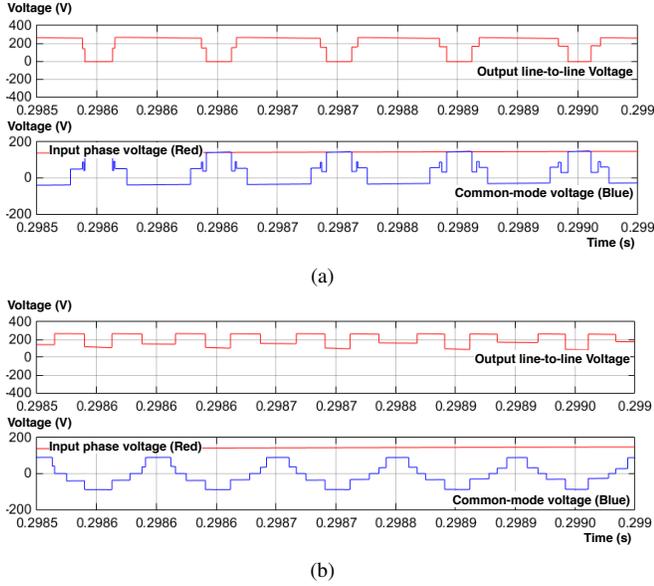


Fig. 9. The enlarged output line-to-line voltage and CMV waveforms of the MC with (a) the traditional SVM, (b) the proposed SVM employed. Modulation index $m=0.9$.

by the DSP to calculate the duty cycle for each switch state while the directions of the output currents are used in the FPGA to complete the commutation.

Fig. 15 shows the waveforms for the converters with $m = 0.9$. Both methods work well to maintain the source and output currents sinusoidal. The RMS of the CMV have been decreased from 149V for the traditional SVM to 62V for the proposed SVM. The peak value of CMV is also reduced from 156V in Fig. 16(a) to 90V in Fig. 16(b). Our proposal outperforms the traditional SVM in generating lower RMS and peak value of CMV. In consistent with the simulation results, the peak value of CMV can be reduced by about 42.3%. Note that ringing effect can be observed in the CMV waveforms due to the inductor at the loads. This effect extends the peak-to-peak value of the CMV. But even taking it into account, the proposed method has smaller CMV peak value than the traditional SVM. As can be seen from the enlarged waveforms of the CMV in Fig. 16, parts of the instantaneous CMV in every switching period are reduced to zero when the proposed method is employed, which can not be observed in the traditional SVM. In addition, the spectra of the CMV in this figure show that the proposed method has lower harmonics than the conventional SVM in the frequency band higher than the sampling frequency.

Similarly, Fig. 17 and Fig. 18 show the performance of the MC when the modulation indices for both methods are set to 0.5. Both methods are able to maintain the input and output currents sinusoidal in the low VTR applications, using the ZSCs rather than the OSCs. As shown in Fig. 18, the zero instantaneous CMV cannot be seen from the zoomed waveforms anymore. In comparison with the traditional SVM, the proposed method reduces the peak value of the CMV by a similar extent as in the situation when the MC is modulated at $m=0.9$. Reductions on the RMS of the CMV, up to 46.1% from 150.7V to 81.2V, can be measured. The ZSC with the

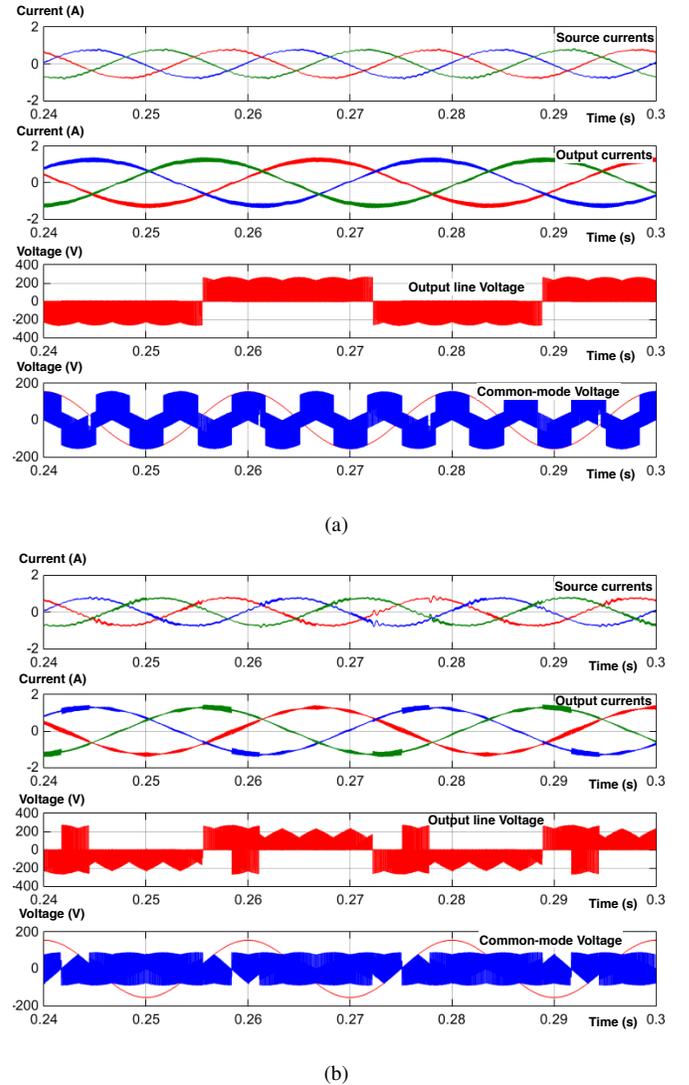


Fig. 10. Simulation waveforms for the MC with (a) the traditional SVM, (b) the proposed SVM employed. Modulation index $m=0.5$. From top to bottom: the source currents, the output currents, the output line-to-line voltages v_{AB} , the common-mode voltages v_{cm} .

intermediate input voltage not only has lower the peak value of CMV, but also makes the transition of the CMV lower. This accounts for the reduction on both the peak value and the RMS of the CMV observed in the proposed SVM. From the figures shown, the FFT analyses of CMV waveforms are also in well accordance with the simulation results.

Further, Fig. 19 is shown to validate that the proposed SVM method can can transit from low to high VTRs or reverse cases. The modulation index m is set as $m = 0.3$ at first and then set as $m = 0.9$ through the host port interface (HPI). The transience is then captured by the oscilloscope. In this circumstance, the input voltage is set to 35V to avoid any possible disruption on the prototype system. As can be seen, during the transience, the modulation strategy maintains both the input and output currents sinusoidal. The transient state can switch smoothly without interruption.

It should be noted that the maximum calculation time used for the traditional SVM and the proposed method are 4660

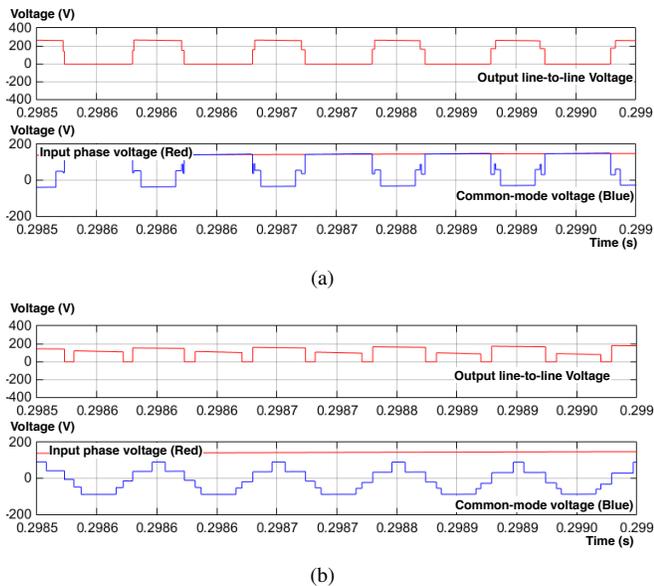


Fig. 11. The enlarged output line-to-line voltage and CMV waveforms for the MC with (a) the traditional SVM, (b) the proposed SVM employed. Modulation index $m=0.5$.

and 4930 timer counts respectively. With respect to the CPU clock rate at 225MHz , the time consumption increases from $82.84\mu\text{s}$ to the $87.64\mu\text{s}$. The difference is acceptable given the sampling period is $100\mu\text{s}$. Therefore, the proposed method needs only similar computation overhead to the traditional SVM.

VI. CONCLUSIONS

A novel SVD-based SVM technique to reduce the common-mode voltage (CMV) at the output side of a matrix converter has been proposed in this work. The reduction is achieved by including either the orientation switch configurations for the case of high voltage transfer ratio (VTR), or the zero switch configurations connecting to the input phase with the medium voltage for the case of low VTR, in the switching sequences. The orientation switch configurations are introduced in by substituting their equivalent switch configurations, without affecting the synthesis of the reference variables. Parts of CMV waveforms during the time intervals for the orientation switch configurations are decreased to zero. Therefore, not only the peak value but also the RMS of the CMV are reduced. The feasibility of the proposed SVM method is substantiated by the simulation as well as the experiment results.

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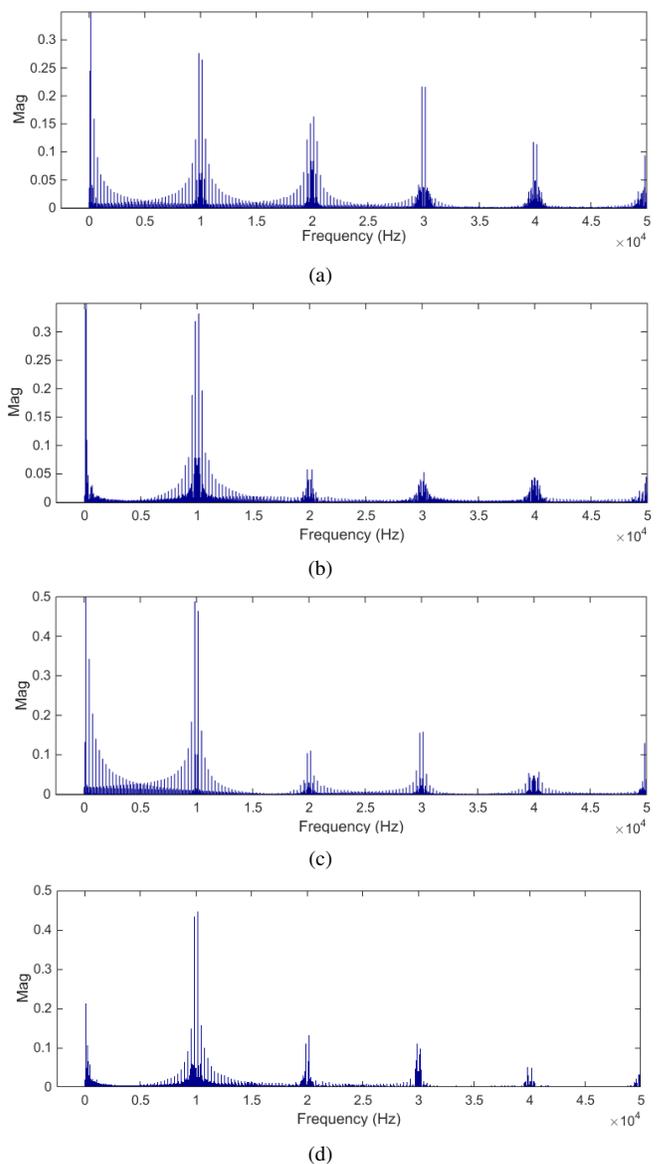


Fig. 12. The spectra of the CMV waveforms for the MC with (a) the traditional SVM and $m=0.9$, (b) the proposed SVM and $m=0.9$, (c) the traditional SVM and $m=0.5$, and (d) the proposed SVM and $m=0.5$ are employed. All magnitude values are calculated with respect to the base value of 100.

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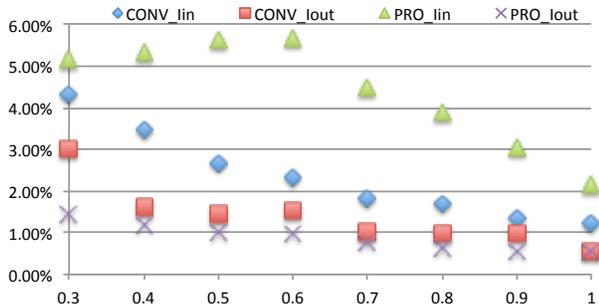
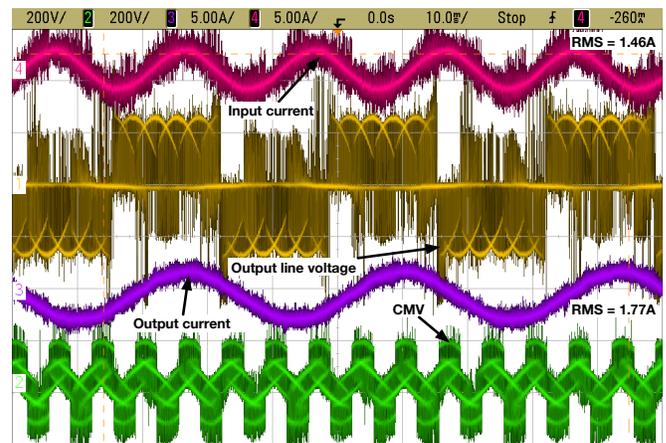


Fig. 13. THD contents of the input and output currents for the proposed and the traditional SVM methods.

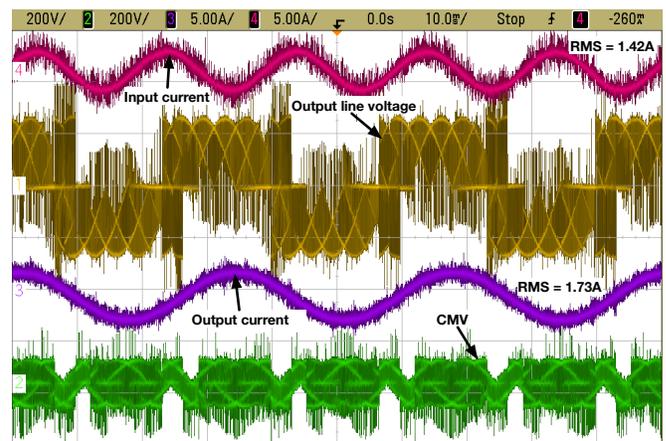


Fig. 14. A direct matrix converter prototype with its control platform.

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(a)



(b)

Fig. 15. Waveforms for the MC with (a) the traditional SVM, (b) the proposed SVM employed. Modulation index $m = 0.9$. From top to bottom: the input current i_a , the output line-to-line voltages v_{AB} , the output current i_A , the common-mode voltages v_{cm} .

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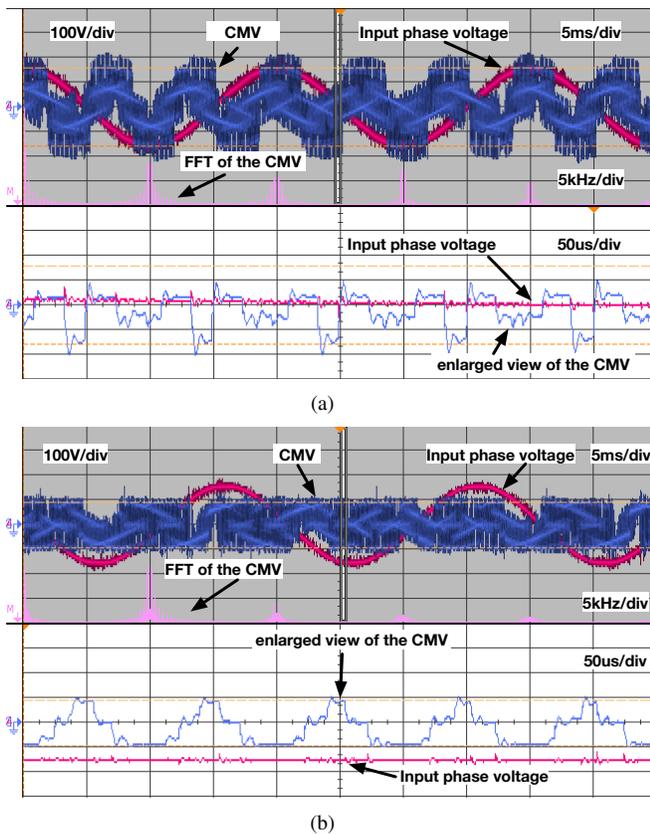


Fig. 16. Detailed CMV waveforms with (a) the traditional SVM, (b) the proposed SVM. Modulation index $m = 0.9$. From top to bottom, the CMV waveforms, the FFT analyses of the CMV waveforms, and the enlarged view of the CMV waveforms.

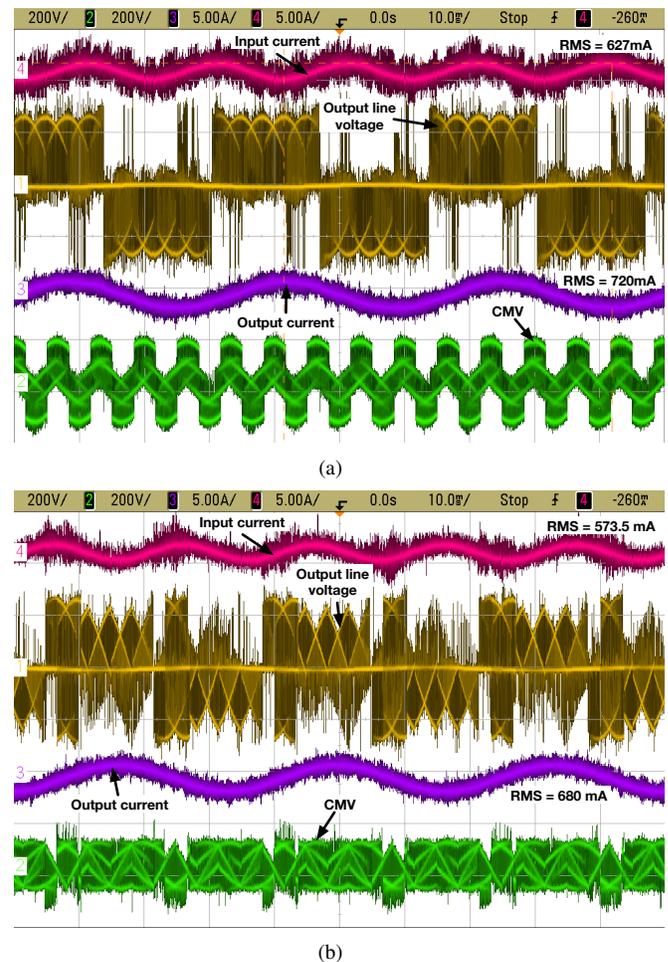


Fig. 17. Waveforms for the MC with (a) the traditional SVM, (b) the proposed SVM employed. Modulation index $m = 0.5$. From top to bottom: the input current i_a , the output line-to-line voltages v_{AB} , the output current i_A , the common-mode voltages v_{cm} .

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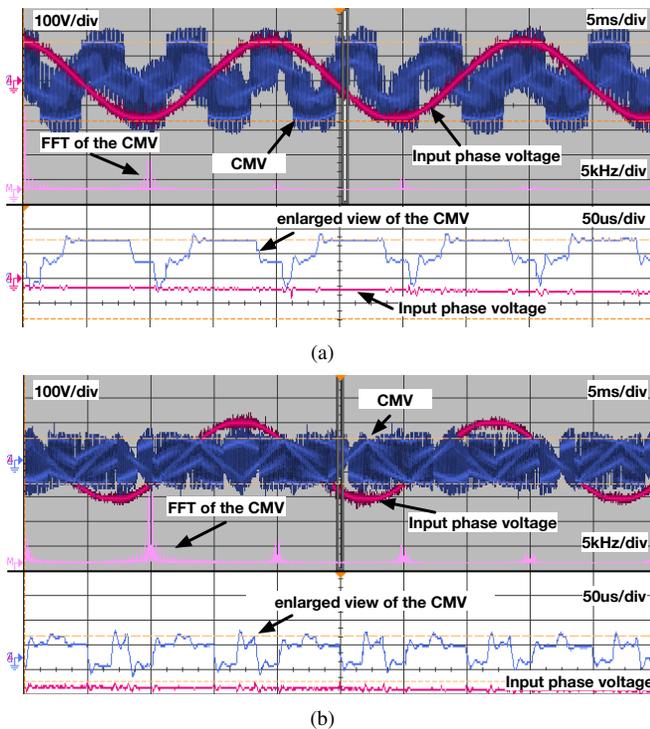


Fig. 18. Detailed CMV waveforms for (a) the traditional SVM and (b) the proposed SVM. Modulation index $m = 0.5$. From top to bottom, the CMV waveforms, the FFT analyses of the CMV waveforms, and the enlarged view of the CMV waveforms.

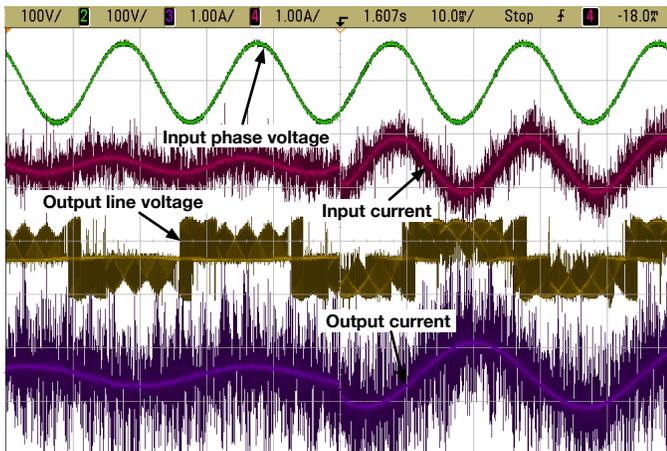
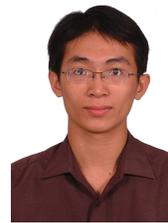


Fig. 19. The transient process of the proposed SVM method from high to low VTR regions. From top to bottom: the input phase voltage v_a , the input current i_a , the output line-to-line voltages v_{AB} , the output current i_A .

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