

# A family of DC-DC converters with reduced MOSFET voltage stress and a high voltage step-up ratio

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**Abstract**—This paper introduces a family of DC-DC converters based on impedance source DC-DC converters. The derived topology is suitable for high voltage step-up ratios. Compared to the typical impedance source DC-DC converters, the proposed topology dramatically reduces the voltage stresses on the power semiconductor devices. In order to suppress the voltage spikes and recycle the leakage inductance energy, the passive-lossless clamp scheme is designed in this paper. The paper presents an analysis of the converter and results from a prototype converter to validate the topology's performance.

**Index Terms**—DC/DC converter,.

## I Introduction

As the ways of delivering the world's electrical energy needs is changing, renewable energy sources are being more widely employed. However, renewable energy sources are generally not directly compatible with the grid, for example PV systems, or even for direct connection to inverters. [1]-[3]. Therefore, high voltage ratio, step-up DC-DC converters are widely used as an interface between the low voltage sources and the inverter [4]. Among the non-isolated converters used the traditional boost converter is a popular choice because of its simple structure [5]. However, if this converter is operated at the extremes of the duty cycles range then the rectifier diode must sustain short pulsed currents with high amplitude when a high voltage gain is required. This operating scenario leads to diode reverse recovery and the electromagnetic interference (EMI) problems. Moreover, the switch suffers from high voltage stress and hence this makes the low resistance MOSFET unavailable. The efficiency will also be lower in high voltage gain applications, it is

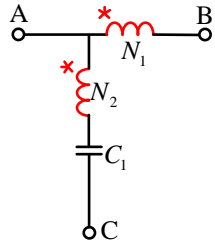
difficult for traditional boost converter to achieve both high voltage gain ratio and high efficiency.<sup>[4]-[6]</sup>

Many topologies have been proposed for high voltage gain applications. These topologies include switched-component techniques (switches-inductor and switched-capacitor), cascaded techniques (output-series and converter-series) and magnetically coupled techniques.<sup>[7]-[12]</sup> Since the Z source impedance network was introduced [13], many impedance networks have been reported for realizing converters with high voltage gain<sup>[14]</sup>. Due to the versatility of the impedance network approach (i.e. DC-DC conversion, DC-AC conversion, AC-AC conversion and AC-DC conversion), it has been used in the high voltage gain application<sup>[15]-[18]</sup>. However the problem with this approach is that the voltage stress on switch is equal to the output voltage, making high performance MOSFET unavailable as well as adding cost and losses to the system

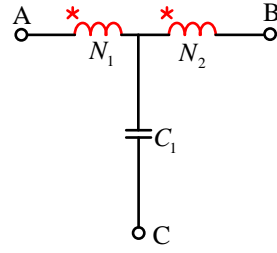
To solve the above concerns, a family of DC-DC converters has been derived from impedance source DC-DC converters for the high voltage gain applications. In this paper one of the resulting topologies is analyzed as an example, theoretical analysis and experimental results are provided to validate the operation of the converter.

## **II Existing X-source network**

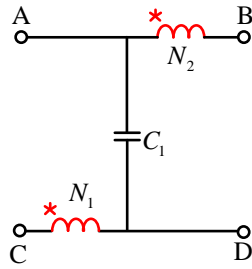
Since the Z source network is presented in 2003<sup>[13]</sup>, various X-source networks have been further developed to provide an efficient means of converting power with a wider range of voltage gain<sup>[14]</sup>. Lots of voltage boosting technology, such as coupled inductor, switched inductor and so on, have also been applied in the X source networks. They typically include  $\Gamma$  source (Fig.1(a)), T source (Fig.1(b)), new type T source (Fig.1(c)), switched coupled inductor Z (SCL-Z) source (Fig.1(d)), basic Z source (Fig.1(e)), switched inductor Z source (Fig.1(f)), switched coupled inductor Z source (Fig.1(g)), Sigma Z source (Fig.1(h)), TZ source (Fig.1(i)), Tau source (Fig.1(j)) and Y source networks (Fig.1(k)).



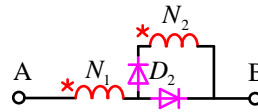
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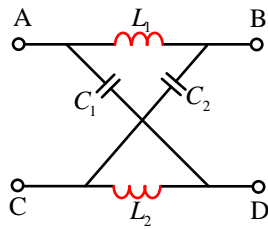
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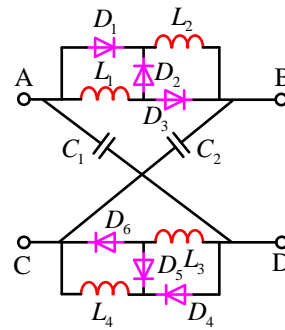
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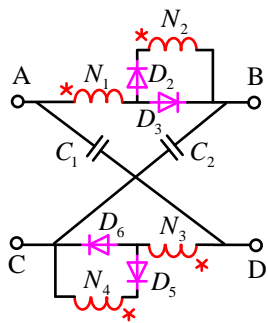
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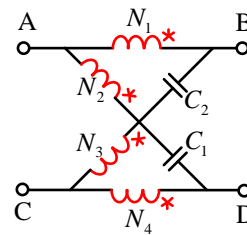
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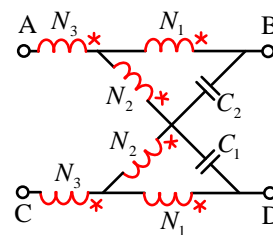
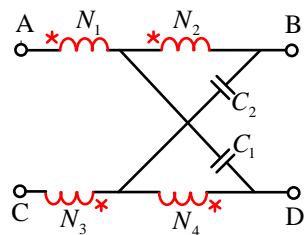
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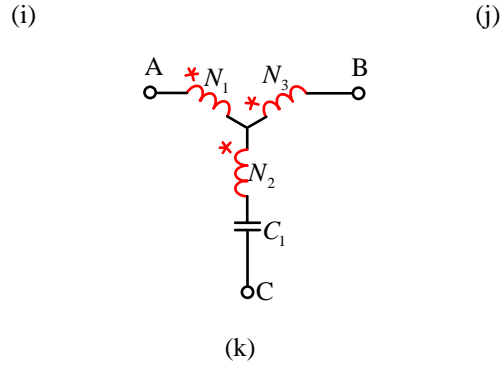


Fig.1 X source networks

### III A family of high step up DC-DC converters stems from X-source network

#### A. X-source DC-DC converters

It is known that the X-source network can be applied to DC-DC, DC-AC, AC-AC and AC-DC power conversion<sup>[13]</sup>. Among four conversion forms, the DC-AC power conversion is the most widely studied.

The DC-DC converters stem from X-source network have recently been studied. By adding the typical boost converter output structure, X source DC-DC converters can be obtained. As shown in Fig.2, Y source DC-DC converter can efficiently boost the low voltage to the high voltage<sup>[15]</sup>.

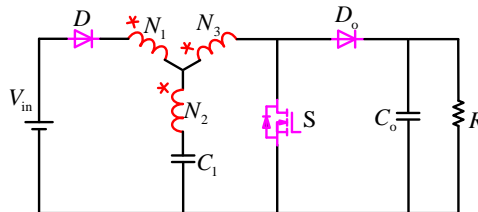


Fig.2 Y source DC-DC converters

The similar methods can be applied to the  $\Gamma$  source network (Fig.3(a)), T source network (Fig.3(b)), new type T source network (Fig.3(c)), switched coupled inductor Z (SCL-Z) source network (Fig.3(d)), basic Z source network (Fig.3(e)), switched inductor Z source network (Fig.3(f)), switched coupled inductor Z source network(Fig.3(g)), Sigma Z source network (Fig.3(h)) , TZ source network (Fig.3(i)) and Tau source network (Fig.3(j)). Then, the X source DC-DC converters can be obtained.

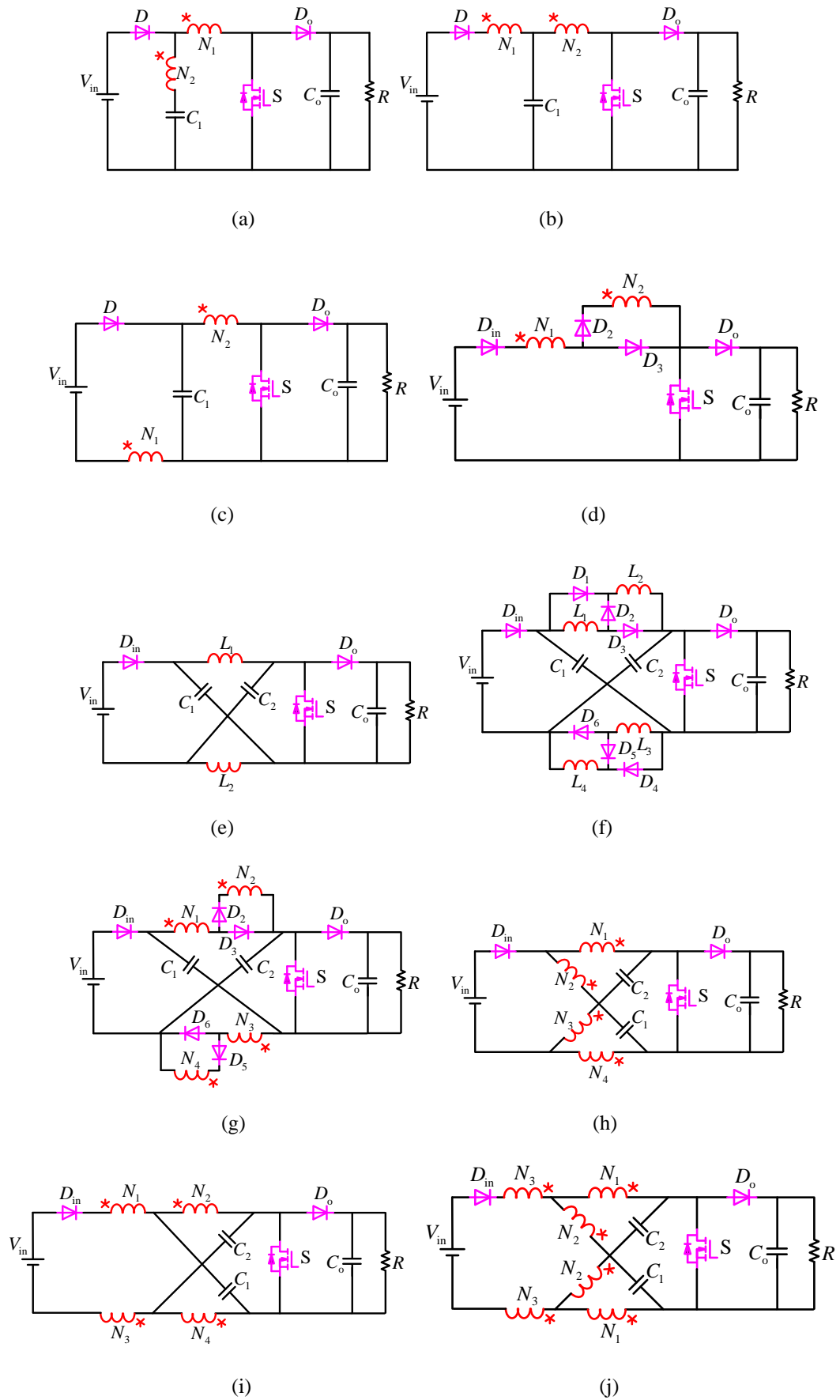


Fig.3 X source DC-DC converters

**B. The existing problems in X-source DC-DC converters**

Based on Fig.3, the generalized X source DC-DC converters structure can be represented as shown in Fig.4 (a). As the voltage stress on the power switch is equal to the output voltage, it is impossible to use the low voltage rated MOSFET. This is not beneficial for the improvement of performance of the converter. Therefore, how to find a way to reduce the voltage stress on the power switch, this is the key point.

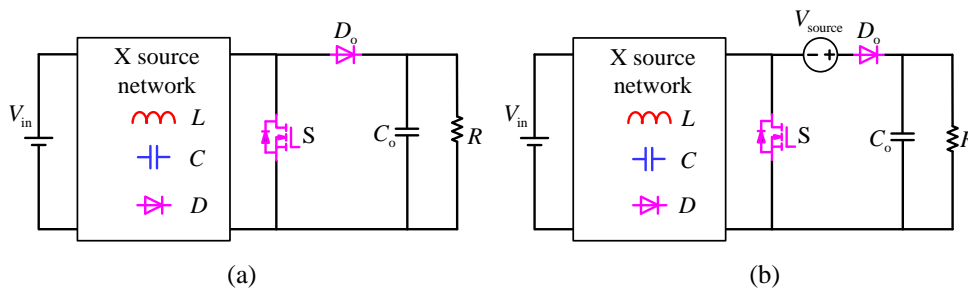
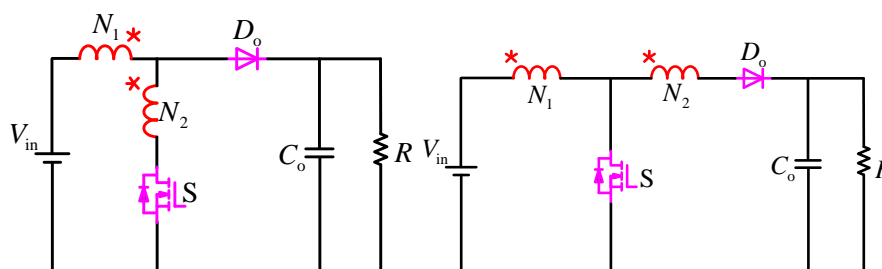


Fig.4 (a) The generalized X source DC-DC converter structure (b) The essence of reducing the voltage stress on the power switch

**C. The deduced high step-up DC-DC converters with reduced voltage stress on MOSFET**

The essence of reducing the voltage stress on the power switch is adding the voltage source between the output capacitor and the power switch as shown in Fig.4 (b). Therefore, in order to make the low voltage rated MOSFET available, the power switch  $S$  in the X source DC-DC converters can be reasonably moved forward, meanwhile, the position of some components need to be changed. Then, a family of basic high step up DC-DC converters can be deduced as shown in Fig.5. According to the basic inductor voltage-second balance principle, Table I shows the gains and switch voltage stresses of converters from Fig.5.



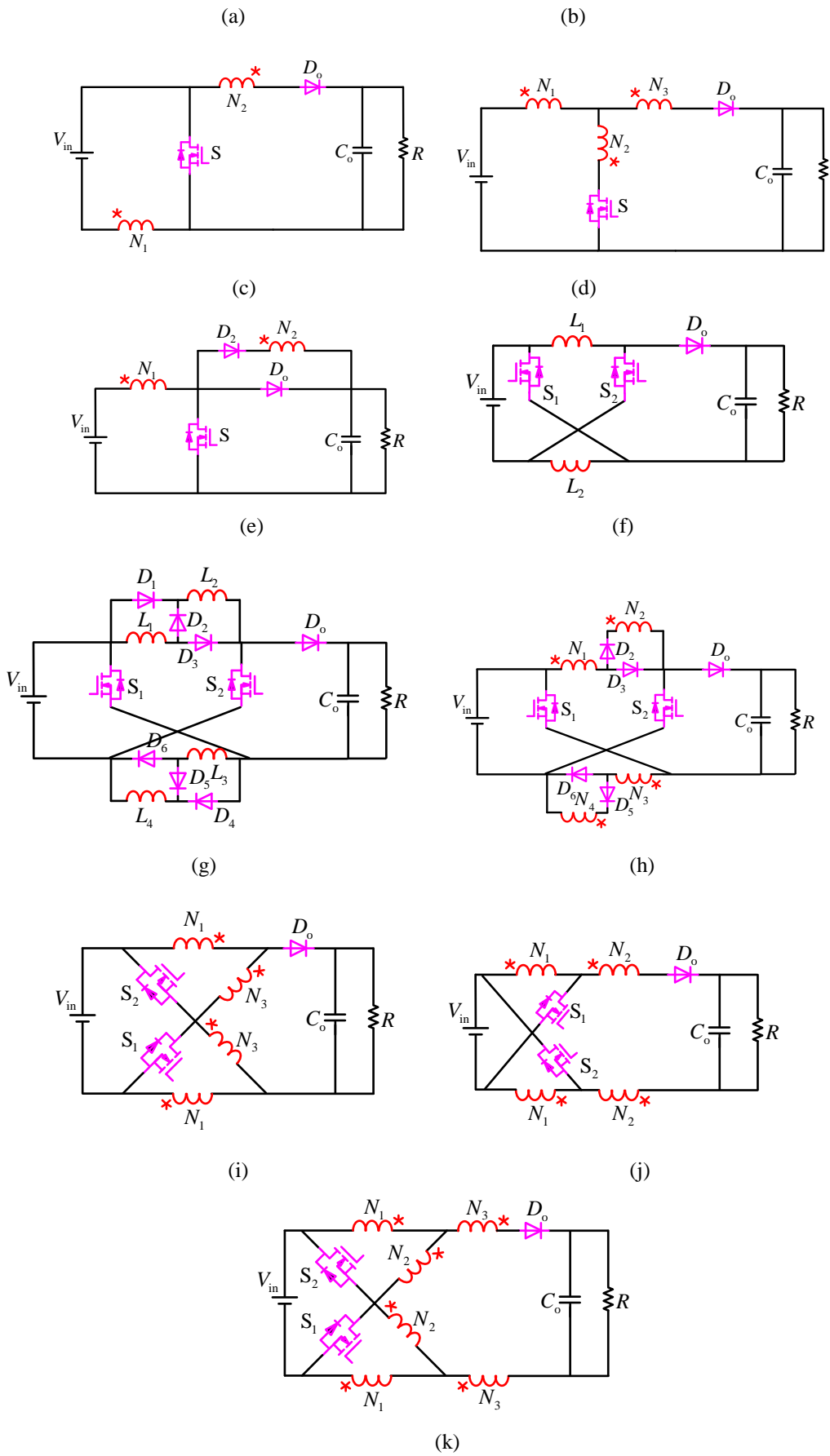


Fig. 5 A family of basic high step up DC-DC converters

Table I Gains and switch voltage stresses of basic converters

Topology	Ideal voltage gain	Ideal voltage stress on the power switch
Fig.4(a)	$\frac{N_1 - N_2 + DN_2}{(N_1 - N_2)(1-D)}$	$\frac{N_1 - N_2}{N_1 - N_2 + DN_2} V_o$
Fig.4(b)	$\frac{1 + DN_2/N_1}{1-D}$	$\frac{V_o}{1 + DN_2/N_1}$
Fig.4(c)	$\frac{1 + DN_2/N_1}{1-D}$	$\frac{V_o}{1 + DN_2/N_1}$
Fig.4(d)	$\frac{(N_1 - N_2) + D(N_2 + N_3)}{(1-D)(N_1 - N_2)}$	$\frac{(N_1 - N_2)V_o}{D(N_2 + N_3) + (N_1 - N_2)}$
Fig.4(e)	$\frac{N_1 + N_2D}{N_1(1-D)}$	$\frac{V_o}{1 + DN_2/N_1}$
Fig.4(f)	$\frac{1+D}{1-D}$	$\frac{V_o}{1+D}$
Fig.4(g)	$\frac{1+3D}{1-D}$	$\frac{(1+D)}{1+3D} V_o$
Fig.4(h)	$\frac{1+(2N_2/N_1+1)D}{1-D}$	$\frac{1+DN_2/N_1}{1+(2N_2/N_1+1)D} V_o$
Fig.4(i)	$\frac{N_1 - N_3 + D(N_1 + N_3)}{(N_1 - N_3)(1-D)}$	$\frac{N_1 - N_3}{N_1 - N_3 + D(N_1 + N_3)} V_o$
Fig.4(j)	$\frac{D(2N_2 + N_1) + N_1}{N_1(1-D)}$	$\frac{N_1}{D(2N_2 + N_1) + N_1} V_o$
Fig.4(k)	$\frac{(N_1 - N_2) + D(N_1 + N_2 + 2N_3)}{(1-D)(N_1 - N_2)}$	$\frac{(N_1 - N_2)V_o}{(N_1 - N_2) + D(N_1 + N_2 + 2N_3)}$

#### IV Operational principle of the proposed converter

In this part, Fig.5 (a) is analyzed in more detail as the representative of the family of basic high step up converters proposed in part II. As the leakage inductor induces high voltage spike on the MOSFET, thus, the diode-capacitor clamped circuit is introduced into the main circuit as shown Fig.6 (a). Fig.6 (b) shows the equivalent circuit of the proposed converter (where  $I = I \sim V$ ). Among Fig.6 (b), the coupled inductor is modeled as the magnetizing inductance  $L_M$ , the leakage inductance  $L_k$  and ideal transformer.

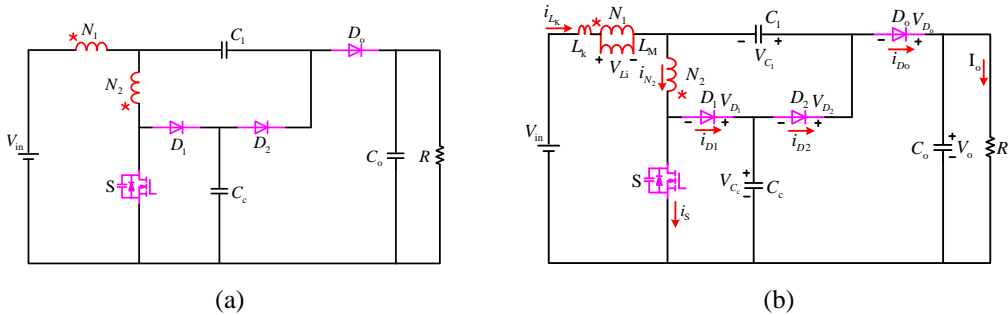




Fig.6 (a) The proposed converter with the clamped circuit, (b) the equivalent circuit of the proposed converter

To simplify the circuit analysis, the following conditions are assumed

(a) Capacitors  $C_1$ ,  $C_c$  and  $C_o$  are large enough that the voltages on them are considered to be constant in one switching period.

(b) The power MOSFET and diodes are treated as ideal, but the parasitic capacitor of the power switch is considered.

(3) The coupling coefficient of the coupled inductor  $K$  is equal to  $L_M/(L_M+L_k)$  and the turns ratio of coupled inductor  $N$  is equal to  $N_1/N_2$ .

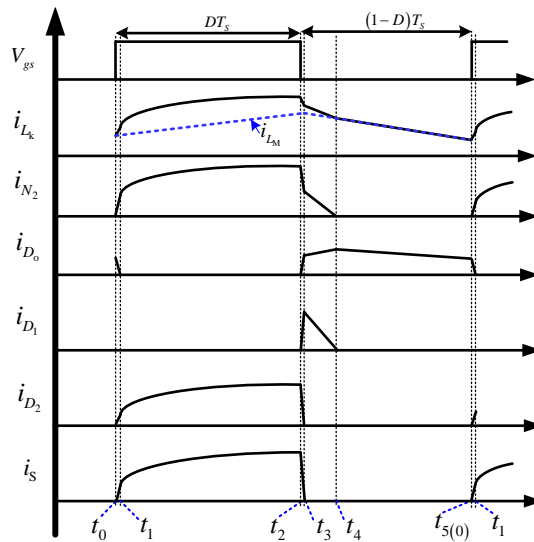


Fig.7 The operational waveforms of the proposed converter

### A.CCM Operation

In the CCM operation, there are five operating modes in one switching period of the proposed converter. Fig.7 shows the operational waveforms and Fig.8 shows the current-flow path of the proposed converter for each modes. Here, the operating modes are described in detail.

Mode I [ $t_0, t_1$ ]: In this transition interval, the switch  $S$  starts to conduct. The diodes  $D_1$  and  $D_2$  are reverse biased. Diode  $D_0$  is forward biased. The current-flow path is shown in Fig.8 (a). The leakage inductance  $L_k$  and magnetizing inductance  $L_m$  are charged by the input source  $V_{in}$ . The leakage inductor current  $i_{L_k}$  increases linearly. The current diode  $i_{D_0}$  decreases. The parasitic capacitor of the

switch S discharges timely. The input source  $V_{in}$ , magnetizing inductance  $L_m$  and capacitor  $C_1$  are in series to provide energy to the output capacitor  $C_o$  and load  $R$ . When the current  $i_{D_o}$  becomes zero, this operating mode ends.

Mode II [ $t_1, t_2$ ]: In this transition interval, the switch is still turned on. Diode  $D_2$  is forward biased. Diodes  $D_1$  and  $D_o$  are reverse biased. The current-flow path is shown in Fig.8 (b). The leakage inductor current  $i_{L_k}$  and secondary-side current  $i_{N_2}$  increase approximately linearly. Meanwhile, the capacitor  $C_1$  is charged by the secondary-side winding  $N_2$  and capacitor  $C_c$ . The output capacitor provides energy to the load. When the switch S is turned off at  $t=t_2$ , this interval is finished.

Mode III [ $t_2, t_3$ ]: In this transition interval, the switch S is turned off. Diodes  $D_1$  and  $D_o$  are reverse biased. Diode  $D_2$  is forward biased. Fig.8(c) shows the current-flow path. The energy of the leakage inductance  $L_k$  is released to the parasitic capacitor of the switch S. The output capacitor provides energy to the load. When the voltage stress on the switch S is equal to the voltage capacitor  $C_c$ , diode  $D_1$  begins to conduct, this mode ends.

Mode IV [ $t_3, t_4$ ]: In this transition interval, the switch S is turned off. Diode  $D_2$  is reverse biased. Diodes  $D_1$  and  $D_o$  are forward biased. The current-flow path is shown in Fig.8 (d). The energy of leakage inductor is transferred into the clamped capacitor  $C_c$ . The input source, magnetizing inductor, and the capacitor  $C_1$  provide energy to the output capacitor  $C_o$  and the load. When the diode current  $i_{D_1}$  decreases to zero at  $t=t_4$ , this mode ends.

Mode V [ $t_4, t_5$ ]: In this transition interval, the switch is turned off. Diodes  $D_1$  and  $D_2$  are reverse biased. Diode  $D_o$  is forward biased. The current-flow path is shown in Fig.8 (e). The input source, magnetizing inductor together with blocking capacitor  $C_1$  provide energy to the output capacitor  $C_o$  and the load. When the switch S begins to conduct at  $t=t_5$ , the new switching period begins.

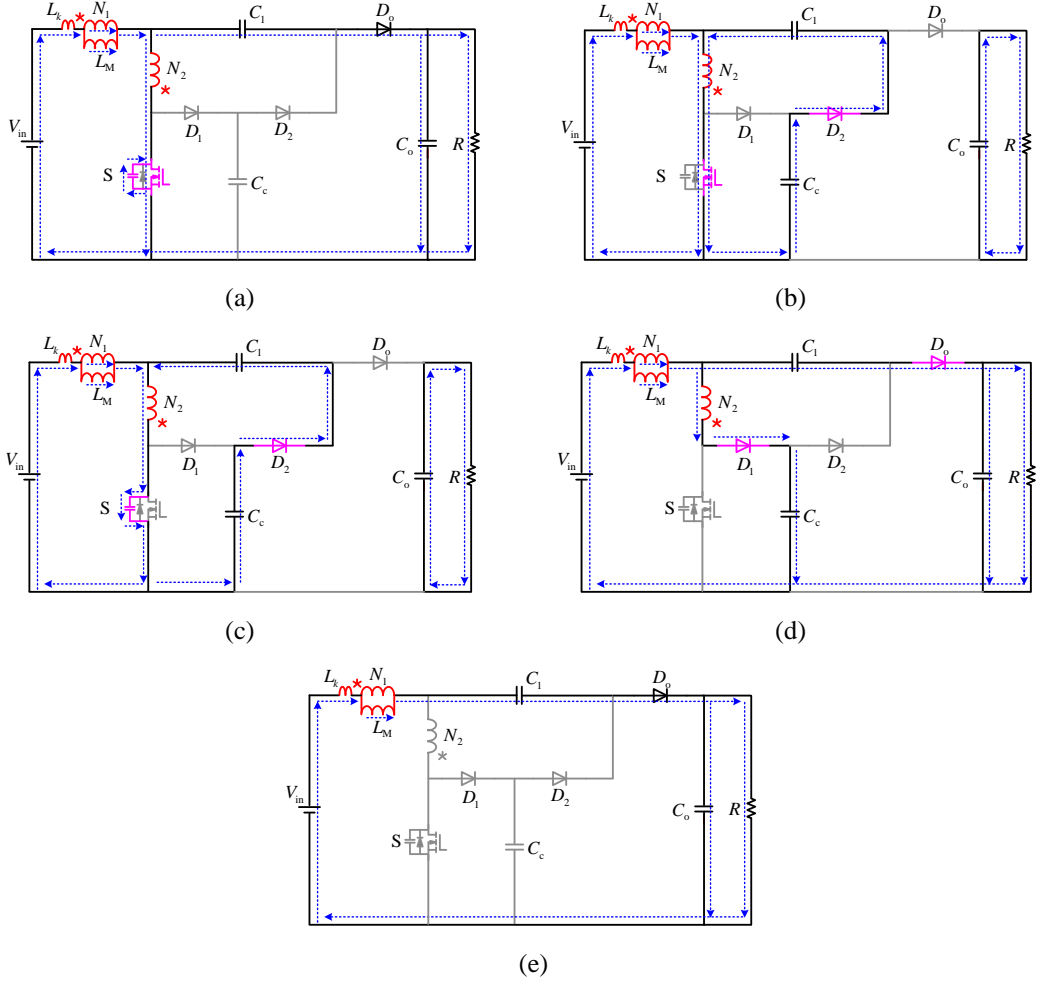


Fig.8 The operational modes of the proposed converter. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

## V Performance analysis of the proposed converter

### A. Voltage gain expression

When the proposed converter operates in CCM mode, since the time durations of modes I and III is very transient, therefore, the two modes are neglected. During the time duration of mode II, the following equations can be expressed based on Fig.8 (b),

$$V_{LII} + \frac{1-K}{K} V_{LII} - \frac{N_2}{N_1} V_{LII} = V_{in} \quad (1)$$

$$V_{C1} = V_{Cc} + \frac{N_2}{N_1} V_{LII} \quad (2)$$

During the time duration of mode IV, the following equation can be derived as,

$$V_{LIV} + \frac{1-K}{K} V_{LIV} - \frac{N_2}{N_1} V_{LIV} + V_{Cc} = V_{in} \quad (3)$$

During the time duration of modes IV and V, the following expression can be written as,

$$V_{LV} + \frac{1-K}{K}V_{LV} - V_{C1} + V_o = V_{in} \quad (4)$$

By applying the volt-second balance principle on magnetizing inductor  $L_M$ , the following equation is given,

$$\int_0^{DT_s} V_{Lm} dt + \int_{DT_s}^{T_s} V_{LV} dt = 0 \quad (5)$$

And substituting (1) and (3) into (4), collecting the terms, the voltage expressions of capacitor  $V_{Cc}$  and  $V_{LV}$  are obtained as

$$V_{Cc} = \frac{1}{1-D} V_{in} \quad (6)$$

$$V_{LV} = \frac{V_{in} D}{\frac{1}{K} - \frac{N_2}{N_1}} * \frac{-1}{1-D} \quad (7)$$

From (1), (2) and (6), the voltage stress on the capacitor  $C_1$  can be obtained as

$$V_{C1} = V_{in} \left( \frac{1}{1-D} + \frac{KN_2}{N_1 - KN_2} \right) \quad (8)$$

Finally, based on the equations (4), (7) and (8), the voltage conversion gain can be computed as

$$M = \frac{1}{1-D} + \frac{1}{1-D} * \frac{N_1}{N_1 - KN_2} \quad (9)$$

The schematic of the voltage gain versus the duty cycle under various coupling coefficients is shown in Fig. 9. It is seen that as the K decreases, the voltage gain increases. When K is equal to 1, the ideal voltage gain is written as

$$M = \frac{2N-1}{(1-D)(N-1)} \quad (10)$$

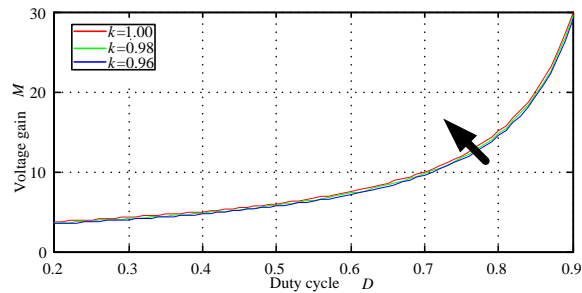


Fig.9 The effect of the coupling coefficient on the voltage gain under N=2

Fig.10 shows the ideal voltage gain comparison versus the duty ratio and turns ratio of the proposed converter as compared with the converters in previous papers [4] and [7]. As the turns ratio  $N$  decreases, the voltage conversion gain increases dramatically. This performance is contrary to other high step up DC-DC converters.

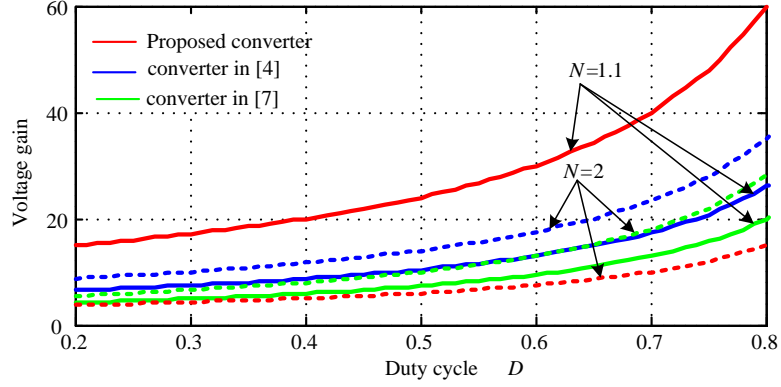


Fig.10 Voltage gain comparison versus duty cycle and turns ratio of the proposed converter

### B. Voltage stress analysis

According to the above analysis, the voltage stresses across the switch S and diodes are derived from

$$V_s = V_{D_1} = \frac{1}{1-D} V_{in} \quad (11)$$

$$V_{D_o} = V_{D_2} = \frac{N}{(1-D)(N-1)} V_{in} \quad (12)$$

The voltage stresses on the power switch S and diodes related to the output voltage and turns ratio can be expressed as

$$V_s = V_{D_1} = \frac{N-1}{2N-1} V_o \quad (13)$$

$$V_{D_o} = V_{D_2} = \frac{N}{2N-1} V_o \quad (14)$$

The relationship between the normalized voltage stresses on the semiconductor components and the turns ratio  $N$  is illustrated in Fig. 11. As the turns ratio decreases (voltage gain increases), the voltage stresses of switch S and diode  $D_1$  also decrease. Although the voltage stresses of diodes  $D_2$  and  $D_o$  are increased, it is below the output voltage.

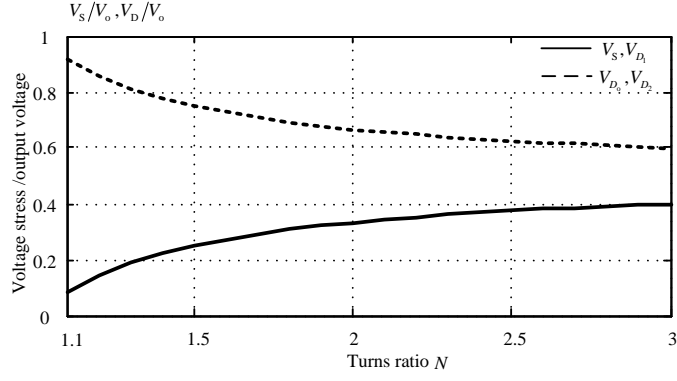


Fig. 11 The normalized voltage stresses on the semiconductor components

### C. Current stress analysis

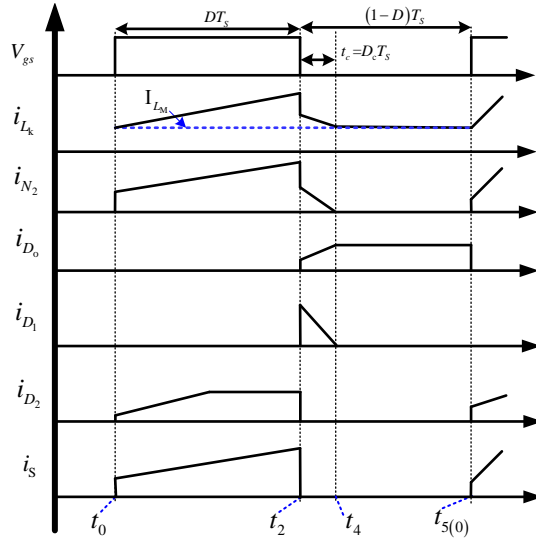


Fig. 12 The simplified waveforms of the proposed converter

In order to simplify the current calculation, the extremely short time interval  $[t_0 - t_1]$  and  $[t_2 - t_3]$  is neglected. The magnetizing current is considered to be a constant as the magnetizing inductance  $L_M$  is large enough. Other parasitic factors are also ignored. The simplified waveforms are shown in Fig.12.

According to the current balance law, the average currents of the output diode  $D_o$  and diode  $D_2$  in its turn on condition are,

$$I_{D_o[t_2, t_5]} = I_o / (1 - D) \quad (15)$$

$$I_{D_2[t_0, t_2]} = I_o / D \quad (16)$$

Based on the charge balance principle of capacitor  $C_c$ , the time interval  $t_{24}$  and  $t_{45}$  can be derived

as

$$t_{24} = t_c = \frac{2(1-D)(N-1)}{2N-1} T_s \quad (17)$$

$$t_{45} = \frac{(1-D)}{2N-1} T_s \quad (18)$$

Thus, according to the current balance law, the average current of the clamped diode  $D_1$  in its turn on condition is:

$$I_{D_1[t_2, t_4]} = \frac{I_o(2N-1)}{2(1-D)(N-1)} \quad (19)$$

During the time interval  $[t_2, t_5]$ , while using KCL, at junction points of the primary side  $N_1$  of the coupled inductor, the secondary side  $N_2$  of the coupled inductor, and multiplier capacitor  $C_1$ , the average current of the leakage inductor can be written as

$$I_{L_k[t_2, t_5]} = \frac{2I_o}{1-D} \quad (20)$$

According to the magnetic flux conservation principle and Fig.12, the following expression can be deduced

$$N_1 I_{L_k[t_0, t_2]} - N_2 I_{N2[t_0, t_2]} = N_1 I_{L_k[t_2, t_5]} - N_2 I_{N2[t_2, t_4]} \quad (21)$$

Meanwhile,

$$I_{N2[t_0, t_2]} = I_{L_k[t_0, t_2]} + I_{D_2[t_0, t_2]} \quad (22)$$

Collecting the terms,  $I_{N2[t_0, t_2]}$  can be computed as

$$I_{N2[t_0, t_2]} = I_o \frac{D(2N^2 - 4N + 1) + 2N(N-1)}{2D(1-D)(N-1)^2} \quad (23)$$

Then, the RMS value of switch S is,

$$I_{\text{RMS-S}} = \sqrt{\frac{1}{T_s} \int_0^{DT_s} \left( I_{N2[t_0, t_2]} - 0.5\Delta I_L + \frac{\Delta I_L}{DT_s} t \right)^2 dt} = \frac{D(2N^2 - 4N + 1) + 2N(N-1)}{2D(1-D)(N-1)^2} I_o \sqrt{D} \sqrt{\frac{K^2}{12} + 1} \quad (24)$$

Where  $K$  is the coefficient of inductor current ripple ( $\Delta I_L = KI_{L_k[t_0, t_2]}$ ).

#### ***D. The effect of parasitic parameters on the voltage gain***

In fact, the winding resistances of the coupled inductor, the conduction resistors of switch, and diode forward voltage have a little impact of the voltage gain. To simplify voltage gain analysis affected by the parasitic parameters, the leakage inductance is taken as zero. The primary sides and secondary sides of coupled inductors are equaled to  $R_{N1}$  and  $R_{N2}$ , respectively. The conduction resistor of switch is equaled

to  $R_s$ . The diode forward voltage is equaled to  $V_d$  and the resistors of diodes are equaled to  $R_d$ . Fig.13 shows the simplified circuit affected by the parasitic parameters of proposed converter, where  $t_j$  is represented by  $t_0, t_2, t_4, t_5$ .<sup>[19]</sup>

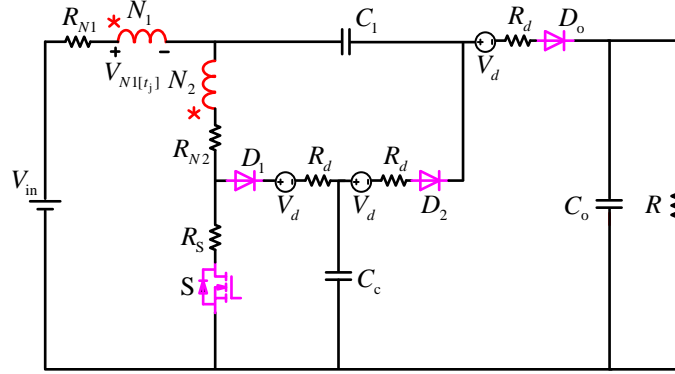


Fig.13 Simplified circuit for voltage gain analysis affected by parasitic parameters

From Fig.13 and Fig.12, when the switch is turned on, during the time interval  $[t_0, t_2]$ , the voltage

across the winding  $N_1$  can be expressed as

$$V_{N1[t_0, t_2]} = \frac{V_{in} - R_{N1}I_{N1[t_0, t_2]} - (R_{N2} + R_S)(I_{N1[t_0, t_2]} + I_{D2})}{1 - N_2/N_1} \quad (25)$$

Meanwhile,

$$V_{C1} = \frac{N_2}{N_1}V_{N1[t_0, t_2]} + V_{Cc} - V_d - R_d I_{D2} - (R_{N2} + R_S)(I_{N1[t_0, t_2]} + I_{D2}) \quad (26)$$

When the switch is turned off, the voltage across the winding  $N_1$  can be expressed as

$$V_{N1[t_2, t_5]} = \frac{V_{in} - V_d - V_{Cc} - R_{N1}I_{N1[t_2, t_5]} - (R_{N2} + R_d)I_{N1[t_2, t_4]}}{1 - N_2/N_1} \quad (27)$$

$$V_{N1[t_2, t_5]} = V_{in} - V_o - V_d + V_{C1} - R_d I_{D0} - R_{N1}I_{N1[t_2, t_5]} \quad (28)$$

Combining (25)-(28), and collecting terms, then the voltage gain can be obtained as

$$M_{pa} = \frac{\frac{2N-1}{(1-D)(N-1)} - 3\frac{V_d}{V_{in}}}{1 + R_{N1}A + (R_{N2} + R_S)B + (R_{N2} + R_d)\frac{2N-1}{2R(1-D)(N-1)} + R_d\frac{1}{DR(1-D)}} \quad (29)$$

Where,



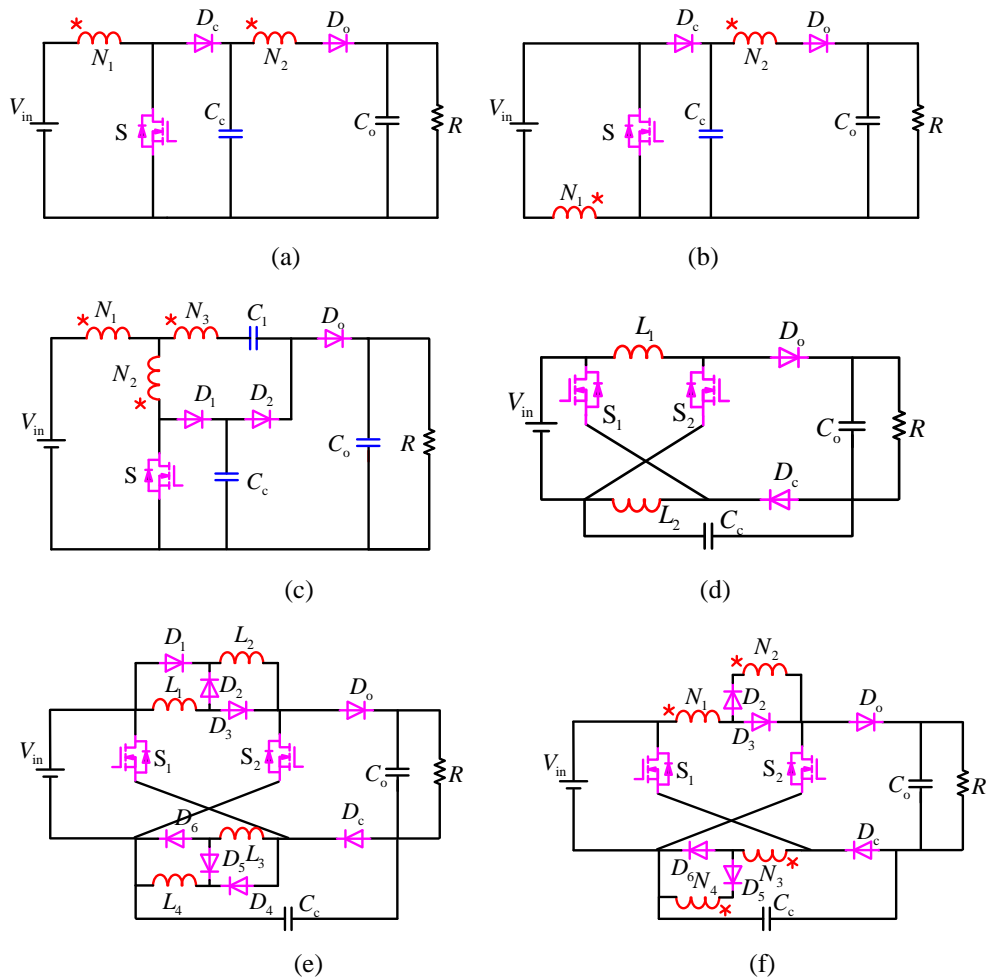
$$A = \frac{(2ND - 2D + 1)(D(4N^2 - 8N + 3) + 2(N - 1))}{2DR(1 - D)^2(N - 1)^3} + \frac{4}{R(1 - D)}$$

$$B = \frac{N(D(4N^2 - 8N + 3) + 2(N - 1))}{2DR(1 - D)(N - 1)^3} + \frac{N}{R(N - 1)D} + \frac{(2N - 1)(D(2N^2 - 4N + 1) + 2N(N - 1))}{2R(1 - D)^2(N - 1)^3}$$

It can be seen that the voltage gain is affected by the parasitic parameters including resistors and diode forward voltage. Once the circuit components are ideal, expression (10) can be obtained. In fact, the parasitic resistors of the circuit component are rather smaller than the output resistor. Therefore, their impact on the voltage can be ignored in practical circuit design.

### VI Leakage energy solution of other converters

The passive-lossless clamp scheme can be employed for other deduced converters in part II as shown in Fig.14. With the simple but effective passive lossless circuits, the leakage energy is recycled and the voltage spikes are absorbed. So the efficiency of the converter is improved<sup>[20]</sup>.



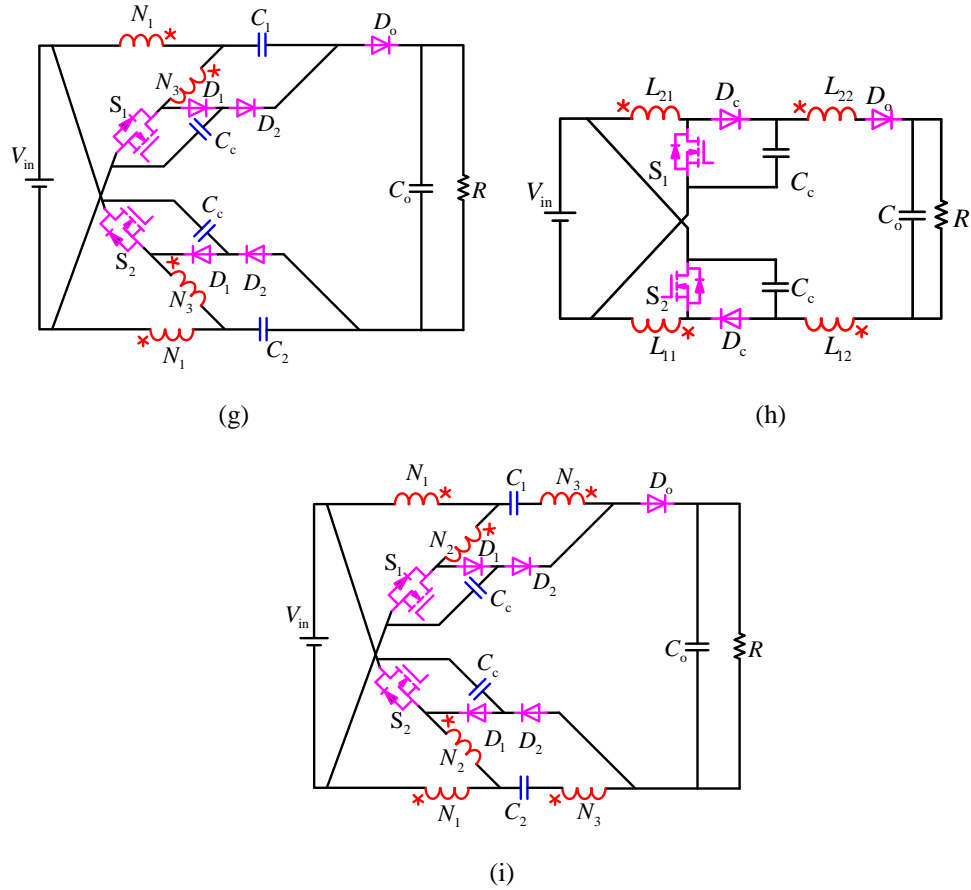


Fig.14 A family of basic high step up DC-DC converters with passive lossless circuits

### VII Experimental verification

A 400W prototype converter with high step up ratio has been implemented and tested. Table I shows

the specifications and circuit components, respectively, used in the proposed converter.

TABLE I System specifications of the proposed converter

Input voltage $V_{in}$	48V
Output voltage $V_o$	380V
Rated power $P_o$	400W
Switching frequency $f_s$	50kHz
MOSFET Switches $S$ ,	IRFP4668
Diodes $D_o, D_{c1}, D_{c2}$	VF30200, MUR460, IDH08G65C5
Output capacitor $C_o$	470 $\mu$ F
Capacitor $C_c, C_{c1}$	12.4 $\mu$ F , 8.8 $\mu$ F (several capacitors in parallel)
Coupled inductors	EE55, $N_p : N_s = 30 : 16$ ,

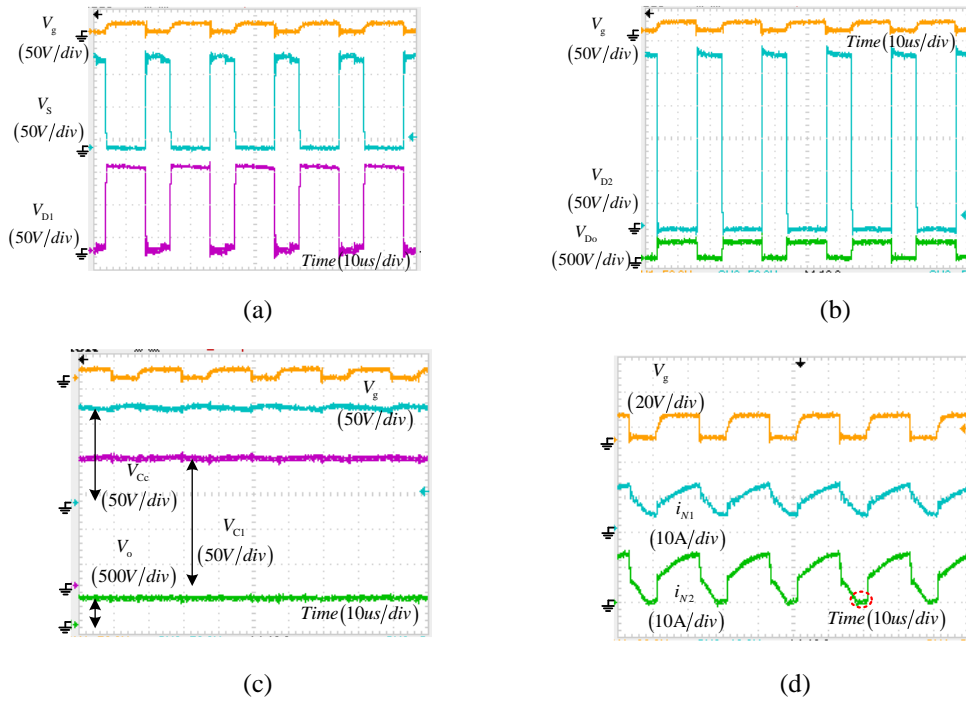
Fig.15 (a) shows the experimental waveforms of driver signal  $V_g$ , voltage stresses on switch  $S$  and diode  $D_1$ ,  $V_s$  and  $V_{D1}$ . Although the leakage inductance of the coupled inductor can induce voltage spike on the switch  $S$ , the voltage  $V_s$  is clamped about 130V. This makes the low resistance MOSFET available.

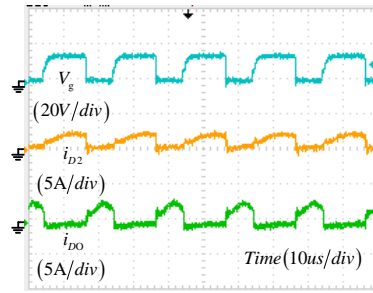
Thus, it is beneficial for the efficiency improvement. The voltage  $V_{D1}$  is also about 130V. Fig. 15 (b) shows the measured waveforms of  $V_{D2}$  and  $V_{D0}$ . The voltage stresses on them is about 260V. Fig. 15 (c) shows the experimental waveforms of all the capacitors. The voltage stresses,  $V_{Cc}$ ,  $V_{C1}$  and  $V_o$  are respectively about 130V, 180V and 380V. Fig. 15 (d) and (e) show the experimental waveforms of currents  $i_{N1}$ ,  $i_{N2}$ ,  $i_{D2}$  and  $i_{D0}$ . They are all corresponding to the theoretical analysis. In addition, as shown in Fig. 15 (d), the current  $i_{N2}$  decreases to zero naturally. It means there is no reverse recovery problem in diode  $D_1$ .

TABLE II Comparison of RMS current  
between theoretical value and experimental value

S1 Duty cycle	Theoretical value	Experimental value
0.5	6.9	7.1
0.62	8.3	8.7
0.7	10	10.5

The experimental RMS of the power switch current is in contrast to the theoretical value based on equation (24), as shown in Table II. Because of parasitic parameters, measurement error and so on, they are not absolutely the same. But, equation (24) can still be a good reference for choosing the switch.





(e)

Figs. 15 Experimental waveforms of the proposed converter

The efficiency of the proposed converter measured per 50W is illustrated in Fig.16. The maximum efficiency is about 96.5%.

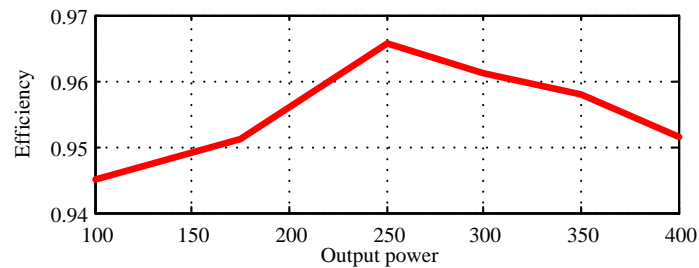


Fig.16 Test efficiency of the proposed converter

### VIII Conclusion

In this paper, a family of DC-DC converters is deduced from impedance source DC-DC converters for high step up conversion. The voltage ratio characteristic of impedance source converters is used in the proposed converters, and the shortcomings of the impedance source converters, i.e. high voltage stress on mosfet, are avoided. The voltage stresses on the switches in the proposed converters are greatly reduced. In addition, in order to suppress the voltage spike induced by the leakage energy, the passive clamp circuit is applied. Therefore, it makes the low resistance mosfet available, and the efficiency is improved. At last, the experiment results verify the theoretical analysis.

### REFERENCES

- [1] Y. Tang, D. J. Fu, T. Wang, and Z. W. Xu, "Hybrid Switched-Inductor Converters for High Step-Up Conversion," *IEEE Trans. Ind. Electron.*, vol.62, no. 3, pp. 1480-1490, Mar. 2015.
- [2] C.T. Pan and C. M. Lai, "A High-Efficiency High Step-Up Converter With Low Switch Voltage

- Stress for Fuel-Cell System Applications,” *IEEE Trans. Ind. Electron.*, vol.57, no. 6, pp. 1998-2006, Jun. 2010.
- [3] C.T. Pan, C. F. Chuang and C. M. Lai, “A Novel Transformerless Interleaved High Step-Down Conversion Ratio DC–DC Converter With Low Switch Voltage Stress,” *IEEE Trans. Ind. Electron.*, vol.61, no. 10, pp. 5290-5299, Oct. 2014.
- [4] X. F. Hu, G. R. Dai, L. Wang, and C. Gong, “A Three Switching State Boost Converter Mixed with Magnetic Coupling and Voltage Multiplier Techniques for High Gain Conversion”, *IEEE Trans. Power Electron.*, Early access. 2015.
- [5] C. M. Lai, C. T. P and M. C. Cheng, “High-Efficiency Modular High Step-Up Interleaved Boost Converter for DC-Microgrid Applications,” *IEEE Trans. Ind. Electron.*, vol.48, no.1, pp. 161-171, Feb. 2012.
- [6] T. J. Liang and J. H. Lee, “Novel High-Conversion-Ratio High-Efficiency Isolated Bidirectional DC–DC Converter”, *IEEE Trans. Ind. Electron.*, vol.62, no.7, pp. 4492-4503, Jul. 2015.
- [7] Ali Ajami, Hossein Ardi, and Amir Farakhor, “A Novel High Step-up DC/DC Converter Based on Integrating Coupled Inductor and Switched-Capacitor Techniques for Renewable Energy Applications”, *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4255 - 4263, August. 2015.
- [8] S. M. Chen, T. J. Liang, L. S. Yang and J. F. Chen, “A Boost Converter With Capacitor Multiplier and Coupled Inductor for AC Module Applications,” *IEEE Trans. Ind. Electron.*, vol.60, no.4, pp. 1503-1511, Apr. 2013.
- [9] W. Li, W. Li, X. Xiang, Y. Hu, X. He, “High Step-Up Interleaved Converter With Built-In Transformer Voltage Multiplier Cells for Sustainable Energy Applications,” *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2829 - 2836, Jun. 2014.

- [10] Y. Tang, and T. Wang, "Study of An Improved Dual-Switch Converter With Passive Lossless Clamping," *IEEE Trans. Ind. Electron.*, vol.62, no.2, pp. 972-981, Feb. 2015.
- [11] C. L. Wei, and M. H. Shih, "Design of a Switched Converter With a Wide Input Voltage Range," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 6, pp. 1648-1656, Jun. 2013.
- [12] Y. P. Hsieh, J. F. Chen, T. J. Liang, and L. S. Yang, "Novel High Step-Up DC-DC Converter With Coupled-Inductor and Switched-Capacitor Techniques," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 998-1007, Feb. 2012.
- [13] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504-510, Mar./Apr. 2003.
- [14] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-Source Networks for Electric Power Conversion Part I: A Topological Review," *IEEE Trans. Power Electron.*, Vol. 30, No. 2, pp. 699-716, Feb. 2015.
- [15] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, S. J. Andreasen, and G. E. Town, "Y-Source Boost DC/DC Converter for Distributed Generation," *IEEE Trans. Industrial Electron.*, Vol. 62, No. 2, pp. 1059-1069, Feb. 2015.
- [16] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "Quasi-Y-Source Boost DC-DC Converter," *IEEE Trans. Power Electron.*, Vol. 30, No. 12, pp. 6514-6519, Dec. 2014.
- [17] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "New Magnetically Coupled Impedance (Z-) Source Networks," *IEEE Trans. Power Electron.*, Early Access, 2014.
- [18] X. P. Fang, "A Novel Z-Source DC-DC Converter," *IEEE International Conference on Industrial Technology, ICIT 2008*.
- [19] A. Ioinovici, *Power Electronics and Energy Conversion Systems (Volume 1)*, John Wiley @ Sons,

2013.

- [20] Q. Zhao and F. C. Lee, "High- Efficiency, High Step-Up DC-DC Converters," *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 65–73, Jan. 2003.