A Current Source Inverter with Series Connected AC Capacitors for Photovoltaic Application with Grid Fault Ride Through Capability

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***Abstract*- The current source inverter (CSI) is preferred to interface a renewable source such photovoltaics (PV) to the AC power grid because it can provide smooth current source in the DC side, which fits to the PV behaviour and also steps-up the voltage from DC side to AC side, which allows smaller and safer DC voltage levels to be used. However, the CSI has the problem that during an AC grid fault, it cannot operate properly. In this paper, a single-stage power conversion approach based on a CSI inverter with series capacitors is proposed, proven to provide improved efficiency and smaller DC inductor size and the capability to ride through AC grid faults with full reactive power injection support when compared to a standard CSI.**

I. INTRODUCTION

In order to feed the DC power generated by a renewable energy source such a Photovoltaic (PV) into the AC power network, a DC/AC power inverter is needed. However, besides providing a high conversion efficiency, the inverter should meet also two additional requirements: the ability to adapt to the change in the DC voltage generated by the renewable energy source and the capability of ride through grid faults such as deep voltage sags and power interruptions, whilst providing reactive power support to the grid.

The first requirement is a consequence of the basic V-I characteristics of a PV illustrated in Fig. 1, that makes that the higher power to be delivered when the voltage across its terminals is lower than the maximum (no-load) voltage. The ratio between maximum power voltage and no load voltage for a PV is typically within a range of 0.7-0.8. If the PV load resistance is varied from infinite to zero, the generated power level initially increases according to the increase in the load current that also causes a fall in the PV terminal voltage: zero power at no-load which is where the terminal voltage is maximum (OP1), then smaller and higher power at light load (OP2) and higher load (OP3) and finally reaching the maximum power point MPP (OP4). After reaching the MPP, the power generated reverses its trend (OP5 and OP6) and even becomes zero again when short-circuiting the PV terminals (OP7).

This complex V-I-P behavior may be accommodated by a few alternative power converter topologies analyzed in [1]-[5]. The first solution may use a nonisolated DC/DC converter to boost the low voltage at DC side (PV) to a higher sufficient level for a DC/AC inverter. Since the DC/DC converter does not provide galvanical isolation, additional precaution should be used to ensure the safety regulation and to withstand any potential EMI [3]. Second solution is to add galvanic isolation by using a high switching frequency transformer in the DC/DC converter. As it has small size, very high efficiency (99%) and the possibility to then match to the standard semiconductor voltage/current ratings, it enabled a wide spread of this solution. The third solution consists of using a DC/AC inverter directly at the PV/FC end to convert the DC power into AC at low voltage level before stepping up at the grid voltage level using a line frequency transformer. This solution uses the simplest technology but a large 50/60Hz transformer size makes it the heaviest/bulkiest. The last solution is to use a single stage DC/AC inverter, which would use either a Voltage Source Inverter (VSI) or a Current Source Inverter (CSI). If the chosen topology is a VSI, a higher voltage level exceeding the peak line-to-line grid voltage level is always needed on the DC side (PV) to provide proper operation. Since at no load, the DC link voltage further increases, this can raise serious insulation and safety issues [3]. In contrast, a CSI has the capability to boost the voltage from the DC side to the AC side which means that a lower DC voltage can be used, compared to a VSI. Moreover, the current drawn from the PV terminals should have a low level of ripple, which would require DC-link current filtering (use of an inductor), a requirement that again points at the CSI as the ideal choice [4].

One drawback of the CSI is that if the input AC voltage level reduces (e.g. during a voltage sag), it makes the CSI unable to operate properly. It may be possible to enable

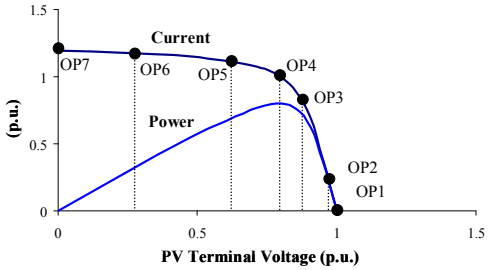


Fig. 1. Typical characteristic curves of a PV

operation of the CSI at reduced voltages from the design stage but this would mean that a rather high DC/AC voltage transfer ratio needs to be used that would increase the cost and degrade the efficiency of the CSI at high power.

Another requirement is regarding the power network stability and protection where distributed generation such as a PV grid interface shall have low voltage ride through (LVFRT) capability, which is the ability to remain transiently stable and connected to the power grid without tripping during the grid fault disturbances in a specified time, support the power grid during the fault with reactive power and be able to supply power to the system immediately after the fault clearance [6]-[9]. Fig. 2 illustrates the typical curves of a required stay connected time according to a particular voltage dip proposed by E.ON [10] (e.g. a 85% voltage dip may last upto 450 ms). It should be noted that the specific requirements of LVFRT vary according to the jurisdiction of each national grid code (i.e. 85% voltage dip may last upto 625 ms in USA [11]).

An evaluation of a current source inverter with series connected AC capacitors (CSI+SC) for PV applications which achieved lower losses and smaller magnetic components in comparison to a standard CSI has been explored in [5]. In this paper, a more detailed analytical model to help the design of the CSI+SC is introduced. Also, in order to accommodate the requirements for grid fault ride through operation, a new control strategy for the CSI+SC will be proposed, and tested via simulations and experiments.

II. Circuit Configurations

A. Circuit Components and Analytical Model

Fig. 3a presents the topology of a CSI+SC using only six reverse blocking IGBTs, similar to [4]. The input LC filter is typically used to reject high order switching harmonics at the AC side whilst the DC-link inductor smoothes the DC-link current at the PV side. The series AC capacitors C_S are the key components to provide the reduction of the AC input voltages at the CSI inputs.

The analytical model is constructed based on the phasor diagram referred to the supply voltage rotating frame as shown in Fig. 3b. The vector V_S and I_S refer to the supply voltage and current with the displacement angle of θ (power factor angle); V_{Cs}, V_{Lf} and V_{Cf} to the voltage drop across the series capacitor C_S, input filter inductor L_f and capacitor C_f; I_{Cf} to the current drawn by C_f; V_{CSI} and I_{CSI} to the input CSI bridge voltage and current a displacement angle of φ; V_{DC} and I_{DC} to the DC side voltage and current. The vector length represents the phase-to-neutral peak value. By applying the vector summation theorem and with the use of an analytical model shown in Fig. 3b, the phase peak values of the relevant

$$\left|\tilde{I}_{CSI}\right| = \sqrt{I_S^2\left(1+\frac{(\omega_c^2-\omega^2)}{\omega_f^2}\right)^2 + (\omega C_f V_S)^2 - 2\omega C_f V_S I_S\left(1+\frac{(\omega_c^2-\omega^2)}{\omega_f^2}\right)\sin\theta} \quad (1)$$

$$\left|\tilde{V}_{CSI}\right| = \sqrt{V_S^2 + \left(\frac{I_S}{\omega C_S}\right)^2\left(1-\frac{\omega^2}{\omega_c^2}\right)^2 - \frac{2I_S V_S}{\omega C_S}\left(1-\frac{\omega^2}{\omega_c^2}\right)\sin\theta} \quad (2)$$

$$P_{CSI} = \frac{3}{2}V_S I_S \cos\theta \quad (3)$$

$$Q_{CSI} = \frac{3}{2}\cdot\left(\omega C_f V_S^2 - V_S I_S \sin\theta\cdot\left(1+\frac{2(\omega_c^2-\omega^2)}{\omega_f^2}\right) + \frac{I_S^2}{\omega C_f}\cdot\left(1+\frac{(\omega_c^2-\omega^2)}{\omega_f^2}\right)\cdot\left(\frac{(\omega_c^2-\omega^2)}{\omega_f^2}\right)\right) \quad (4)$$

$$\varphi = \tan^{-1}\left(\frac{Q_{CSI}}{P_{CSI}}\right) \quad (5)$$

where $\omega_c = 1/\sqrt{L_f C_s}$; $\omega_f = 1/\sqrt{L_f C_f}$; P_{CSI} and Q_{CSI} refer to the active and reactive power seen at the input CSI bridge. parameters can be formulated:

It can be seen in Fig. 3b that the amplitude of V_{CSI} (line OQ), which relates to the PV terminal voltage via the CSI voltage transfer, can vary depending on the position of Q on the line PR (leading by 90 degrees the supply current). In the situation when Q moves close to R, V_{CSI} is the largest and the series capacitor voltage will reduce which means that the CSI+SC will see an input voltage level as high as the standard CSI. In contrast, if Q moves close to P, the series capacitor voltage will be larger and V_{CSI} begins to reduce and reaches the smallest value when Q=P which is where V_{CSI} is equal to $V_S\cos\theta$. This means that the reduction factor of V_{CSI} can be directly represented by the power factor ($\cos\theta$).

To facilitate the analysis and the circuit component design, the parameters m and a are defined as the CSI modulation index (6) and the input CSI voltage reduction factor (7).

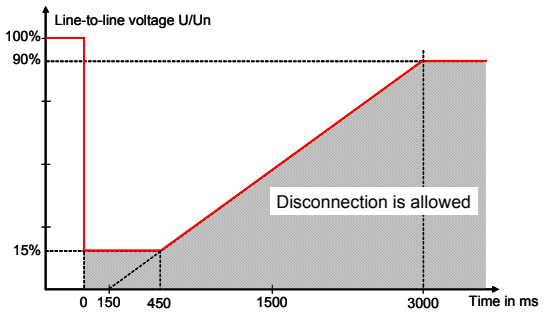


Fig. 2. Typical requirement for Low Voltage Ride-through for high and extra high voltage (Credit: E.ON Netz, Aug 2003 [10])

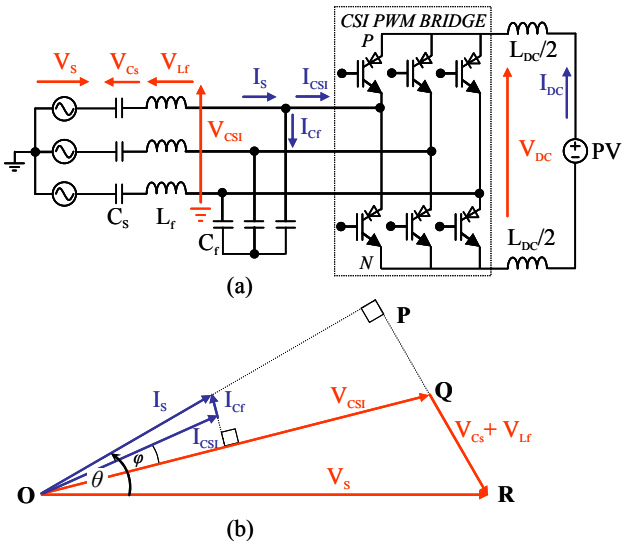


Fig. 3 a topology of a CSI with series connected AC capacitors (a) and its corresponding pharsor diagram (b) when it operates in rectification mode.

$$\left|\vec{I}_{CSI}\right| = mI_{DC} \qquad ; 0 < m \le 1 \tag{6}$$

$$\left|\vec{V}_{CSI}\right| = aV_S \qquad ; 0 < a \le 1 \tag{7}$$

B. *Design of Series Connected AC Capacitors*

As the size of a series connected AC capacitor is inversely proportional to the voltage drop across it, its required size desired to be the smallest, should be therefore determined at full load power where the series capacitor voltage is the largest, which is the case when a =cosθ. Using (1)-(4), (6) and (7), the required series capacitor can be formulated:

$$C_S = \frac{1}{\omega^2 L_f + \left(\frac{3\omega V_S^2 \cdot (a\sqrt{1-a^2})}{2P_{\max}}\right)} \qquad ; a = \cos\theta \tag{8}$$

Fig. 4 shows the required value of a series capacitor as a function of the input CSI voltage at different power levels. It can be noticed that a smaller series capacitor is required for a low input CSI voltage in the range of 0.6-0.8, which matches the typical no-load vs. full load PV voltage.

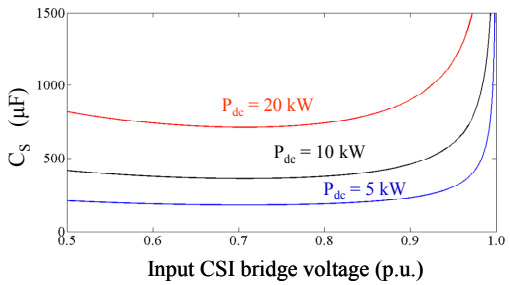


Fig. 4. The required series AC capacitors vs. the input CSI bridge voltage in different DC power levels: 5kW, 10kW and 20kW (line voltage 415 V; L_f= 0.5mH).

III. Modulation and Control Strategy

A. *Modulation Strategy*

The PWM switching signals for a CSI must satisfy the constraints of always providing a current path for the DC current source whilst not short circuiting the input supply lines [12]. As a result only two switches are needed to conduct at any instant time that reflects in only six legal active switching states and three zero current switching states that the shortcircuit DC-link. The technique used to generate the switching signals in this paper is the Space Vector Modulation (SVM), which is used often in modern PWM converters [13]. It uses the input current as the reference vector to select the appropriate switching state. The description of the implementation is detailed in [5].

B. *Control Strategy for Low AC Input CSI Bridge Voltage*

The control of the CSI +SC in order to achieve low voltage ratings of the switches is done in similar way to [14]. Fig. 5a-d illustrate the phasor diagrams when the CSI+SC operates at no load (OP1), light load (OP2), high load (OP3) and full load (OP4) as shown in Fig.1, respectively. It is clear that at no load (Fig. 5a), no current flows in the DC circuit which means that no power generated from PV; the series capacitor voltage V_C and the voltage across filter inductors are very small in which means the CSI voltage will be as high as the supply voltage. At light load (Fig.5b), a small DC-link current that causes a small AC current, begins to flow, which causes only a small voltage drop across the series capacitor and therefore only a small drop in the input CSI voltage amplitude V_{CSI}, reflected by a similar amplitude to the supply voltage V_S and a small displacement angle of the supply current angle. At higher generated power (Fig. 5c) and maximum power (Fig. 5d), larger DC-link currents are applied that induce larger capacitor voltage drops. This causes a significant reduction of the input CSI voltage, which could eventually match the reduction in PV voltage on the DC side, but also a larger phase shift of the supply current displacement angle. By controlling the CSI+SC in this way, the CSI+SC will allow a close matching of the voltage synthesized on the DC side by the CSI to the external characteristics of the PV, whilst maintaining the CSI modulation index (and therefore the utilization of the semiconductors) at higher levels than for a standard CSI. Moreover, as the reduced input CSI voltage provided by the CSI+SC is switched during each commutation at higher DC-link current (power), lower switching voltage stress and lower DC-link voltage ripple will be produced. As the result, a smaller DC-link inductance and lower switching losses compared to a standard CSI can be achieved [5].

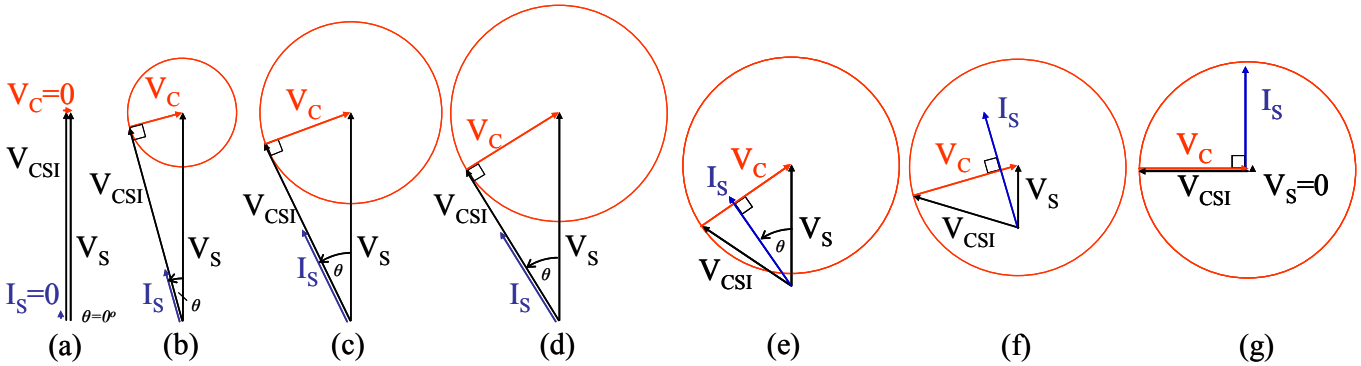


Fig. 5 The phasor diagram of a CSI+SC when it operates at: (a) no load (OP1 in Fig. 1); (b) light load (OP2); (c) high load (OP3) and (d) full load (OP4) and also when the voltage at the power grid side drops by: (e) 40% (OP5); (f) 70% (OP6) or(g) 100% (OP7).

C. *Control Strategy for Grid Fault Ride-Through*

As the further reduction in PV terminal voltage results in a larger supply current, (OP5, OP6 and OP7 as shown in Fig.1), this allows the supply voltage to be further reduced at a particular delivered power. However, a large dip in the supply voltage demands a larger reactive current (power).

Fig. 6 shows the reactive current injection as required by the LVFRT grid codes in comparison to the capability of the CSI+SC topology to inject reactive current, depending on the magnitude of the voltage sag. Due to the presence of series capacitors, the CSI+SC is normally injecting reactive current when grid voltage is at the rated value and the rise in capacitive current injection as a dependence on the fall in supply voltage does not accurately follow the requirement, but is obviously better than for standard CSI. However, this also means that the CSI + SC can allow feeding active current into the power grid during very large voltage dips, if needed.

Fig. 5e-g presents the progression of the phasor diagram of a CSI+SC with respect to a dip in the supply voltage at the operating point OP5, OP6 and OP7 as shown in Fig. 1 respectively. The control runs based on a simple process by equalizing the amplitude of V_{CSI} and a series capacitor voltage V_C and then the injection of a reactive current can be controlled by adjusting the appropriate power factor angle (θ), which is defined by:

$$\theta = \sin^{-1}\left(\frac{1-b}{2}\right) \qquad ; 0 \le b \le 1 \qquad (11)$$

where b is the supply voltage reduction factor. After that the angle (θ) will be put in equation (3), (4), (5) to calculate the displacement angle between input CSI voltage and current (φ), which then controls the injection of reactive current, by means of reactive power control, eventually.

Fig. 7 illustrates the control diagram which is used to achieve both low input CSI voltage during normal grid conditions and also LVFRT operation. It can be noticed that the supply current is not necessary to calculate (φ); that is

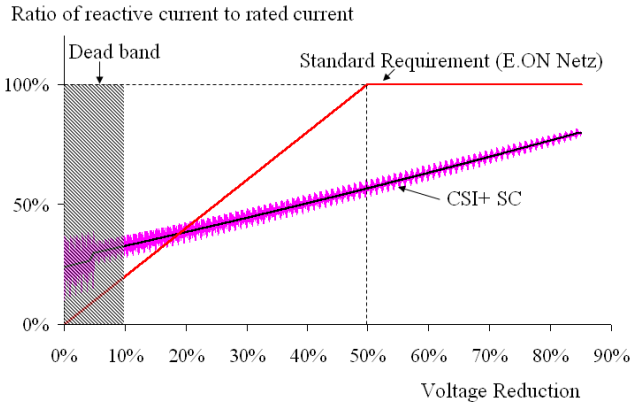


Fig. 6 a typical permissible reactive current according to the percentage of voltage reduction for standard requirement (E.ON Netz, Aug 2003 [10]) and for the proposed CSI+SC topology

$$I_S = \frac{\omega C_f V_S \sin\theta + \sqrt{(mI_{DC})^2 - (\omega C_f V_S \sin\theta)^2}}{\left(1 + \frac{\omega_c^2 - \omega^2}{\omega_f^2}\right)} \qquad ; 0 \le \theta \le \pi/2 \qquad (12)$$

because it can be derived from (1) and (6) as (12). It can also be noted that the control for LVFRT will begin working only when the supply voltage drops by more than 10 %, which is suggested by a standard curve shown in Fig. 2. In addition, in the worst case of a shortcircuit at the supply terminals (100% dip), the CSI+SC still allows operation as shown in Fig. 5g, However, there may be no active power delivering the power grid because the angle φ will become $\pi/2$.

IV. Simulation and Experimental Results

A. *Simulation Results*

The simulation models of the CSI+SC was implanted in Saber in order to verify its performance. The value of the series capacitor was calculated using (8). All simulation parameters are listed in Appendix A. Fig. 8a-h shows the simulation results of the CSI+SC riding though a low voltage grid fault as defined in Fig. 2. It can be seen that throughout the fault, the amplitude of the supply current does not change

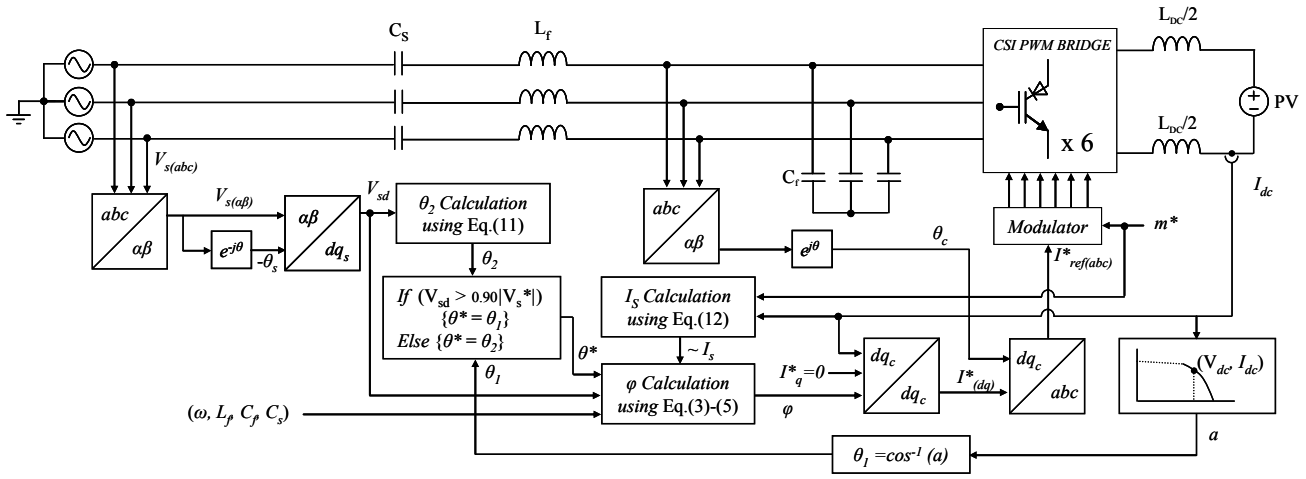


Fig. 7 The control schematic of a CSI+SC topology to control low AC input voltage reduction matching to PV external characteristic curves and provide the grid fault ride through capability.

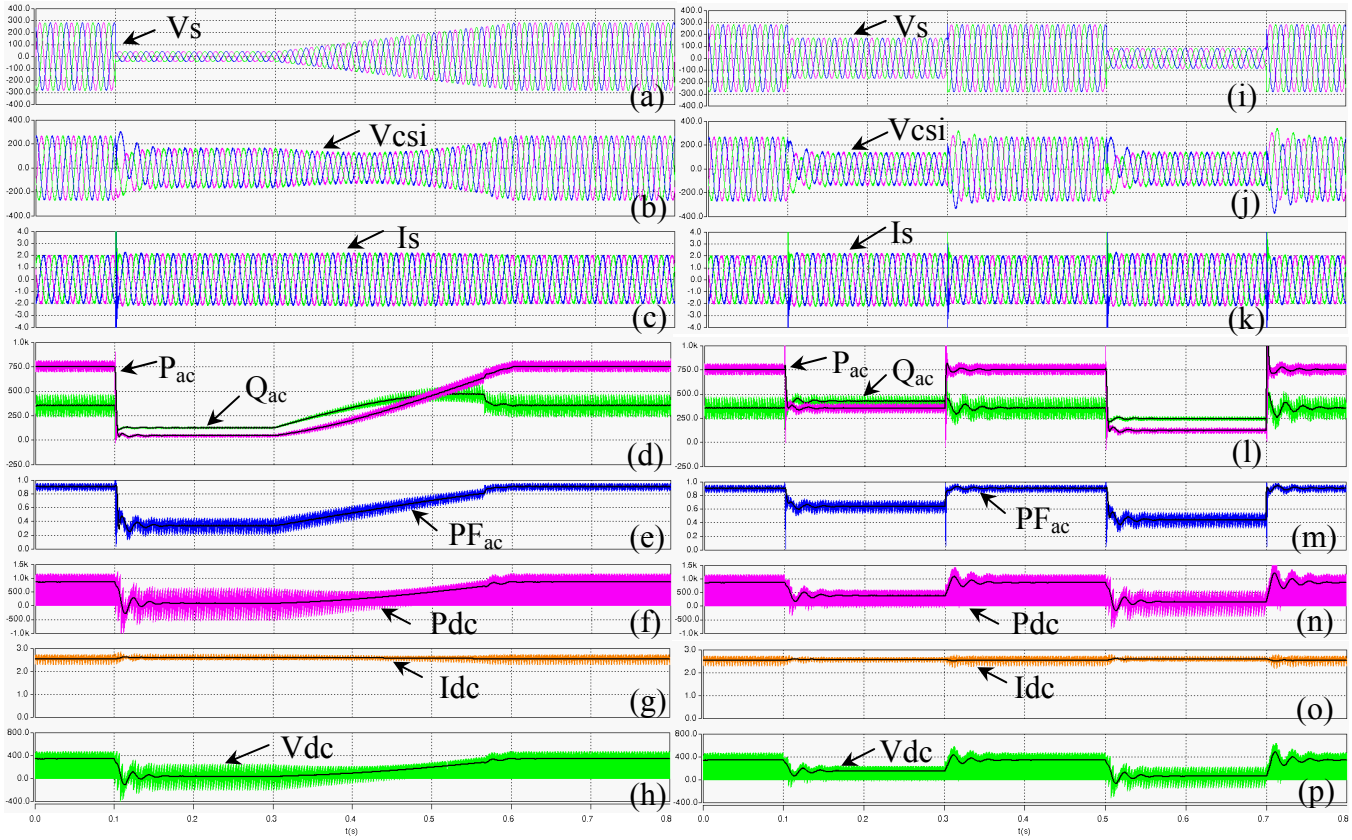
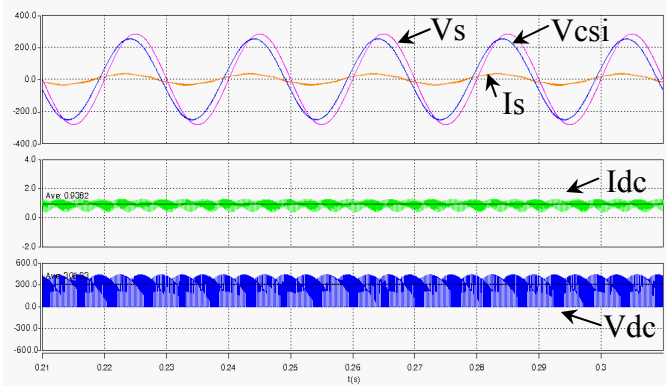


Fig. 8. Simulation results of a CSI+SC riding though a low voltage grid fault (15% of rated supply voltage) starts at t=0.1s (left side) and during grid voltage steps by 60% and 30% of rated supply voltage at t=0.1s and t=0.5s then return to rated voltage at t=0.3s and t=0.7s respectively (right side). The waveforms: a), i) supply voltage Vs; b), j) supply current Is; c), k) phase voltage on the CSI AC side Vcsi; d), l) active (Pac) and reactive power (Qac) seen from the AC power grid; e), m) the ac power factor (PFac); f), n) the actual and filtered waveforms of the DC power (Pdc); g), o) the DC-link current Idc; h), p) the actual and the filtered DC-link voltage on the DC CSI terminals.

but only its displacement angle, even though the supply voltage drops to a level as small as 15% of the rated value, the CSI input voltage remains to a higher value, facilitated by the existence of the series capacitor. The active power drops almost to zero; there is also a drop in the level of reactive power, but that is mostly due to the collapse in the supply voltage. The power factor change from near one to near zero illustrates that almost all the supply current is capacitive, supporting therefore restoring the grid voltage towards rated conditions.

The transient response to step changes in the supply voltage from rated level to 60 % (t=0.1 s) then back to the rated level (t=0.3s) and again from rated level to 30 % (t=0.5s) is shown in Fig. 8i-p. In all cases, the DC-link current varies very little, because the operating point of the PV moves from OP4 to OP5 and OP6 (see Fig. 1), in the area of constant current of the PV, which also causes the collapse of the PV voltage in order to match with the required fall in the CSI input voltage as dictated by the phasor diagram (Fig. 5f) to maintain the capability of the CSI+SC to export reactive power. This is revealed by the active and reactive power graphs (Fig. 8l) where the variation of the active power follows accurately the variation of the supply voltage, whilst the reactive power remains more or less constant.

To confirm the viability of the control, the operation of the CSI+SC is tested also for operation in rectifier mode and the results are presented in Fig 9. The case of light load which is equivalent to OP2 in Fig. 1 and high load (OP3) are shown in Fig. 9a-b. At light load (Fig. 9a) with a low DC-link current (I_{DC}=0.95A), causes the supply current to be low therefore only a small voltage drop across series capacitors is induced. The DC-link current ripple is approx. 0.8Apk-pk. At high load in Fig.9b, a larger DC-link current (2.35A) causes with a drop of 30% in the input CSI voltage ($225V_{pk}/285V_{DC}$) compared to light load ($283V_{pk}/306V_{DC}$). Because a larger DC current induces a larger series capacitor voltage drop, which also causes a larger phase shift of the supply current angle but reduces the input CSI voltage. This has a consequence in lowering the voltage stresses across the switching devices and therefore lower switching losses. Fig. 9c,d demonstrate the operation with low grid voltage of 40% and 70% V_S dips, that are equivalent to OP5 and OP6 in Fig.1, which are relevant for the fault ride through capability. Slightly larger DC-link currents (approx. 2.7A) cause larger supply currents and also the high series capacitor voltage drops and lower input CSI voltages (180V/60V for 40% and 70% Vs dip respectively). This reflects on the increase of the displacement angle φ (48 degrees for the 40% voltage dip



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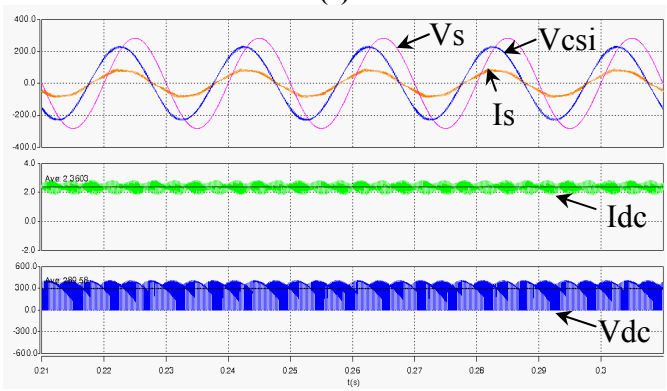

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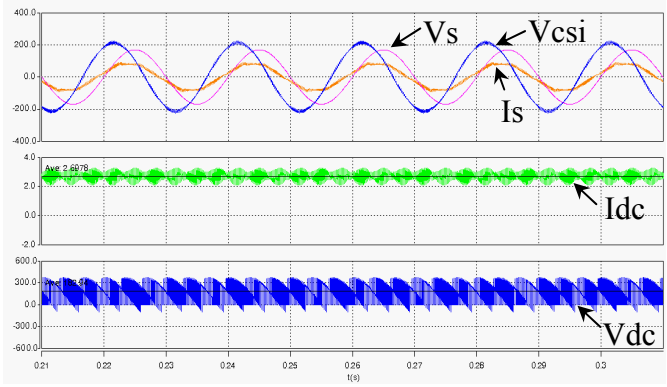

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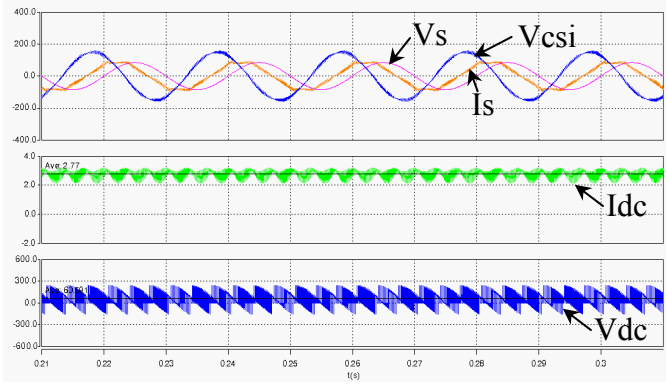


(d)

Fig. 9. Simulation results of CSI+SC operates at: a) light load (R_L=326Ω); b) high load (R_L=123Ω); c) 40% supply voltage dip (R_L=65Ω) and d) 70% supply voltage dip (R_L=21Ω); Waveforms: Is: supply current(x100); Vs: phase-to-neutral voltage; Vcsi: input CSI phase voltage on the AC side terminals; Idc: DC-link current; Vdc: DC-link voltage on the DC CSI

and 70 degrees for the 70% dip).

B. Experimental Results

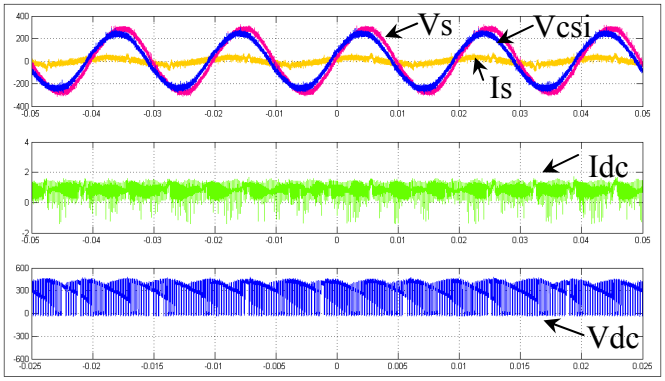
A laboratory prototype of a CSI using six reverse blocking IGBTs reported in [4] is used to validate the operation of a CSI+SC in the two situations: with low input AC voltage reduction whilst operating in LVFRT mode and in normal grid conditions whilst the DC-load changes. Due to the potential problems of connecting a DC-source in the CSI DC-link, it was chosen to test the operation of the CSI+SC in rectifier mode (the power flows from the AC side / power grid to the DC side); however, the operating points were chosen to match OP1-3 in Fig. 1. The circuit parameters and load conditions are the same as in the simulation and presented in the Appendix. Fig. 10a-d shows the experimental results of a CSI+SC operating in rectification mode, similar results to of the simulation. A large voltage across the DC terminals (235 V) and a low DC-link current (approx 0.7A) were chosen to emulate the light load condition (OP1). The result is shown in Fig. 10a consequently, producing insignificant series capacitor voltage drop. Fig. 10b shows an equivalent high load test result with a DC-link current level of 1.7-1.9A whilst the input CSI voltage reduces to $230V_{peak}$ compared to $247V_{peak}$ at light load, by a slightly higher series capacitor voltage drop. Fig. 10c-d show the operation with a 40% and 70% supply voltage dip respectively. Similar results to the simulation in Fig. 9 are obtained. The input CSI voltage is approx 210 Vpk (40% dip) and 160Vpk (60% dip) is leveled down according to the equivalent decrease of PV voltage in Fig. 1 (140V/44V). This change in CSI input voltage causes a slightly smaller DC-link current ripple (approx $1.0A_{pk\text{-}pk}$) compared to approx $1.3A_{pk\text{-}pk}$ at full load.

CONCLUSIONS

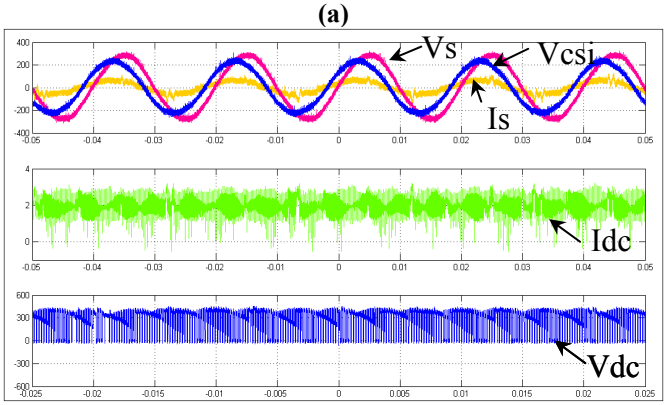
In this paper, the analytical model and control method used for a Current Source Inverter with series connected AC capacitors in order to achieve operation with reduced AC input voltage to accommodate smaller voltage stress at high power, which is characteristic for PVs and low voltage ride though fault capability which is a requirement for distributed generation, have been proposed. This is performed by controlling the voltage drop across the series connected capacitors through the control of the input CSI current/displacement angle to match to the external characteristics of a PV/the drop in the power grid voltage level. Simulation and experimental results are used to confirm the viability of the proposal.

APPENDIX A

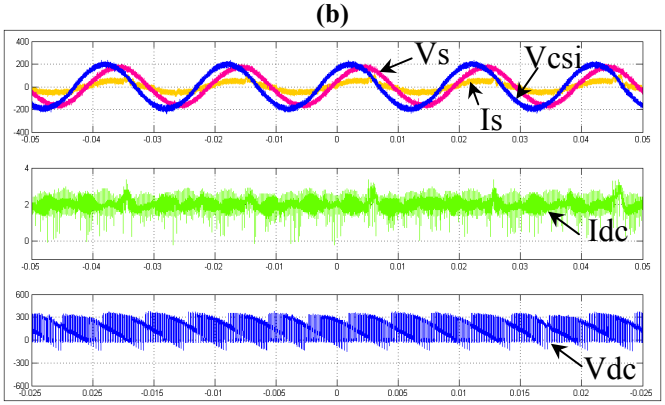
Parameters both for simulations and experiments: $V_{S\text{-}line}$= 346Vrms; fin= 50Hz; L_f= 1.4mH/ph; C_f= 6.9μF/ph; $2xL_{DC}$= 13mH; C_S= 33μF, fsw= 5 kHz, m= 0.95 (fixed); PV rating of a=0.7, I_{DC} =2.65A, P=0.62kW (88.3Ω); R_L= 326/123/65/21Ω (light load, high load, 40% Vs dip and 70% Vs dip).



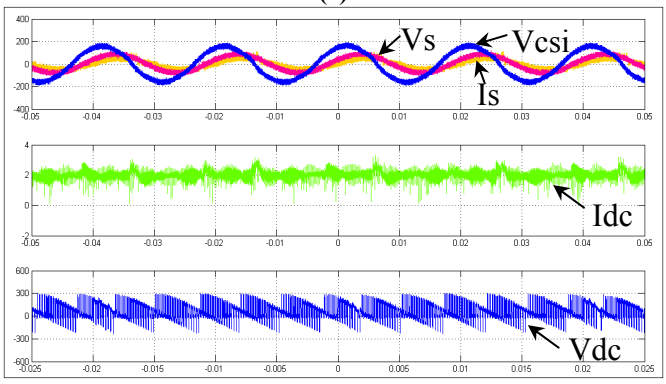
(a)



(b)



(c)



(d)

Fig.10. Experimental results of CSI+SC operates at: a) light load (R_L=326Ω); b) high load (R_L=123Ω); c) 40% supply voltage dip (R_L=65Ω) and d) 70% supply voltage dip (R_L=21Ω); Waveforms: Is: supply current(x100); Vs: phase-to-neutral voltage; Vcsi: input CSI phase voltage on the AC side terminals; Idc: DC-link current; Vdc: DC-link voltage on the DC CSI terminals.

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