A Hybrid Chain-Link Push-Pull Series Connected (H-CL-P2SC) M2C with DC Fault Blocking Capability

Mustafa Kaya*, Alessandro Costabeber, Alan J. Watson, Francesco Tardelli and Jon C. Clare
Power Electronics, Machines and Control Group, University of Nottingham
Email: *mustafa.kaya@nottingham.ac.uk

Abstract—This paper introduces a hybrid chain-link push-pull series connected (H-CL-P2SC) modular multilevel converter for HVDC applications, especially for those considering a connection of off-shore wind farms to the grid. On the ac side, each converter phase is connected to the corresponding grid phase via a single-phase center-tapped transformer whereas on the dc side, the converter phases are connected in series. The required functionality of the chain-link (CL) inductors in other modular multilevel topologies is achieved by using the leakage inductance of each transformer. As a result, the converter does not require separate CL inductors. Since the phases are series connected on the dc side, the H-CL-P2SC requires 33.3% less cells (NCs) to withstand the same dc voltage when compared to the standard modular multilevel converter (M2C). A control strategy for the H-CL-P2SC is discussed in detail. The global and internal power balance controllers are illustrated with block diagrams. A numerical comparison between the H-CL-P2SC and other typologies is also presented. Finally, the response of the H-CL-P2SC to a dc pole-to-pole (P2P) fault is shown using PLECS simulations for a 20 MW-20 kV demonstrator.

Index Terms—M2C, HVDC, dc fault ride through, push-pull inverter

I. INTRODUCTION

The modular multilevel converter (M2C), constructed using half-bridge cells (HB-Cs), is a well-known and commercially used voltage source converter (VSC) in high voltage direct current (HVDC) applications [1]. The M2C is the most attractive VSC used in high voltage transmission applications compared to the other multilevel ac-dc converters as a result of its modularity, scalability, and efficiency [2].

In the M2C, each chainlink (CL) is connected in series with an inductor to limit fault and circulating currents [3]. Although the M2C does not require transformers for its operation, three-phase star-delta connected transformers are generally used in practical applications to provide isolation between the converter and the grid, and to adjust the ac voltage level [4]. The air-cored CL inductors and grid interface transformers require significant space which is undesirable in off-shore applications [5].

By increasing the number of the series connected HB-Cs in CLs, the output waveform quality can be improved whilst reducing the voltage stress on the cells semiconductor devices and potentially reducing the device switching frequency. However, increasing the number of cells (NCs) increases the cost and complexity of the converter.

A major drawback of the M2C utilizing HB-Cs is the inability to block dc fault current resulting from a short circuit on the dc bus [6]. An opposing voltage can be generated by using full-bridge cells (FB-Cs) instead of HB-Cs in the CLs of the M2C, to prevent the fault current flowing through the converter and damaging the cells. However, the number of semiconductor devices are doubled in the case of CLs with FB-Cs under these circumstance. There has been significant research on different cell and CL arrangements of the M2C to provide fault blocking capability whilst minimising the increase in device count, construction cost and the losses [7], [8]. Some of these topologies are only capable of fault blocking whilst others can achieve this whilst providing static synchronous compensator (STATCOM) operation [8].

The alternate arm converter (A2C) is a hybrid topology combining some of the features of both the M2C and the two-level VSCs to provide dc fault ride through capability (FRT-C) [9]. The A2C improves some of the aspects of the M2C, such as lowering the capacitor and energy storage requirements whilst adding dc fault ride through capability [10], [11]. However, these come with some drawbacks such as requiring bulky passive filters on the dc side, the use of series connected switches, and some difficulty in capacitor voltage balancing due to the alternating CL currents [12], [13].

This paper proposes a hybrid chain-link push-pull series connected (H-CL-P2SC) modular multilevel converter intended to overcome some of the practical issues related to the M2C as addressed above. In this paper, hybrid chain-links (H-CLs) consisting of both the HB-Cs and FB-Cs as described in [14], are used to achieve FRT-C in the H-CL-P2SC. The operating, modelling and control of the converter is shown in detail and the STATCOM operation of the converter under dc pole-to-pole (P2P) faults is validated via PLECS simulations.

II. OPERATION OF THE P2SC

The three-phase circuit diagram of the H-CL-P2SC is illustrated in Fig. 1. As in the M2C, having HB-Cs or FB-Cs in the CLs does not affect the operation or modularity of the converter. The number of HB-Cs and FB-Cs that are used in each CL are N_{HB} and N_{FB} , respectively. The total number of cells in each CL is $N_C = N_{HB} + N_{FB}$. u_c^{cap} is the capacitor voltage of the cell capacitors C_c . The sum of the cell output

Fig. 1. Grid connected three-phase circuit configuration of the H-CL-P2SC.

voltages u_c^{out} in each CL corresponds to the CL voltages (as in the M2C).

The left and the right CLs (L-CH and R-CH) construct one phase of the converter that is connected to the corresponding ac phase e_g^k via a centre-tapped transformer. Here $k = a, b, c$ corresponds to the phases a, b, and c, respectively. The inductances L_{lk} in Fig. 1 illustrate the equivalent leakage inductances of the transformers referred from each secondary to primary side. The number of turns on the secondary sides are equal and denoted as $M_S/2$ while the number of turns on the primary side of the transformers is M_P . The purpose of having L-CHs and R-CHs is to cancel out the ac components of the CL voltages u_{CL}^{left-k} and $u_{CL}^{right-k}$ on the dc side i.e. the potential difference between the points A and B (u_{AB}^k) in Fig. 1.

The same dc current i_{dc}^{con} flows through the converter phases since the phases are connected in series on the dc side. The full ac grid current i_g^k circulates within each corresponding converter phase. The left and right CL currents are i_{CL}^{left-k} and $i_{CL}^{right-k}$ respectively. The ac components of the CL currents cancel out on the dc side leaving the dc current ripple free. The dc components of the CL currents do not cause saturation of the transformer since the dc flux generated by these current components oppose and hence cancel.

The dc grid is modelled as a constant dc voltage source E_{dc} connected to the converter via a lumped dc cable model. Here L_{dc} , R_{dc} , and C_{dc} are the equivalent inductance, resistance, and capacitance of the cable model, respectively. The current flowing through the dc cable is denoted as i_{dc}^{cab} .

A. Mathematical Expressions

In order to simplify the mathematical analysis of the converter model, it is assumed that each cell in the CLs are identical and their capacitor voltages are well balanced

and ripple free. Under these assumptions, the CLs can be approximated as controllable voltage sources.

The balanced ac grid voltages and currents can be expressed as

$$e_g^k = E_g^k \sin(\omega t - k \frac{2\pi}{3}) \quad (1)$$

$$i_g^k = I_g^k \sin(\omega t - k \frac{2\pi}{3} - \varphi) \quad (2)$$

where E_g^k and I_g^k are the magnitudes of the phase grid voltage and current respectively, ω is the fundamental angular frequency and φ is the phase shift between the grid voltage and current.

Each CL must be capable of generating one third of the dc voltage and half of the ac grid voltage to balance the power between ac and dc sides. Assuming zero voltage drop across the transformer leakage inductances, the CL voltages can be expressed as:

$$u_{CL}^{left-k} = \frac{E_{dc}}{3} - \frac{M_S}{2M_P} e_g^k \quad (3)$$

$$u_{CL}^{right-k} = \frac{E_{dc}}{3} + \frac{M_S}{2M_P} e_g^k. \quad (4)$$

As is clear from (3) and (4), the ac components of the CL voltages cancel on the dc side leaving $u_{AB}^k = E_{dc}/3$ free from ac ripple in the ideal, balanced case. Therefore, high-voltage capacitor filters are not required on the dc side. Note that the overall dc voltage is the sum of the voltages between points A and B of each phase

$$E_{dc} = u_{AB}^a + u_{AB}^b + u_{AB}^c. \quad (5)$$

The ac modulation index m_{ac} relates the ac voltage magnitude to the dc voltage in each CL and is described as:

$$m_{ac} = \frac{3}{2} \frac{M_S}{M_P} \frac{E_g}{E_{dc}}. \quad (6)$$

Fig. 2. Equivalent Circuit of the H-CL-P2SC during P2P dc short-circuit.

Assuming identical CLs and transformers, half of the dc current flows through each CL. With the transformer arrangement in Fig. 1, the full ac current circulates in each phase. Therefore, the semiconductor devices in the CLs must be rated for the half of the dc current plus the full ac current. The CL currents are expressed as:

$$i_{CL}^{left_k} = \frac{i_{dc}^{con}}{2} - \frac{M_P}{M_S} i_g^k \quad (7)$$

$$i_{CL}^{right_k} = \frac{i_{dc}^{con}}{2} + \frac{M_P}{M_S} i_g^k. \quad (8)$$

As seen from Fig. 1, the CL currents enter the transformer secondary windings with opposing signs. Therefore, the dc flux generated by the left and the right CL currents cancel. Applying Kirchhoff's current law to the transformer arrangement in Fig.1, the ac grid current can be calculated from the CL currents as:

$$i_g^k = \frac{M_S}{2M_P} (i_{CL}^{right_k} - i_{CL}^{left_k}). \quad (9)$$

One of the requirements of the VSCs is that the average mean power in each CL must be equal to zero. Neglecting the losses, the instantaneous power of each CL in a phase is obtained by multiplying the voltage generated by that CL and the current through that CL

$$p_{CL}^{left_k} = u_{CL}^{left_k} i_{CL}^{left_k} \quad (10)$$

$$p_{CL}^{right_k} = u_{CL}^{right_k} i_{CL}^{right_k}. \quad (11)$$

Substituting the CL voltage and current equations ((3),(4) and (7),(8)) into (10) and (11) and averaging the instantaneous powers over a line period, the average mean power in each CL is found as:

$$P_{CL}^{avg} = \frac{E_{dc} I_{dc}^{con}}{6} - \frac{E_g I_g \cos(\varphi)}{4}. \quad (12)$$

If the ac and dc powers in each CL are balanced, the average mean power in each CL is inherently zero as seen in (12).

Assuming a unity ac modulation index $m_{ac} = 1$, each CL must be capable of generating $2E_{dc}/3$, as seen from (3) and (4). Hence the total number of cells in each CL is described as:

$$N_C = \frac{2E_{dc}}{3U_c^{cap}}. \quad (13)$$

For the same power, dc and ac voltage levels, each CL in the M2C must be rated for the full dc voltage E_{dc} . Considering the same nominal capacitor voltage value U_c^{cap} for both converters, the H-CL-P2SC requires a 33.3% lower quantity of cells when compared to the M2C.

B. DC Fault Considerations

A P2P short circuit fault is the most severe dc fault condition in HVDC applications [15], [16]. The equivalent circuit of the H-CL-P2SC under a P2P short circuit fault is illustrated in Fig. 2. The dc voltage drops to approximately zero. Hence, the voltage between the points A and B is also approximately zero ($u_{AB}^k \approx 0$). If the total capacitor voltage of the cascaded FB-Cs in each phase is higher than the corresponding phase ac voltage magnitude, dc fault current blocking can be achieved by switching off all the IGBTs in the converter. Since the FB-Cs can generate reverse-biased voltages, reactive power can be exchanged with the grid even during the dc fault by generating the appropriate ac voltages at the output of the converter phases. The minimum number of FB-Cs for the STATCOM operation during dc faults can be calculated by:

$$2U_c^{cap} N_{FB} \geq E_g. \quad (14)$$

Substituting (6) and (13) into (14), the ratio between the N_{FB} and N_C can be found as:

$$N_{FB} \geq m_{ac} \frac{M_P}{M_S} \frac{N_C}{2}. \quad (15)$$

C. Numerical Expressions

A numerical comparison between the H-CL-M2C, A2C, and H-CL-P2SC with dc FRT-C is illustrated in Table I. The values for the two H-CL converter topologies, H-CL-M2C and H-CL-P2SC are calculated by using the same techniques for both converters whereas the values for the A2C have been collected from [9]–[11] for comparison. The power ratings, the dc voltage and the nominal cell capacitor voltages of the converters are the same.

The converter side ac voltages of the H-CL-M2C and H-CL-P2SC are adjusted for a unity ac modulation index. The ac voltage of the A2C is adjusted for the “sweet-spot” operating point of the converter. The number of cells per CL for all the converters includes a 10% redundancy. The NCs per CL in the H-CL-M2C is the highest with 16 cells. Although the A2C and H-CL-P2SC require the same NCs in each CL (10 cells), the total number of IGBTs in the A2C (288) is higher than the H-CL-P2SC (180). This is due to the director switches used in the A2C CLs. Moreover, all the cells used in the A2C are FB-Cs whereas the CLs in the H-CL-P2SC consist of both HB-Cs and FB-Cs. The H-CL-P2SC requires a significantly lower number of semiconductor devices, compared to other topologies, to withstand the same dc voltage under normal conditions and STATCOM operation during dc faults.

The cell capacitor value and the energy requirement are significantly reduced in the A2C. Here, 16 kJ/MVA represents the total energy per power requirement of the cell and the dc filter capacitors. The cell capacitor value in H-CL-P2SC is 1.5

TABLE I
NUMERICAL COMPARISON

	H-CL-M2C	A2C	H-CL-P2SC
Power rating	20 MW		
DC voltage	20 kV		
Converter side RMS L-L ac voltage	11 kV	15.6 kV	14.6 kV
Nominal cell voltage	1.5 kV		
No of cells per CL	16	10	10
No of IGBTs per CL	48	40	30
No of director switches per CL	-	8	-
Total no of IGBTs	288	288	180
Cell Capacitance	8 mF	4 mF	12 mF
Energy per power	32 kJ/MVA	16 kJ/MVA	32 kJ/MVA
No of CL inductors	6	6	-
CL inductance	0.25 mH	0.5 mH	-
DC Filter Capacitance	-	3.36 mF	-
DC Filter Inductance	-	12 mH	-
Conduction Losses	155 kW	139 kW	155 kW
Switching Losses	76.5 kW	36 kW	76.5 kW
Filter Losses	-	56 kW	-
Total Losses	231.5 kW	231 kW	231.5 kW

times the cell capacitor value of the H-CL-M2C. However, the total energy requirement is the same for both converters as the NCs in the H-CL-M2C is 1.5 times the H-CL-P2SC. As shown in Table I, the A2C requires passive components for filtering purposes, whereas the H-CL-M2C and the H-CL-P2SC do not require these. The H-CL-P2SC further decreases the number of passive components by eliminating the arm inductors as the functionality of these is provided by the leakage inductance of the transformers.

The loss breakdown of the H-CL-M2C and the H-CL-P2SC are the same. The conduction and the switching losses in the A2C are lower compared to other arrangements in Table I, as a result of the director switches. The FB-Cs are rated for a voltage level less than the full dc voltage since the director switches share the dc voltage blocking. Due to the soft switching capability of the director switches, the overall switching losses in the A2C is low. However, the resistive losses associated with the dc filters increase the overall converter losses in the A2C.

III. CONTROL OF THE P2SC

For modelling purposes, it is assumed that the dc voltage is fixed at the receiving end of a back-to-back HVDC system by representing it with a dc voltage source. The dc current reference is imposed for the dc current controller as shown in Fig. 3(a), which generates the overall dc voltage desired u_{mod}^{dc} to drive the required dc current. The reference dc current is

Fig. 3. Block diagrams of the controllers. (a) dc current controller. (b) Total energy and ac current controllers. (c) Inter-phase balancing controller. (d) Intra-phase balancing controller.

calculated from the required power reference which is zero when there is a P2P short circuit on the dc side.

Since the dc power is fixed by the dc current controller and the dc voltage source, a global energy controller ensures that converter power on both the ac and the dc sides are balanced by generating the magnitude of the active power part of the ac current (Fig. 3(b)). The total capacitor voltage in the converter is compared with the reference $\sum_{con} u_c^{cap*} = 6N_C U_c^{cap}$ and the error is compensated by acting on the ac current reference. A standard three-phase PLL is used to generate the angle function for each phase. The reactive power component of the ac current is imposed. The final ac current reference is calculated by:

$$i_g^{k*} = i_g^{act*} \sin(\theta_g^k) + i_g^{react*} \cos(\theta_g^k) \quad (16)$$

where θ_g^k is the phase angle generated by the PLL. Three single phase PR controllers are used to ensure that the sinusoidal current references are tracked accurately. The ac

current controllers generate the ac output voltage references $u_{mod_ac}^k$ for each converter phase to ensure the correct power is delivered.

In order to achieve internal energy balance within the converter, two more controllers are introduced: (1) inter-phase balancing and (2) intra-phase balancing controllers. The block diagram of the inter-phase and intra-phase balancing controllers are given in Fig. 3(c) and Fig. 3(d) respectively. The purpose of the inter-phase balancing is to ensure that the power balance between three phases is achieved. A method to balance power between the three series connected phases in [17] is used in this paper. When the power between two phases is balanced, the third phase is automatically balanced as the dc voltage correction terms generated by these controllers $u_{dc_corr}^k$ sum up to zero as shown in Fig. 3(c).

The intra-phase balancing controller ensures the power balance between the left and the right CLs in each phase by generating a common ac voltage correction term $u_{ac_corr}^k$ in phase with the ac current of the corresponding phase. The difference between the total capacitor voltages of the left and the right CLs is forced to zero by adding an ac voltage correction term to the CL voltage references. As seen in (3) and (4), the ac components of the CL voltages are the same but with opposite signs. The common voltage term moves power from one CL to another to balance their powers without changing the operating point of the converter as these voltage terms are in phase with the corresponding ac current. Finally, the voltage reference for the PWM and the capacitor balancing is generated as:

$$u_{CL}^{left_k*} = \frac{u_{mod}^{dc*}}{3} - \frac{u_{mod_ac}^k}{2} + u_{dc_corr}^k + u_{ac_corr}^k \quad (17)$$

$$u_{CL}^{right_k*} = \frac{u_{mod}^{dc*}}{3} + \frac{u_{mod_ac}^k}{2} + u_{dc_corr}^k + u_{ac_corr}^k \quad (18)$$

The modulation and capacitor balancing strategy that is described for hybrid CLs in [14] is used in this paper to generate the desired voltages and achieve capacitor balancing in the CLs.

IV. SIMULATION RESULTS

In this section the simulation results for the H-CL-P2SC with the parameters given in Table I is shown. The steady state simulation results under normal operation of the proposed converter are illustrated in Fig. 4.

The top figure shows the ac output voltage of the converter at the secondary side of the transformer. The ac current is calculated from the measured CL currents as in (9) at the secondary side of the transformer. The total harmonic distortion (THD) of the ac current is approximately 1.8%.

The mean value of the CL voltages is approximately 6.67 kV ($E_{dc}/3$) as expected. The mean value of the CL currents is equal to half of the dc current (-500 A).

As seen in Fig. 4 the capacitor voltages are well balanced. The mean value of the capacitor voltages is approximately 1.5 kV as this is the nominal capacitor voltage value. The capacitors have a ripple at the fundamental frequency (50 Hz).

Fig. 4. Steady state simulation plots for the H-CL-P2SC under normal conditions.

The transient response of the H-CL-P2SC to short circuit faults, working as a STATCOM, and response to the fault clearance are illustrated in Fig. 5. In this figure, the short circuit occurs at 1.5s while converter is running under normal conditions. After 150ms (at 1.65s), the reactive power reference is increased to the rated value (8MVar) in order to operate as a STATCOM. The fault is cleared at 1.7 s and the active power reference is ramped up to the rated value (20MW) in 100ms.

As seen in Fig. 5(a), the dc voltage drops to zero when the fault occurs. Just after the fault occurs, the cable current increases quickly as seen in Fig. 5(a). The peak current is approximately six times the dc current. However, this peak in the dc current does not pass through the converter as a result of its fault blocking capability.

No active power is delivered from the ac side to the dc side. However, the total energy controller is still able to regulate the power balance during the fault by generating a small amount of ac current to compensate the losses in the converter. The ac output current is fully controlled during the fault as seen in Fig. 5(b). The ac output voltage of the converter is adjusted accordingly to exchange reactive power with the grid.

An opposing voltage is generated in the CL voltages as the dc bus voltage drops to zero in the case of a P2P short circuit fault as shown in Fig. 5(b). The phase and the amplitude of these voltages are controlled to allow zero active power during the fault whilst still providing reactive power support. The average capacitor voltages in the CLs are regulated around the nominal cell voltage value.

Fig. 5. Transient response of the H-CL-P2SC to a dc P2P short circuit fault and the fault clearance. (a) Voltage and current components on the dc side. (b) Voltage and current components on the converter side.

V. CONCLUSION

A push-pull series connected ac-dc converter utilizing hybrid chain-links with dc fault blocking capability has been introduced in this paper. The operation and the modelling of the converter has been presented analytically. The analysis enabling the numerical comparison of the three converter topologies (H-CL-M2C, A2C, and H-CL-P2SC) has shown that the proposed converter potentially has a smaller converter footprint. The overall power and internal energy control strategies for the converter have been described in detail along with the supporting block diagrams. The operation of the converter has been validated using steady state simulation results for the converter under normal grid conditions. The simulation of a dc P2P short circuit has verified the dc fault blocking capability and the STATCOM operation of the H-CL-P2SC.

VI. DEDICATION

This paper is dedicated to the memory of our fellow researcher, friend and co-author, Dr Alessandro Costabeber. Alessandro was integral to the development of the topology described in this paper, and sadly died before the work could be completed.

REFERENCES

- [1] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for hvdc applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, 2015.
- [2] R. Marquardt, "Modular multilevel converter: An universal concept for hvdc-networks and extended dc-bus-applications," in *The 2010 International Power Electronics Conference - ECCE ASIA* -, 2010, pp. 502–507.
- [3] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for hvdc-transmission," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 174–179.
- [4] K. Friedrich, "Modern hvdc plus application of vsc in modular multilevel converter topology," in *2010 IEEE International Symposium on Industrial Electronics*, 2010, pp. 3807–3810.
- [5] P. Brestesi, W. L. Kling, R. L. Hendriks, and R. Vailati, "Hvdc connection of offshore wind farms to the transmission system," *IEEE Transactions on Energy Conversion*, vol. 22, no. 1, pp. 37–43, 2007.
- [6] E. Kontos, G. Tsolaridis, R. Teodorescu, and P. Bauer, "On dc fault dynamics of mmc-based hvdc connections," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 497–507, 2018.
- [7] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for hvdc systems based on various submodule circuits," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 385–394, 2015.
- [8] T. H. Nguyen, K. A. Hosani, M. S. E. Moursi, and F. Blaabjerg, "An overview of modular multilevel converters in hvdc transmission systems with statcom operation during pole-to-pole dc short circuits," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4137–4160, 2019.
- [9] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, and F. Hassan, "The alternate arm converter: A new hybrid multilevel converter with dc-fault blocking capability," *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 310–317, 2014.
- [10] M. M. C. Merlin, D. Soto-Sanchez, P. D. Judge, G. Chaffey, P. Clemow, T. C. Green, D. R. Trainer, and K. J. Dyke, "The extended overlap alternate arm converter: A voltage-source converter with dc fault ride-through capability and a compact design," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3898–3910, 2018.
- [11] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter," *IET Power Electronics*, vol. 8, no. 3, pp. 350–360, 2015.
- [12] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, 2015.
- [13] S. Cui and S. Sul, "A comprehensive dc short-circuit fault ride through strategy of hybrid modular multilevel converters (mmcs) for overhead line transmission," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7780–7796, 2016.
- [14] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1137–1146, 2015.
- [15] G. Tang, Z. Xu, and Y. Zhou, "Impacts of three mmc-hvdc configurations on ac system stability under dc line faults," *IEEE Transactions on Power Systems*, vol. 29, no. 6, pp. 3030–3040, 2014.
- [16] X. Yu, Y. Wei, and Q. Jiang, "Statcom operation scheme of the cdsm-mmc during a pole-to-pole dc fault," *IEEE Transactions on Power Delivery*, vol. 31, no. 3, pp. 1150–1159, 2016.
- [17] F. Tardelli, A. Costabeber, D. Trainer, and J. Clare, "Series chain-link modular multilevel ac-dc converter (scc) for hvdc applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5714–5728, 2020.