Active Modulation Strategy for Capacitor Voltage Balancing of Three-Level Neutral-Point-Clamped Converters in High-Speed Drives

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Abstract—In this paper, the equivalent relationship between the nearest-three-virtual space vector (NTV²) and carrier-based pulse-width-modulation (CBPWM) scheme is established based on space vector coordinate for a three-level neutral-point-clamped (3L-NPC) converter. Moreover, to solve the neutral-point (NP) voltage imbalance problem of the studied 3L-NPC converter-fed high-speed drives, an active modulation strategy with the generalized bias-offset injection technique is proposed. Meanwhile, the excessive computational burden is significantly overcome by the fast calculation approach. The effectiveness of the proposed modulation algorithm is validated through both simulation and experimental results obtained from a 45 kW, 32 krpm aircraft electric starter/generator (ESG) prototype system.

***Index Terms*—Capacitor voltage balance, generalized bias-offset injection, high-speed drives, more-electric-aircraft (MEA), three-level topology.**

I. INTRODUCTION

THE more-electric-aircraft (MEA) has become a cutting-edge technology over the last decade because of more expected fuel efficiency, better environmental impact and less maintenance cost [1]-[3]. It aims at reducing the number of pneumatic, hydraulic and mechanical systems in favor of their electrical counterparts [4]-[6]. State-of-the-art starter/generator (S/G) systems employ three-stage wound-field synchronous generators [7]. Nevertheless, several defects constrain its development. For example, high-speed rotation (over 20 krpm) may result in mechanical failure due to its wound rotor embedded with rotating diodes. In contrast, the ESG system opens opportunities for applying new machine types that are free from mentioned limitations and allows for novel design of high-performance S/G system in MEA [8]. To enable active rectification technology in aircraft, two sets of S/G take power from the main engine through high pressure (HP) shaft and low pressure (LP) shaft and operate in parallel to transfer the power to the aircraft DC-bus. The entire system primarily consists of a high-speed machine and a bidirectional power converter with bipolar DC voltage output, as shown in Fig.1. More specifically, the permanent magnet synchronous machine (PMSM) is chosen
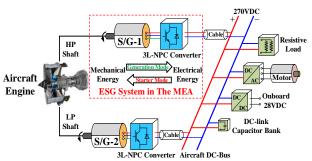
Fig. 1. Configuration of the studied ESG system in the MEA.

due to its high torque-to-current ratio, high power density and high robustness. Although increasing the numbers of pole can sometimes increase the efficiency of machine, high operational speed leads to a high fundamental frequency, thereby resulting in low carrier-pulse ratio issue [9]. With this consideration, a 6-poles 36-slots machine is chosen as the optimal candidate which also has the lowest eddy-current losses [8]. Owing to lower voltage stress across semiconductor devices, reduced EMI emission and better output harmonics, three-level neutral-point-clamped (3L-NPC) topology shown in Fig.2, instead of two-level converter, is selected for the considered system. Although active NPC (ANPC) structure gains the advantage of more commutation paths, thereby attaining evenly distributed losses among switching devices [10]. However, additional devices and complicated gate driver design are adverse for the laboratory-developed converter at the initial stage. T-type NPC (TNPC) benefits for minimum semiconductors, but outer switches must be rated to block full DC-link voltage [11]. It means that this topology is normally applied in low-power applications. Consequently, the diode-clamped NPC (DNPC) converter [12] is manufactured for the aircraft ESG prototype system.

In the developed ESG system, the PMSM is mechanically coupled to the engine shaft via a gearbox, and electrically connected with a 3L-NPC converter which interfaces S/G system to the onboard electric power system (EPS). During engine startup process, the power converter runs as an inverter which drives the PMSM to crank and accelerate the engine shaft. Once the engine reaches a self-sustaining speed, the fuel and air mixture is ignited. After that, the ESG system goes into standby mode, followed by generation mode when the PMSM shaft speed (linked to the engine speed via gearbox ratio) approaches 20 krpm. In the generation mode, the engine drives the PMSM to generate electrical power, and the power converter is operated as a rectifier to convert this variable frequency AC power into DC and to supply the onboard EPS.

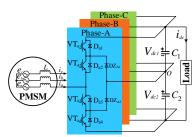As the 3L-NPC converter serves as a crucial component in

Fig. 2. The topology of 3L-NPC power converter.

the main path of energy flow in our studied ESG system, it has a significant influence on the reliability and efficiency of entire EPS system. But the selected topology has the inherent problem of unbalanced NP voltage due to split DC-link capacitors. The NP potential drift and oscillation issue cause extra over-stress across switches, and also lead to low-order harmonics on the motor side. Even though self-equilibrium phenomenon can be observed and analyzed, its strength is constrained by system parameters, PWM patterns and sampling frequency [13], [14].

To address the aforesaid disadvantage, several advanced modulation techniques have been developed by researchers [15]-[32]. These methods can be classified into two categories: 1) space vector modulation (SVM) scheme [15]-[22] and 2) carrier-based PWM (CBPWM) scheme [25]-[32]. Based on the unbalanced range of capacitor voltages, an improved nearest-three-vector (NTV) scheme has been presented in [15], where a NP voltage feedback control loop is added to determine a predefined switching sequence only composed by P-type or N-type small vector. But it cannot avoid undesirable low-frequency NP voltage oscillation generated by medium vector for the reason of its predominant participation. In [16], a modified modulation scheme abandons medium vectors to balance NP potential and suppress the oscillation. The concept of the nearest-three-virtual space vector (NTV^2) modulation scheme is firstly proposed in [17]. This technique aims to produce average zero NP current during a switching period, which can guarantee balanced capacitor voltage in all range of modulation index and power factor. It should point that, without capacitor voltage balancing control, the original method cannot provide compensated electric charges in the NP if an initial capacitor voltage error exists in the DC-link unexpectedly, thereby constraining its practical application. The study reported in [18] brings an opportunity to keep two capacitor voltages balanced with DC-link voltage feedback control, but subsector identification and dwell time determination are executed in the α-β reference frame. This indicates that trigonometric functions are required to calculate in a PWM interrupt service, which causes complexity for the digital controller. In the work of [19], an improved NTV^2 scheme has been explored, which features simple subsector repartition. Besides, the NTV^2 technique has been well developed to incorporate more advantages, such as common-mode-voltage (CMV) suppression [20] and switching losses reduction [21]. In order to select optimal virtual space vector with fast dynamic response, a more recent study by [22] proposes a discrete space vector modulation (DSVM) scheme based on model predictive control (MPC). However, it is notable that total harmonic distortion (THD) of phase current highly depends on the

number of virtual switching states [23]. More importantly, heavy computational burden, with 33 switching states, is another challenge for the method. In order to simplify the calculation process, reference [24] proposes vector shifted model to reduce execution time for MPC controller.

Compared with SVM scheme, CBPWM scheme is carried out because of its simplicity and easy implementation. In [25], an optimized zero-sequence voltage (ZSV) injection method is presented for balancing capacitor voltage. In [26], a voltage-offset injection solution is reported for a single-phase 3L-NPC converter. A method based on discontinuous PWM (DPWM) strategy has been proposed for mitigated NP voltage oscillation and less switching losses in high-power applications [27]. Despite that, the effectiveness of these modulation schemes are still limited since the manipulated NP current becomes insufficient under lower power factor conditions. In [28], a novel CBPWM scheme with appropriate ZSV injection offers a chance to operate traction drives in overmodulation region. To pursuit balanced NP voltage and power loss reduction, a flexible CBPWM method is proposed in [29]. In [30], NP variation range is compromised to reduce switching losses. Furthermore, SVM-based CBPWM algorithms have been explored from ZSV injection viewpoint, thereby settling the imbalance issue [31], [32]. However, in terms of the equivalent relationship between two main modulation methods mentioned above, the derivation result based on the position of reference space vector is not revealed. Also, none of the existing methods in the literature can deliver desirable performance for high-speed aerospace drives under stringent operating conditions.

In this paper, an active modulation technique is studied for capacitor voltage balancing of 3L-NPC converters for the aircraft ESG system featured with a higher fundamental frequency in the MEA applications. With the established reference frame transformation, the NTV^2 and CBPWM scheme can be unified. With the proposed generalized bias-offset injection (GBOI) technique, NP voltage drift problem can be easily addressed, especially for initial capacitor voltage imbalance in high modulation index and low power factor operation. Meanwhile, the bias-offset injection (BOI) process is simplified, hence, the heavy computational burden can be drastically overcome. The conventional NTV and CBPWM schemes are chosen as the benchmark method to evaluate the performance of the presented scheme in the following.

This paper is organized as follows. The principles of ESG system are introduced in Section II. The NP voltage balance issue of 3L-NPC converter is analyzed in Section III. The fast calculation approach is presented in Section IV. Section V gives the details of the proposed modulation strategy. Simulation and experimental results are presented in Section VI-VII. Finally, Section VIII summarizes the main conclusions of this study.

II. PRINCIPLES OF ESG SYSTEM

A. Control Design of ESG System

The ESG control system shown in Fig.3 involves flux-weakening control, machine speed control and DC-link current control. Speed control is activated in starter mode and DC-link current is manipulated by droop characteristics in generation
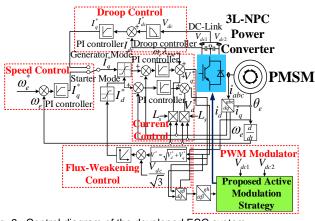
Fig. 3. Control diagram of the developed ESG system.

TABLE I
SWITCHING PRINCIPLE OF 3L-NPC CONVERTER

| Switching State | Switch Status | | | | V'_{mx} & V_{ci} ($V_{c1} > V_{c2}$) | Output Voltage Level |
	VT_{x1}	VT_{x2}	VT_{x3}	VT_{x4}		
P	1	1	0	0	$V'_{mx} > V_{c1}$	$V_{dc}/2$
O	0	1	1	0	$V_{c1} > V'_{mx} > V_{c2}$	0
N	0	0	1	1	$V'_{mx} < V_{c2}$	$-V_{dc}/2$

mode. Vector control technique is used for machine decoupling purpose, which allows to control flux and torque independently. Thus, machine torque represented as active power is controlled by q-axis current. Large negative d-axis current is needed at high-speed operation, which causes lower power factor.

B. Three-Level NPC Converter, Conventional NTV, Carrier-Based PWM and NTV² Scheme

As can be seen from Fig.2, each phase comprises four IGBTs ($VT_{x1} \sim VT_{x4}$) and two clamped-diodes (DZ_{x1} and DZ_{x2}), where $x = \{A, B, C\}$. Two equal capacitors (C_1 and C_2) are series-connected to form the DC-link. The output AC-side voltage generates three levels ($\pm V_{dc}/2$ and 0). For a 3L-NPC converter, 27 switching states can be produced, which are represented as P, O and N. When VT_{x1} and VT_{x2} are turned on, the switching state is denoted as P and output voltage level is $V_{dc}/2$. The switching state O indicates that VT_{x2} and VT_{x3} are turned on, which produces zero voltage. The switching state N manifests that VT_{x3} and VT_{x4} are turned on and output voltage is $-V_{dc}/2$. Noted that VT_{x1} is complimentarily switched with VT_{x3}, while VT_{x2} and VT_{x4} follow the same manner. These combinations can be categorized as zero, small, medium and large vectors, wherein small ones are 12 while the number of large ones and medium ones are both 6, and the rest belongs to zero vectors.

Assuming that the reference space vector is located in the subsector 4 of Sector-I, as shown in Fig.4(a). Conventional NTV scheme uses a small vector [PPO] or [OON], a medium vector [PON] and a large vector [PPN] to synthesize V_{ref}. Based on the volts-second principle, (1) and (2) can be obtained as:

$$V_{ref} = V_2 \cdot d_1 + V_3 \cdot d_2 + V_5 \cdot d_3 \qquad (1)$$

$$d_1 + d_2 + d_3 = 1 \qquad (2)$$

where V_2, V_3 and V_5 are nearest-three small, medium and large vectors labeled with number shown in Fig.4(a). d_1, d_2 and d_3 represent the corresponding duty cycle of these space vectors.

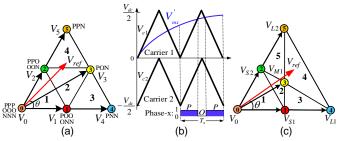It is known that CBPWM scheme is essentially equivalent to

Fig. 4. Conventional modulation schemes for 3L-NPC power converter. (a) NTV scheme. (b) CBPWM scheme. (c) NTV² scheme.

SVM method by injecting ZSV into three-phase sinusoidal modulation waveforms, which can be written as:

$$\begin{cases} V'_{ma} = V_{ma} + V_z = m \cdot \cos(\theta) + V_z \\ V'_{mb} = V_{mb} + V_z = m \cdot \cos(\theta - 2\pi/3) + V_z \\ V'_{mc} = V_{mc} + V_z = m \cdot \cos(\theta + 2\pi/3) + V_z \end{cases} \qquad (3)$$

where m is the modulation index defined by (4), θ denotes reference space vector rotating angle and V_z represents zero-sequence voltage.

$$m = \frac{\sqrt{3} V_{ref}}{V_{dc}} \qquad (4)$$

The comparison between SVM and CBPWM scheme is shown in Fig.4(b). As shown, switching state is P when V'_{mx} is larger than V_{c1} and V_{c2}, and switching state can be obtained as O when V'_{mx} is smaller than V_{c1} but larger than V_{c2}, where $x = \{a, b, c\}$. Otherwise, switching state is N. Based on that mechanism, CBPWM scheme generates firing pulses to semiconductor devices. The switching principle is summarized in Table I.

In the case of NTV² scheme, as shown in Fig.4(c), the selection of zero and large vectors denoted as V_0, V_{L1} and V_{L2} are the same with NTV method. However, V_{S1}, V_{S2} and V_{M1} are virtual small and medium vectors, respectively, which are defined as follows:

$$\begin{cases} V_{S1} = (V_{POO} + V_{ONN})/2 \\ V_{S2} = (V_{PPO} + V_{OON})/2 \\ V_{M1} = (V_{ONN} + V_{PON} + V_{PPO})/3 \end{cases} \qquad (5)$$

As seen from (5), virtual small vectors evenly allocate P-and N-type basic small vectors, and therefore produce average zero NP current. Similarly, virtual medium vector also has no impact on NP potential since the sum of NP currents generated by [ONN], [PON] and [PPO] equals to zero ($i_a + i_b + i_c = 0$). This denotes that NTV² scheme is capable of dealing with NP potential drift problem for all loads.

III. ANALYSIS OF NEUTRAL-POINT VOLTAGE IMBALANCE AND OSCILLATION ISSUE

A. The Effect of NP Current

The switching states signify different types of switches connected to the DC-link, which, in turn, determine the magnitude and direction of NP currents. As can be seen in Fig.4(a), any space vectors can be composed by one or more combinations of different switching states. The corresponding relationship among space vectors, switching states and NP currents are listed in Table II, in which zero and large vectors

TABLE II
SPACE VECTORS, SWITCHING STATES AND NP CURRENTS OF 3L-NPC
CONVERTER

Space Vectors	Switching States		NP Currents	
Zero Vector	[PPP] [OOO] [NNN]		-	
	P-type	N-type	P-type	N-type
	[POO]	[ONN]	$-I_a$	I_a
	[PPO]	[OON]	I_c	$-I_c$
Small Vector	[OPO]	[NON]	$-I_b$	I_b
	[OPP]	[NOO]	I_a	$-I_a$
	[POP]	[ONO]	I_b	$-I_b$
	[OOP]	[NNO]	$-I_c$	I_c
	[PON]		I_b	
	[OPN]		I_a	
	[NPO]		I_c	
Medium Vector	[NOP]		I_b	
	[ONP]		I_a	
	[PNO]		I_c	
Large Vector	[PNP] [PPN] [NPN] [NPP] [NNP] [PNP]		-	

have no influence on NP voltage as there is no current associated with the center tap of DC-link. For small vectors, the NP currents associated with two redundant switching states are complimentary with opposite directions. Each medium vector is only associated with one switching state and therefore one type of NP current. It means that medium vectors have special impact on capacitor voltage, which cannot be offset by itself.

The specific switch connections used to synthesize V_{ref} shown in Fig.4(a) are displayed in Fig.5, in which, except the large vector [PPN], other space vectors affect two capacitor voltages. The average current flowing into and out of the NP during a switching cycle is given by:

$$\overline{I_{NP}} = D \cdot I_{abc} \qquad (6)$$

where $D = [(d_{onn} - d_{poo})\ d_{pon}\ (d_{ppo} - d_{oon})]$ and $I_{abc} = [i_a\ i_b\ i_c]^T$.

According to switching states and NP currents specified in Table II, the above equation can be attained as:

$$\overline{I_{NP}} = \mu \cdot d_{ppo} \cdot i_c + d_{pon} \cdot i_b + (1-\mu) \cdot d_{oon} \cdot (-i_c),\ \mu \in [0,\ 1] \quad (7)$$

where μ is the distribution ratio of [PPO] and [OON].

With (7), through properly selecting coefficient μ, two small vectors can be proportionally employed to compensate NP potential charge or discharge incurred by medium vector in each switching cycle. Further, NP potential deviation can be calculated as:

$$\Delta V_{dc} = \frac{1}{C} \int_{t=0}^{t=T_s} \overline{I_{NP}} \cdot dt \qquad (8)$$

where C represents the capacitance of DC-link and T_s denotes a switching period.

From (6)-(8), normalized amplitude of NP voltage charge yielded by small vector can be calculated and shown in Fig.6(a). Noted that the normalization factor is the maximum accumulated neutral-point electric charge produced by space vectors under the unity phase current. As shown, the NP potential charged by small vector becomes smaller when modulation index rises and power factor drops down, which indicate it is harsh to offset the impact of medium vector in these regions. Thus, such operation scenario indicates the
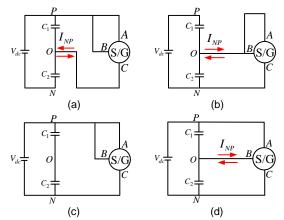

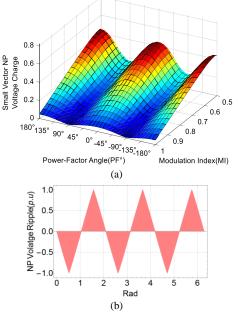Fig. 5. The effect of space vector on NP current. (a) [PPO]. (b) [OON]. (c) [PPN]. (d) [PON].

(a)

(b)

Fig. 6. (a) Normalized amplitude of NP voltage charged by small vectors. (b) Normalized NP voltage oscillation (m=1 and φ=90°).

unfavorable working condition of the applied 3L-NPC converter in our ESG system and requires special attention.

B. Source of NP Voltage Oscillation

It is assumed that phase currents of ESG system are balanced, hence, three-phase currents are as follows:

$$\begin{cases} i_a = I_o \cos(\omega t - \varphi) \\ i_b = I_o \cos(\omega t - \varphi - 2\pi/3) \\ i_c = I_o \cos(\omega t - \varphi + 2\pi/3) \\ i_a + i_b + i_c = 0 \end{cases} \qquad (9)$$

where ω is angular frequency, I_o denotes magnitude of phase current and φ indicates power factor angle.

The average current flowing to the center tap of DC-link within a carrier period meets:

$$\begin{cases} \overline{I_{NP}} = \sum_{x=a,b,c} d_{xo} \cdot i_x \\ 0 \leq d_{xo} \leq 1 \end{cases} \qquad (10)$$

where d_{xo} is the phase duty cycle of switching state O.

TABLE III
THE SUBSECTOR IDENTIFICATION CRITERIA IN SECTOR-1

Subsector	Identification Criteria
1	$0 < V_g + V_h \leq 0.5$
2	$V_g + V_h > 0.5$ && $V_h + 2V_g \leq 1$ && $0.5V_g + V_h \leq 0.5$
3	$V_h + 2V_g > 1$ && $0.5V_g + V_h < 0.5$ && $V_h \geq 0$
4	$V_{g1} + V_{h1} < 1$ && $V_{h1} + 2V_{g1} \geq 1$ && $0.5V_{g1} + V_{h1} \geq 0.5$
5	$V_{g1} \geq 0$ && $0.5V_{g1} + V_{h1} > 0.5$ && $V_{h1} + 2V_{g1} \leq 1$

TABLE IV
THE DUTY CYCLE EXPRESSIONS IN SECTOR-1

Subsector	d_1	d_2	d_3
1	$2g$	$2h$	$1-2(g+h)$
2	$2(1-g-2h)$	$2(1-h-2g)$	$3[2(g+h)-1]$
3	$2(1-2h-g)$	$2g+h-1$	$3h$
4	$3(1-g-h)$	$2g+h-1$	$2h+g-1$
5	$2(1-2g-h)$	$2h+g-1$	$3g$

As the frequency of carrier waveform is much higher than that of modulation waveform, the relationship between d_{xo} and V'_{mx} is given by:

$$d_{xo} = 1 - \left| V'_{mx} \right|, \quad x = \{a, b, c\} \tag{11}$$

The NP voltage variation can be therefore quantified by substituting (9)-(11) into (8) in a fundamental period. As shown in Fig.6(b), the low-frequency NP voltage oscillation features three times of fundamental frequency, which has a negative impact on the lifetime of capacitor, and also has detrimental effects on the stability of EPS. Although this drawback can be suppressed by large capacitor or isolated DC voltage source, extra cost and bulky size are inevitable for the converter design. In general, the balanced NP voltage with eliminated oscillation is crucial for high-speed motor drives in aerospace applications.

IV. FAST CALCULATION APPROACH OF PWM SIGNALS

Due to the superiority of balanced capacitor voltages, here, the NTV^2 scheme is taken as a candidate to introduce the fast PWM signals calculation approach.

Assuming that the reference space vector is located in subsector 4 of the first sector built in the traditional α-β reference frame, as shown in Fig.4(c), the solutions derived from (1) and (2) are as follows:

$$\begin{cases} d_1 = 3[1 - m \cdot \sin(\pi/3 + \theta)] \\ d_2 = \sqrt{3}m \cdot \cos\theta - 1 \\ d_3 = \sqrt{3}m \cdot \sin(\pi/6 + \theta) - 1 \end{cases} \tag{12}$$

where d_1, d_2 and d_3 represent the duty cycles of V_{M1}, V_{L1} and V_{L2}, respectively.

It is clearly seen that apart from complex subsector repartition compared with the NTV scheme, cumbersome dwell time calculation by (12) causes excessive computational burden for the implementation of digital control system. Hence, a simplified solution needs to be established before presenting the proposed active modulation algorithm afterward.

A. Reference Frame Transformation

Transformation matrix defined in (13) shifts β-axis in clockwise by 30° to configure a new plane of space vector diagram (SVD), as shown in Fig.7.
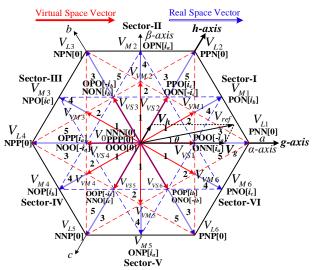

Fig. 7. Fast calculation-based SVD for 3L-NPC converter.

$$\begin{bmatrix} V_g \\ V_h \end{bmatrix} = \begin{bmatrix} 1 & -\dfrac{1}{\sqrt{3}} \\ 0 & \dfrac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{13}$$

where V_g and V_h are the magnitude of space vector in g-h frame.

B. Subsector Identification and Dwell Time Calculation

Similar to (1) and (2), the duty cycle of each vector associated with NTV^2 scheme satisfies:

$$V_{ref} = V_x \cdot d_1 + V_y \cdot d_2 + V_z \cdot d_3 \tag{14}$$

where V_x, V_y and V_z represent nearest-three virtual space vectors.

By projecting (14) into this new reference frame, the volts-second principle can be re-written as:

$$\begin{cases} V_g = X_g d_1 + Y_g d_2 + Z_g d_3 \\ V_h = X_h d_1 + Y_h d_2 + Z_h d_3 \end{cases} \tag{15}$$

where (V_g, V_h), (X_g, X_h), (Y_g, Y_h) and (Z_g, Z_h) are the coordinates of V_{ref} and virtual space vectors in g-h plane, respectively.

For the computationally-efficient purpose, the coordinates of all space vectors are normalized with respect to the magnitude of large vector $(2/3V_{dc})$. Thus, (V_g, V_h) can be conveniently expressed as (g, h) in following deductions. For instance, $(1, 0)$ is the coordinate of V_{L1} in g-h plane.
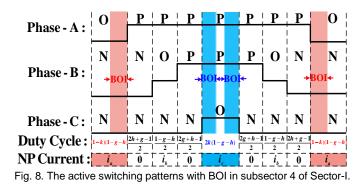
The full identification criteria of subsector number are derived in Table III. Table IV shows the simplified duty cycle expressions of the nearest-three virtual space vectors in each subsector of Sector-I.

V. PROPOSED ACTIVE MODULATION STRATEGY

To achieve active DC-link capacitor voltage balancing and suppress NP voltage oscillation for applied 3L-NPC converter in the ESG system, NTV^2 scheme is firstly modified by the proposed technique based on the fast calculation approach. And then, the method is further extended to CBPWM scheme. The detailed descriptions of each part are provided in the following.

A. Generalized Bias-Offset Injection Technique

Capacitor voltages drift reflects extra electric charge in the last control period, with (8), the required NP potential charge

Fig. 8. The active switching patterns with BOI in subsector 4 of Sector-I.

or discharge to mitigate NP imbalance within a sampling time is calculated as:

$$0 = C \cdot \Delta V_{dc} + \Delta Q \tag{16}$$

where $\triangle Q$ is defined as the compensated charge.

Since the 3L-NPC converter in our studies is connected to an aircraft electric S/G, the divergence of NP potential is related to motor or generator mode of converter-fed machine drives. In startup process, NP potential raises with more participation of P-type small vector. On the contrary, NP potential drops down with more utilization of P-type small vector in generation mode and vice versa.

As a result, in accordance with operation mode of the ESG system, NP voltage deviation can be actively balanced by offsetting a bias in the switching interval of small vectors. Subsector 4 of the first sector displayed in Fig.4(c) is considered as a representative case to study. The active switching pattern with the presented algorithm is shown in Fig.8. Red and blue shadow bars refer to the injected bias-offset areas. Further, the compensated charge can be derived as:

$$\Delta Q = (T_1 + T_{BOI}) \cdot i_a + T_3 \cdot i_b + (T_2 - T_{BOI}) \cdot i_c \\ = (1 - 2k) \cdot (1 - g - h) \cdot (i_a - i_c) \cdot T_s \tag{17}$$

where T_1, T_2 and T_3 are the dwell time for clamping phase-A, B and C to the midpoint of DC-link, and T_{BOI} is the injected bias-offset value in time domain. The coefficient k indicates capacitor voltages deviation range and is defined by:

$$k = \frac{V_{dc1}}{V_{dc1} + V_{dc2}} \in [0, \ 1] \tag{18}$$

On the other hand, voltage-domain injection for CBPWM scheme can be reversely calculated and carried out by the active switching patterns, as shown in Fig.9. It is noted that, due to three-level clamping during a switching period illustrated in Fig.8, the reference modulation signal of phase-B has to be decomposed before comparing with double carrier waveforms, which can be expressed as follows:

$$\begin{cases} 2V_{b1}^* \cdot T_s / V_{dc} = [1 - (1 - g - h) - (2g + h - 1) - (1 - g - h)] \cdot T_s \\ -2V_{b2}^* \cdot T_s / V_{dc} = [(2g + h - 1) + (1 - g - h)] \cdot T_s \end{cases} \tag{19}$$

where V_{b1}^* and V_{b2}^* are two decomposition modulation waves.

Moreover, except the decomposed one, the magnitude of modulation signals of phase-A and C are both offset in each magnitude, which can be calculated as follows:

$$2V_a^* \cdot T_s / V_{dc} = [1 - 2(1 - k)(1 - g - h)] \cdot T_s \tag{20}$$

$$-2V_c^* \cdot T_s / V_{dc} = [1 - 2k(1 - g - h)] \cdot T_s \tag{21}$$
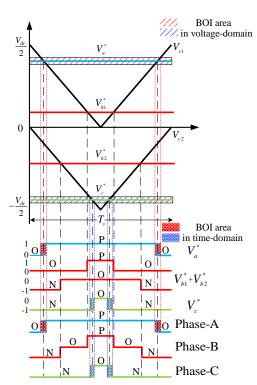

Fig. 9. The relationship between the active switching patterns and modulation waves based on the proposed strategy.
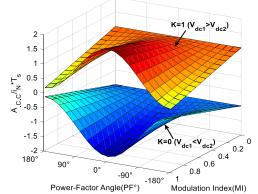

Fig. 10. NP voltage balancing control capability of the proposed strategy.

Thus, the modulation voltages can be further written as:

$$\begin{cases} V_a^* = V_{dc} / 2 \cdot [1 - 2(1 - k)(1 - g - h)] \\ V_{b1}^* = V_{dc} / 2 \cdot h \\ V_{b2}^* = -V_{dc} / 2 \cdot g \\ V_c^* = -V_{dc} / 2 \cdot [1 - 2k(1 - g - h)] \end{cases} \tag{22}$$

B. NP Voltage Control Performance Analysis

The capacitor voltage balancing control capability of the proposed method is defined as $A_{c.c.}$. Therefore, the compensated charge in subsector-4 of Sector-I is yielded as:

$$A_{c.c} = \Delta Q = (1 - 2k) \cdot [1 - m\sin(\frac{\pi}{3} - \theta) - m\sin(\theta)] \cdot I_{rms} \\ \cdot T_s [\cos(\theta - \varphi) - \cos(\theta + \frac{2\pi}{3} - \varphi)] \tag{23}$$

where I_{rms} is the phase current root-mean-square (RMS) value.

Consequently, the average active NP voltage control capability during a fundamental cycle can be calculated as:
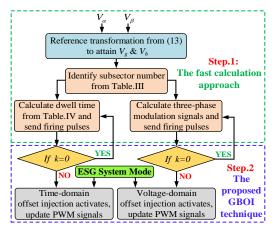
Fig. 11. Flowchart diagram of the proposed active modulation strategy.

TABLE V
ESG SYSTEM PARAMETERS

Parameters	Value
$L_d = L_q$	99 μH
Pole pair	3
Switching/Carrier frequency	16 kHz
PM flux	0.03644 V_s/rad
Base speed	8000 rpm
Control system sampling frequency	16 kHz
Fundamental frequency in generation mode	1~1.6 kHz
Capacitor value ($C_1=C_2$)	600 μF
DC-link voltage	270 V

$$\frac{\overline{A_{c.c}}}{I_{rms}T_s} = \frac{1}{2\pi}\int_0^{2\pi}\frac{A_{c.c}(\theta)}{I_{rms}T_s}\cdot d\theta \qquad (24)$$

For the worst condition, V_{dc1} or V_{dc2} equals to DC-link voltage, which refers to $k = 0$ or 1. As shown in Fig.10, the voltage across each capacitor can be actively balanced in entire range of modulation indices and power factor angles.

In this work, (17) and (22) are defined as the GBOI technique implemented with the fast calculation approach. It can be clearly seen that NTV^2 and CBPWM scheme have been unified in the form of reference space vector position. In the case of other sectors, a similar derivation process can be performed. Fig.11 shows the flowchart diagram of the proposed strategy.

VI. SIMULATION RESULTS

For comparing the performance of the proposed modulation strategy with the benchmark method. The simulated ESG system given in Fig.3 is built in Simulink/PLECS and the parameters are listed in Table V.

A. Capacitor Voltage Balancing Performance

Initially, the ESG system runs in starter mode, and flux-weakening control is operated at 0.5s. With engine ignition, the speed of PMSM reaches to 20 krpm. Power generation starts by connecting a 5 kW resistive load to the DC-link at 1s and droop control takes over DC-link voltage regulation at the same time.

As shown in Fig.12, PMSM speed diagram describes the status of the ESG system in every stages. With the speed of machine increasing, the benchmark method incurs unbalanced upper and lower-side capacitor voltages (V_{DC}-H/V_{DC}-L) after 0.8s, as shown in Fig.13(a). However, two capacitor voltages can be quickly recovered after employing the proposed strategy
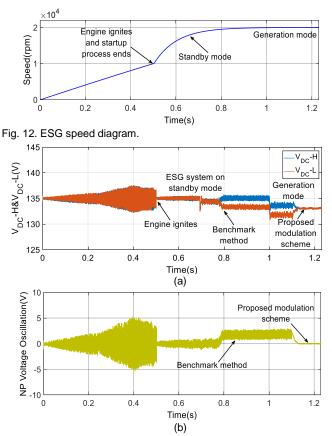

Fig. 12. ESG speed diagram.

(a)

(b)

Fig. 13. Simulation results of the benchmark method and proposed scheme. (a) DC-link capacitor voltages. (b) NP voltage oscillation.
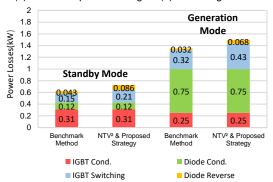

Fig. 14. Comparison of power losses distribution of different modulation schemes under two operating conditions.

at 1.1s. Furthermore, the magnitude of NP voltage oscillation is also significantly mitigated, as shown in Fig.13(b).

B. Power Losses Analysis

The power losses is performed by the applied Infineon F3L400R07ME4_B22/B23 insulated-gate bipolar transistor (IGBT) module which has the maximum collector-emitter voltage of 650V and continuous collector current of 400A, which is capable of withstanding required phase current as well as surge voltage for our application. Based on a curve from the manufacturer's datasheet, the energy dissipated can be calculated in every turn-on (E_{on}) and turn-off (E_{off}) of switching devices as a function of the current. With loss equations and these data, switching losses and conduction losses of the IGBTs and diodes can be obtained under different modulation schemes.

Here, the power losses are carried out when the ESG system

operates in standby mode and power generation of 25 kW at 20 krpm, and the switching frequency is set to be 16 kHz. Fig.14 shows the total losses distribution of the benchmark method, NTV^2 scheme and the proposed strategy. It can be seen that the amount of conduction losses produced by these approaches are the same in each case and the switching losses by the proposed modulation technique are higher than the amount by benchmark method, whereas the amount is the same as that of NTV^2 scheme. This is because one of phase switches to the NP and positive/negative rail of the DC-link, which results in extra commutation number within a switching or carrier period. However, it facilitates trade-off for balancing capacitor voltage and eliminating NP voltage oscillation.

C. Comparison With Other NP Voltage Balancing Control-Based Modulation Schemes

Compared with the existing NP voltage balancing control schemes for motor drives presented in [16], [18], [28] and [29]. The proposed active modulation strategy brings the following attractive features:

1) The proposed modulation strategy applies NTVs to synthesize the reference voltage vector. As a result, the output distortion by the proposed algorithm is less than that of the method in [16]. In contrast, in order to eliminate the NP voltage oscillation caused by medium vectors, the scheme presented in [16] utilizes non-nearest three vectors to configure the dedicated pulse train.

2) The fast calculation approach adopted in the proposed modulation strategy overcomes the excessive computational burden. Compared with [18], the subsector identification criteria of presented method is simple. In addition, the technique uses algebraic functions instead of sinusoidal ones. These benefit computation efficiency in the digital controller.

3) The presented modulation strategy only leads to two switches transition from one switching state to the next in the same phase leg. Nevertheless, the methods in [16] and [18] indicates that the active NP voltage control is realized at the expense of the directive commutation path through positive to negative DC-rail, particularly for the operating conditions in a high modulation index region.

4) With the help of the equivalent derivation, the proposed NP voltage balance control method can be realized with simple expressions. However, appropriate ZSV signals in [28] and [29] are injected to tackle the imbalance issue.

However, similar to [18], because of three-level voltage instants during a switching cycle, the proposed strategy trades the reduced NP voltage oscillation against the extra switching losses as compared to [16], [28] and [29].

VII. EXPERIMENTAL RESULTS

The proposed modulation strategy is verified by a 45 kW, 32 krpm ESG system prototype, as shown in Fig.15. Mechanically, the prime mover emulates aircraft engine shaft and is coupled with the PMSM. 150 kW prime mover and machine are located in an isolated room for the safety consideration. The 3L-NPC converter along with a digital control platform, prime mover controller, host PC and DC source are placed outside the high-speed room. The grid-tied source sink (GSS) mimics the aircraft EPS of 270VDC. Air-cooling fans are installed underneath the
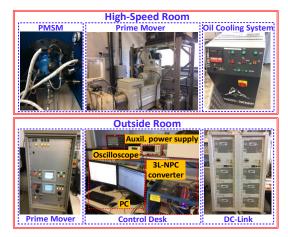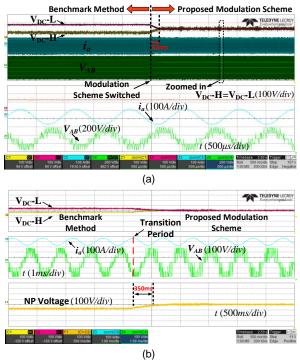

Fig. 15. ESG system test rig.

(a)

(b)

Fig. 16. Transition period from the benchmark method to the proposed modulation scheme at (a) m=0.82 and φ=0.46. (b) m=0.95 and φ=0.12.

heat-sink of the converter. TT-OIL300 is used as the cooling system for the high-speed aerospace machine. The control board includes DSK6713 and Actel FPGA-ProAsic3 A3P400. AC-side parameters are monitored by a PPA5530 precision power analyzer. Since the direction of phase current changes rapidly in light-load condition, it weakens the ability of NP voltage balancing. Thus, experimental tests primarily focus on the ESG system operating in light-load condition in generation mode. The results in the startup process are not presented here because of its short duration compared with the whole period. In the following tests, all the variables are measured by high voltage differential probes and CP500 current probes displayed on a Teledyne LeCroy oscilloscope.

A. Initial Capacitor Voltage Imbalance

The experimental results with respect to capacitor voltage balance are obtained in generation mode at 20 krpm. The q-axis command current is -15A. The average modulation index and
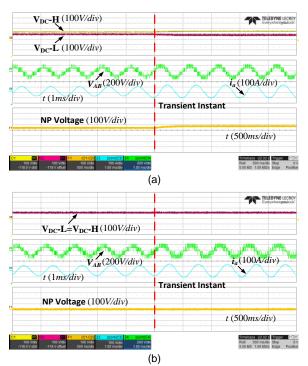
(a)

(b)

Fig. 17. NP voltage control performance during the loading process. (a) The benchmark method. (b) The proposed active modulation strategy.
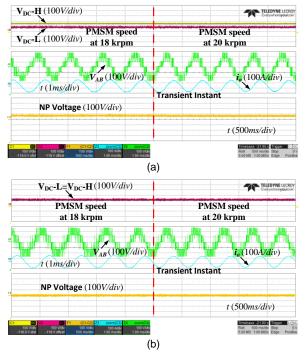

(a)

(b)

Fig. 18. NP voltage control performance during the change of speed. (a) The benchmark method. (b) The proposed active modulation strategy.

power factor in that operation are 0.82 and 0.46, respectively. As seen from zoomed-in waveform in Fig.16(a), after switching to the proposed modulation scheme, NP voltage can be quickly maintained balanced again within 42 ms. The transition period at the average modulation index of 0.95 and power factor of 0.12 is shown in Fig.16(b). As shown, a static error exists between two capacitor voltages and the phase voltage is distorted under the benchmark method. While NP potential drift can be recovered within 350 ms under the presented technique.
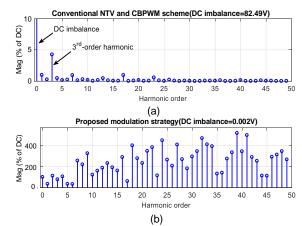

(a)

(b)

Fig. 19. The FFT analysis of NP voltage oscillation. (a) The benchmark method. (b) The proposed modulation scheme.
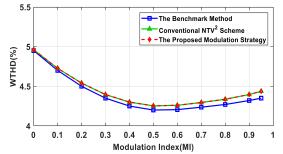

Fig. 20. WTHD of the line-to-line voltage at different modulation indices with the modulation techniques.

B. Transient-State Experiments

To validate the dynamic performance of the proposed modulation strategy, the load and machine speed are changed suddenly. The first scenario represents the q-axis command current increases from -5A to -25A in the power generating mode. It can be seen from Fig.17(a) that the NP voltage severely shifted with the benchmark method during the transient process. In contrast, two capacitor voltages can effectively maintain balanced under this situation by the proposed strategy, as shown in Fig.17(b). Moreover, the proposed active capacitor voltage control is tested when the average machine speed is ramping up from 18 krpm to 20 krpm. This scenario indicates that the fundamental frequency of the PMSM is increased from 900 Hz to 1 kHz. The results from Fig.18(a) shows that the benchmark method always causes NP potential imbalance in the case of speed changing condition. However, the deviated capacitor voltage can be well controlled by the presented active modulation technique under this process, as shown in Fig.18(b). Hence, the dynamic performance of the proposed algorithm has been improved as compared to the conventional PWM schemes.

C. Distortion Analysis

Harmonic content of the NP voltage oscillation with the FFT analysis is shown in Fig.19. As shown, not only DC imbalance is effectively eliminated, but also the magnitude of low-frequency NP voltage oscillation, including 3rd-order harmonics, is reduced. THD of phase current with the benchmark and the proposed methods are 4.85% and 5.73%, respectively.

Fig. 20 shows the weighted THD (WTHD) comparison of the line-to-line voltage under different modulation strategies. At lower modulation indices, the curves are similar for each

method. When modulation index increases, compared with benchmark method, that value by both NTV^2 and the proposed modulation strategy slightly increases harmonic distortion, which is due to the three-level switching instant.

D. Computational Performance

The execution time of the proposed strategy is tested by the controller kit and the result shows that the time-domain and voltage-domain injection method costs 56.8 μs and 46.3 μs, respectively. In comparison with typical implementations in the traditional *α-β* reference frame, the corresponding execution time is approximately reduced by 25% and 12%.

VIII. CONCLUSION

An active modulation strategy has been proposed in this paper for a 3L-NPC converter in aircraft ESG system. With the presented GBOI process, not only low-frequency NP voltage oscillation can be eliminated, but also two capacitor voltages can be kept balanced even though initial NP voltage imbalance emerges during high modulation index and low power factor operating conditions. The main contributions of this work are as follows: 1) Heavy computational burden can be overcome, which is beneficial to achieve better algorithmic-efficiency for high-speed drives. 2) Active capacitor voltage balancing control can be generalized for NTV^2 and CBPWM schemes based on the transformed reference frame. 3) Due to the establishment of coordinate of reference space vector in modulated signals, the technique introduces a degree of freedom to avoid the calculation of an appropriate ZSV. This method can also apply to all 3L-NPC converter-fed drives, and provides a new starting point for future research of silicon carbide (SiC)-based ESG system with advanced CBPWM schemes at 32 krpm for the purpose of higher power density, such as overmodulation can be gained by programming the position of reference space vector, etc. Simulation and experimental results confirmed the good overall modulation performance of the proposed strategy in terms of capacitor voltage oscillation, balancing, ease of use and scalability.

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