A Novel Repetitive Controller Assisted Phase-Locked Loop with Self-learning Disturbance Rejection Capability for Three-phase Grids

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***Abstract*—The synchronization between power grid and distributed power sources is a crucial issue in the concept of smart grids. For tracking the real-time frequency and phase of three-phase grids, phase-locked loop (PLL) technology is commonly used. Many existing PLLs with enhanced disturbance/harmonic rejection capabilities, either fail to maintain the fast response or are not adaptive to grid frequency variations or have high computational complexity. This paper therefore proposes a low computational burden Repetitive Controller (RC) assisted PLL (RCA-PLL) that is not only effective on harmonic rejection, but also has remarkable steady-state performance while maintaining fast dynamic. Moreover, the proposed PLL is adaptive to variable frequency conditions and can self-learn the harmonics to be cancelled. The disturbance/harmonic rejection capabilities together with dynamic and steady-state performances of the RCA-PLL have been highlighted in the paper. The proposed approach is also experimentally compared to the synchronous rotation frame PLL (SRF-PLL) and the Steady-State Linear Kalman filter PLL (SSLKF-PLL), considering the effect of harmonics from the grid-connected converters, unbalances, sensor scaling errors, d.c. offsets, grid frequency variations and phase jumps. The computational burden of the RCA-PLL is also minimized, achieving an experimental execution time of only 12 µs.**

Keywords— repetitive control, phase-locked loops, power system harmonics, fault tolerant control.

I. INTRODUCTION

Accurate real-time phase tracking of power grids is required for the synchronization of distributed power sources and their integration in the modern concept of smart grids. With more and more power electronics interfaced to the power networks, issues such as harmonics introduced by power converters, load unbalances, as well as measurement scaling error and d.c. offsets, produce periodic disturbances and degrade the accuracy of the phase tracking using a traditional phase-locked loop (PLL).

Vast varieties of three-phase PLLs have been proposed in literature. Although, there is no clear classification yet, authors in [1] have categorized three-phase PLLs according to their operating coordinates. We therefore have PLLs in natural *abc* coordinates (such as the zero crossing method[2]), in stationary αβ coordinates (such as the second order generalized integrator (SOGI) PLL[3]), and in rotating *dq* coordinates (as the synchronous rotation frame (SRF) PLL[4], the *dq* frame filter based PLL[5]). Authors in [6] have compared the SRF-PLL and some PLLs in the other two categories under conditions such as harmonics, voltage dips, and grid frequency variation; the SRF-PLL results as the simplest method that can sufficiently perform in all the test conditions. However, it needs to be dynamically slow to properly attenuate the harmonics and it provides poor performance on phase jumps [7].

In addition, as the SRF-PLL is based on a second-order model, it cannot track a frequency ramp without introducing a phase error. To solve such issues, a novel PLL structure, based on a third-order model Steady-State Linear Kalman Filter (SSLKF-PLL), has been originally proposed in [8] to mitigate the speed noise measurement in electrical drives. Such a technique has then been extended to the grid phase estimation for the first time in [9]. A third-order model has been successively employed in the type-3 SRF-PLL [10], which recently has been demonstrated to produce equivalent results to SSLKF-PLL [11].

A partial classification and a performance comparison of PLLs with enhanced filtering capabilities have been presented in [12]. Many papers have been published aiming at the enhancement of PLLs' disturbance rejection capability. For example, the notch filter (NF) based PLL[13] is fast, with strong filtering capability and adaptive to grid frequency variations. However, the disturbance due to d.c. sensor offsets have been not considered in [13]. Other advanced PLLs, such as the multiple-complex coefficient-filter (MCCF) PLL [14] and the multiple delayed signal cancellation (MDSC) PLL [15], are adaptive to grid frequency variations and can reject quickly all the aforementioned disturbances. However, their computational burden increases as the number of harmonics to cancel increases. Therefore, pre-knowledge of the harmonic pattern is required to reduce the unnecessary computational burden.

It seems that the requirements of effective disturbance rejection, fast dynamics, adaptive to grid frequency variations and a low computational burden are difficult to achieve all at the same time. A good balance between all these requirements has been achieved by using the SSLKF-PLL [9, 16, 17], which has been compared with the Discrete Fourier Transform (DFT) based PLL[18] in [19], showing superior performances in all the tested conditions.

The aim of this paper is to design a PLL that fulfils all the above-mentioned requirements at the same time. As a result, a novel Repetitive Controller Assisted SRF-PLL (RCA-PLL) is

proposed in this paper. Particularly, it can self-learn the grid harmonic pattern online while its computational burden does not increase if more target harmonics occur. Therefore, a benefit of the RCA-PLL is represented by the minimized computational effort, leading to an execution time of around 12μs, which is the same as the SSLKF-PLL.

Although RC has been used for PLLs in [20], its usage is more similar to a band-pass filter that mitigates the odd harmonics; furthermore, it is structurally very different from the traditional RC initially proposed by the authors in [21]. Moreover, to make the RC adaptive to grid frequency variation, the RC employed in the proposed solution is upgraded using a Lagrange fractional filter. Besides, fast dynamic of the SRF-PLL is maintained since the RC only works on harmonic rejections, while the SRF-PLL is responsible for the dynamic response.

This paper is organized as follows: the influences of harmonics, unbalances/sensor scaling errors and d.c. offsets in the grid voltages on its *dq* axis components will be analyzed in Section II. The RCA-PLL will be described in Section III. The SSLKF-PLL will be reviewed in Section IV. An experimental comparison among the RCA-PLL, the basic SRF-PLL and the SSLKF-PLL will be illustrated in Section V. The conclusions will be given in Section VI.

II. Making Full Use of the Park Transformation

One way to obtain better performances of a PLL is to filter the distortions in the three-phase voltages measurements. However, the analysis on the Park transformation results in the following subsections, performed under a variety of grid anomalies as well as considering the errors introduced by the measurements conditioning interfaces, shows that such issues can be solved without filtering the three-phase voltages.

The Clarke Transformation and the Park Transformation matrices are defined as in (1).

$$M_{abc2\alpha\beta}=\frac{2}{3}\begin{bmatrix}1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix},\ M_{\alpha\beta2dq}=\begin{bmatrix}\cos(\theta) & \sin(\theta)\\ -\sin(\theta) & \cos(\theta)\end{bmatrix} \quad (1)$$

A. Harmonics distortion

If a balanced three-phase system U_{abc} is polluted with the n^{th} harmonic, it is widely known that the $(n\text{-}1)^{th}$ and $(n\text{+}1)^{th}$ harmonics will be generated in U_{dq} after the Clarke and Park Transformations.

B. Negative sequence due to unbalances or sensor scaling error

A balanced grid only has positive sequence voltages. If any unbalances occur, negative sequence voltages will arise. Assuming the amplitudes of the positive, negative and zero sequences are U_1, U_2 and U_0, respectively, the resultant *dq* axis components generated by the negative sequence voltages are as in (2). As shown, a second harmonic in U_q is generated by the negative sequence voltages. Whereas, for the positive and zero sequences, there are no effects on U_q as in (3) and (4).

$$\begin{bmatrix}U_{d-}\\ U_{q-}\end{bmatrix}=M_{\alpha\beta2dq}M_{abc2\alpha\beta}\begin{bmatrix}U_2\cos(\theta)\\ U_2\cos(\theta+\frac{2\pi}{3})\\ U_2\cos(\theta-\frac{2\pi}{3})\end{bmatrix}=\begin{bmatrix}U_2\cos(2\theta)\\ -U_2\sin(2\theta)\end{bmatrix} \quad (2)$$

$$\begin{bmatrix}U_{d+}\\ U_{q+}\end{bmatrix}=M_{\alpha\beta2dq}M_{abc2\alpha\beta}\begin{bmatrix}U_1\cos(\theta)\\ U_1\cos(\theta-\frac{2\pi}{3})\\ U_1\cos(\theta+\frac{2\pi}{3})\end{bmatrix}=\begin{bmatrix}U_1\\ 0\end{bmatrix} \quad (3)$$

$$\begin{bmatrix}U_{d0}\\ U_{q0}\end{bmatrix}=M_{\alpha\beta2dq}M_{abc2\alpha\beta}\begin{bmatrix}U_0\\ U_0\\ U_0\end{bmatrix}=\begin{bmatrix}0\\ 0\end{bmatrix} \quad (4)$$

C. Offset error

d.c. offsets in three-phase voltages may occur due to reasons such as sensors offset errors or mismatch in the signal conditioning circuits. Assuming the offsets are *x, y* and *z* for the three phases, the resultant *dq* axis voltages are as in (5). As shown, d.c. offsets produce first order harmonics in the *dq* axis voltages.

$$\begin{bmatrix}U_d\\ U_q\end{bmatrix}=M_{\alpha\beta2dq}M_{abc2\alpha\beta}\begin{bmatrix}U_1\cos(\theta)+x\\ U_1\cos(\theta-\frac{2\pi}{3})+y\\ U_1\cos(\theta+\frac{2\pi}{3})+z\end{bmatrix}$$

$$=\begin{bmatrix}U_1(1+\frac{\sqrt{3}}{3}(y\text{-}z)\sin(\theta)+\frac{2x\text{-}y\text{-}z}{3}\cos(\theta))\\ U_1(-\frac{2x\text{-}y\text{-}z}{3}\sin(\theta)+\frac{\sqrt{3}}{3}(y\text{-}z)\cos(\theta))\end{bmatrix} \quad (5)$$

Summarizing the analysis results, it can be noticed that, the d.c. value of the *q* axis voltage is always zero once the θ used in the Park Transformation matches the real phase θ of the three-phase voltages. Therefore, to make the PLL work with the distorted three-phase voltages, the key is to control the d.c. value of U_q to zero.

The results also indicate that, when the grid voltage is distorted, ripple may appear in the frequency and phase identified by the SRF-PLL in Fig. 1, the mean value of the frequency still remains accurate since the Proportional-Integrator (PI) controller will bring the d.c. value of U_q to zero. Hence, to make full use of this characteristic, the average value of the frequency has been used in the intended harmonic compensation scheme. The symbols in Fig. 1 will be defined later in Section III.

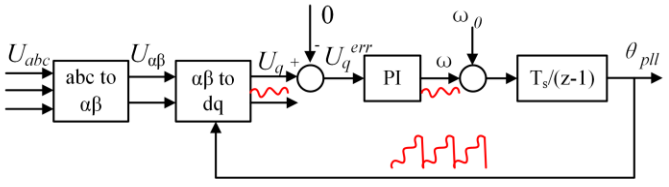
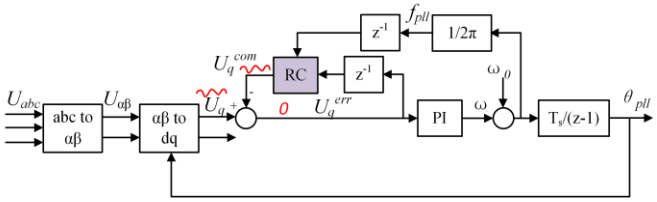


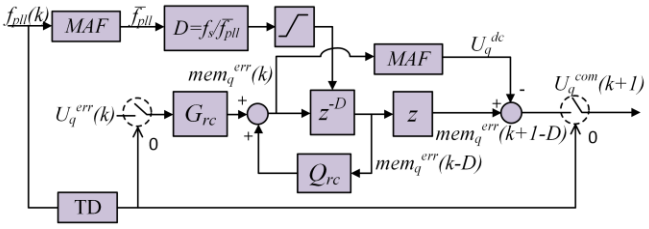
Fig. 1 Block diagram of the SRF-PLL

III. The Proposed RCA-PLL

A novel Repetitive Controller Assisted PLL (RCA-PLL), whose block diagram is shown in Fig. 2, is proposed.



(a) RCA-PLL block diagram



(b) the variable frequency RC

Fig. 4 Block diagram of the RCA-PLL

In Fig. 2(a), RC denotes the repetitive controller, $\omega_0=100\pi$ is the initial value for the output angular speed ω of the PI. The input of the PLL are the three-phase voltages U_{abc}, the outputs are the tracked frequency f_{pll} and the tracked phase θ_{pll}. In Fig. 3(b), MAF denotes the moving average filter, D is the fractional number of delay calculated from the ratio between the sampling frequency f_s (which equals 20 kHz in this paper) and the average tracked frequency $\bar{f}_{pll}$. The fractional delay z^{-D} is implemented using a 6th order Lagrange fractional delay filter. Q_{rc} is namely the forgetting factor of the RC, G_{rc} is the gain of the RC. TD denotes the transient detector: once a transient is detected, the input and output of the RC will be set to zero for 0.01s (i.e. half a cycle for a 50 Hz system).

The working principles of the RCA-PLL operating at fixed grid frequency have been introduced in [22], whilst in this paper a modified structure of the RCA-PLL is investigated for the first time in order to adapt the operation to grid frequency variations.

A flowchart of the RCA-PLL for the $(k+1)^{th}$ interval is illustrated in Fig. 3. Considering one sampling period of computational delay, only the tracked frequency f_{pll} and U_q^{err} of the previous sampling period are available in the $(k+1)^{th}$ interval. Any sudden step changes of more than 8 Hz in f_{pll}, are detected to properly disable the RC, otherwise a wrong computation action may be generated due to the transients in the frequency tracking. More explanations on how the RC improves the tracking performance when harmonics in U_q present will be explained later in the *Zero Error Tracking Proof* section in III-D.

A. Transfer functions

The transfer fucntion of the MAFs are as in (6), where, window sizes of the two MAFs are both chosen to be 400 because when the fundamental frequency is 50 Hz, there are 400 samples each cycle if fix the sampling frequency to 20 kHz. According to the ENTSO-e standard[23], the fundamental frequency should be regulated in the range 49.5 ~ 50.5 Hz. The fractional number of delay D is limited accordingly from 396

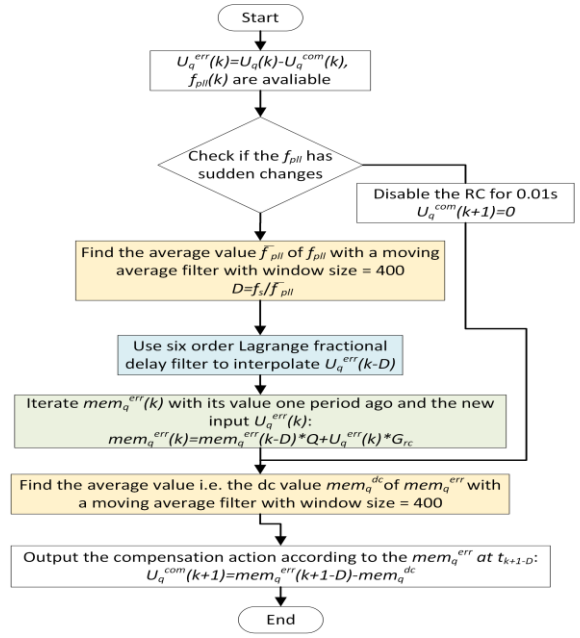


Fig. 3 Flowchart of the RCA-PLL

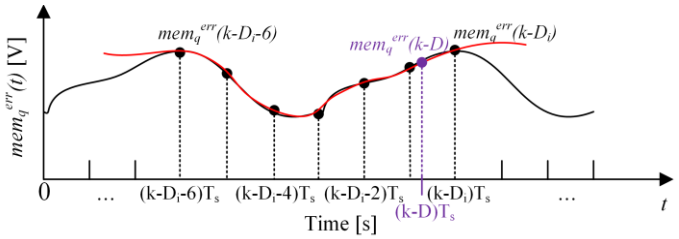


Fig. 2 6th order Lagrange interpolation.

to 404.1 (i.e. 20kHz/50.5Hz to 20kHz/49.5Hz). The transfer function of the RC is therefore as in (7).

$$MAF(z)=\frac{1}{400}(1+z^{-1}+\ldots+z^{-399}) \tag{6}$$

$$RC(z)=\frac{U_q^{com}}{U_q^{err}}=\frac{G_{rc}}{1-Q_{rc}z^{-D}}[z^{-D+1}-MAF(z)] \tag{7}$$

As shown in Fig. 3, the fractional number D is updated in every sampling interval according to the newest tracked grid frequency. The fractional delay z^{-D} is implemented using a Lagrange fractional delay filter. Denoting with D_i and D_f respectively the integer portion and the fractional part of the number D, i.e. $D=D_i+D_f$, $0<D_f<1$, the $mem_q^{err}(k-D)$ in Fig. 2(b) and Fig. 3 can be calculated as in (8) and (9), where, the order n is chosen to be 6. As shown in Fig. 4, the value of mem_q^{err} at t_{k-D} is interpolated using other seven memorized data at t_{k-Di-6}, t_{k-Di-5}, t_{k-Di-4}, t_{k-Di-3}, t_{k-Di-2}, t_{k-Di-1}, t_{k-Di}, respectively.

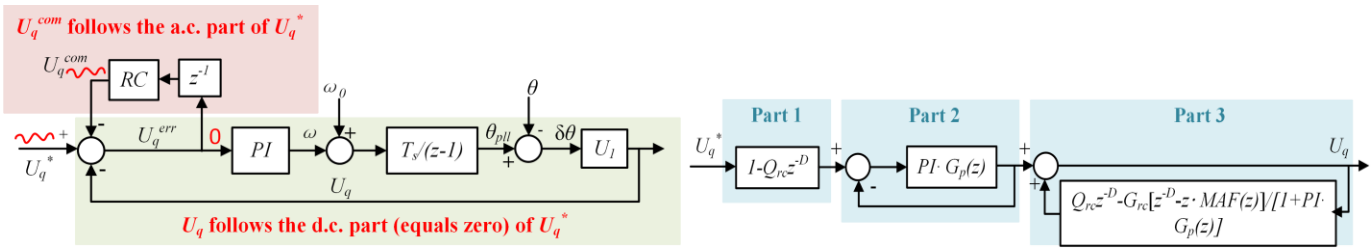
$$mem_q^{err}(k-D)=\sum_{j=0}^{n}P_j\cdot mem_q^{err}(k-D_i-j) \tag{8}$$

$$P_j=\prod_{\substack{h=0\\h\neq j}}^{n}\frac{D_f-h}{j-h},\ \text{for } j=0,1,\ldots,n \tag{9}$$

The transfer function of the PI controller is expressed as (10):

$$PI(z)=k_p+k_i\cdot\frac{T_s}{z-1} \tag{10}$$

where k_p is the proportional gain and k_i is the integral gain. T_s is the sampling period, and $T_s=1/f_s$.



(a) Small-signal model of the RCA-PLL. (b) Equivalent diagram of (a)

Fig. 5 Equivalent diagrams of the RCA-PLL.

As given in (7) and (10), there are four parameters to tune in the RCA-PLL, i.e. the gain G_{rc} and the forgetting factor Q_{rc} for the RC, and the gains k_p, k_i for the PI controller. These four parameters can be chosen according to stability criteria. Before analyzing the stability of the system, it is worth deriving the equivalent diagram for the RCA-PLL.

B. Equivalent Diagram and Working Principle of the RCA-PLL

Given the balanced and purely sinusoidal three-phase voltages U_{abc} as defined in (11), where, U_1 denotes the peak value of the positive sequence. Phase θ denotes the actual phase of the three-phase system. If the tracked phase θ_{pll} is used for the Park Transformation and it has a small error δθ, i.e. $\theta_{pll}=\theta+\delta\theta$, the relationship between U_{dq} and δθ is derived in (12).

$$\begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = \begin{bmatrix} U_1\cos(\theta) \\ U_1\cos(\theta-\frac{2\pi}{3}) \\ U_1\cos(\theta+\frac{2\pi}{3}) \end{bmatrix} \tag{11}$$

$$\begin{bmatrix} U_d \\ U_q \end{bmatrix} = \begin{bmatrix} \cos(\delta\theta) & \sin(\delta\theta) \\ -\sin(\delta\theta) & \cos(\delta\theta) \end{bmatrix} \begin{bmatrix} U_1 \\ 0 \end{bmatrix} \tag{12}$$

Since $\delta\theta$ is assumed to be small, $\sin(\delta\theta)\approx\delta\theta$. Therefore, q-axis voltage $U_q=-U_1\cdot\sin(\delta\theta)\approx-U_1\cdot\delta\theta$. Based on this conclusion, the equivalent small-signal model of the RCA-PLL can be drawn as in Fig. 5(a), where, the U_q^* denotes the q-axis voltage when $\delta\theta=0$. Therefore, if the system is balanced and do not contain ripple, $U_q^*=0$. Following the discussions in Section II, if the three-phase system is not balanced or contains ripple, U_q^* will contain ripple.

As illustrated in Fig. 5(a), the RC is used to track the a.c. part (i.e. ripple part) of U_q^*, whereas, the PI controller is used to track the d.c. part (which is always zero) of U_q^*. Ideally, at steady-state, U_q^{com} cancels the entire ripple in U_q^*, and the d.c. value of U_q^{err} is regulated to zero by the PI controller, such that the phase tracking error $\delta\theta=0$.

C. Tuning of the RCA-PLL

Fig. 5(b) shows the equivalent diagram of the system in Fig. 5(a). The system stability is ensured if each of the three parts in Fig. 5(b) is designed to be stable [24].

In fact, Part 2 in Fig. 5(b) is the closed loop system without RC. Therefore, the first step of the RCA-PLL tuning procedure is to tune the PI controller without considering the RC.

The relationship between proportional and integral gains (K_p, K_i) of the PI controller and natural frequency, damping factor (ω_n, ζ) is given by (13), as derived in [22].

$$k_p=\frac{2\zeta\omega_n}{U_1},\ k_i=\frac{\omega_n^2}{U_1} \tag{13}$$

Part 1 in Fig. 5(b) is exactly the denominator of the RC equation in (7). By substituting z with $e^{j\omega T_S}$, the term $(1-Q_{rc}z^{-D})$ can be expressed as $1-Q_{rc}e^{-jD\omega T_S}$. Its minimum value $(1-Q_{rc})$ is achieved when $D\omega T_s=2\pi i$, $i=0, 1, 2\ldots$, i.e. $\omega=2\pi i f_d$. By setting Q_{rc} to one, the system response will be zero for inputs at the fundamental frequency f_d and its multiple frequencies.

Sill with reference to Fig. 5(b), from the discussion above regarding Part 2 and Part 1, we can determine that input and output of Part 3 is bounded. For bounded systems, the small gain theorem can be applied to guarantee system stability. Part 3 will be stable if (14) is verified. Hence, the choices of G_{rc} and Q_{rc} should satisfy (14).

$$\begin{aligned} |S(e^{j\omega T_S})| &= \left|Q_{rc}-\frac{G_{rc}[e^{j\omega T_S}-MAF(e^{j\omega T_S})e^{jD\omega T_S}]}{1+PI(e^{j\omega T_S})\cdot G_p(e^{j\omega T_S})}\right|\cdot|e^{-jD\omega T_S}|<1 \\ \xrightarrow{yields} &\left|Q_{rc}-\frac{G_{rc}[1-MAF(e^{j\omega T_S})e^{j(D-1)\omega T_S}]}{1+PI(e^{j\omega T_S})\cdot G_p(e^{j\omega T_S})}\right|<1 \end{aligned} \tag{14}$$

In this paper, G_{rc} and Q_{rc} are chosen to be 1 and 0.8 respectively, the natural frequency ω_n and damping ζ are chosen to be 62.83 rad/s (i.e.10 Hz) and 0.791 respectively. The peak value of the positive sequence in the three-phase system U_1 is 311.1 V (i.e. 220 V RMS). Calculating from (13), k_p=0.32 and k_i=12.7.

D. Zero Error Tracking Proof

According to Fig. 5(a) and equation (7), the error $U_q^{err}(z)$ can be expressed as in (15).

$$U_q^{err}(z)=\frac{U_q^*(z)}{1+RC(z)z^{-1}+\frac{PI(z)U_1T_S}{z-1}}=\frac{U_q^*(z)(1-Q_{rc}z^{-D})}{\left(1+\frac{PI(z)U_1T_S}{z-1}\right)\left[1-Q_{rc}z^{-D}+\frac{G_{rc}(z^{-D}-MAF(z)z^{-1})}{1+\frac{PI(z)U_1T_S}{z-1}}\right]} \tag{15}$$

Substituting z with e^{jwT_S}, (15) yields (16).

$$U_q^{err}(e^{j\omega T_S})=\frac{U_q^*(e^{j\omega T_S})(1-Q_{rc}e^{-j\omega DT_S})}{\left(1+\frac{PI(e^{j\omega T_S})U_1T_S}{e^{j\omega T_S}-1}\right)\left[1-Q_{rc}e^{-j\omega DT_S}+\frac{G_{rc}(e^{-j\omega DT_S}-MAF(e^{j\omega T_S})e^{-j\omega T_S})}{1+\frac{PI(e^{j\omega T_S})U_1T_S}{e^{j\omega T_S}-1}}\right]} \tag{16}$$

As Q_{rc}=1, $D=f_s/\bar{f}_{pll}=1/(T_s\bar{f}_{pll})$ and, at steady-state, the tracked frequency $\bar{f}_{pll}$ equals the fundamental frequency f_d of the three-phase voltage, it can be seen that (16) equals zero when the frequency $\frac{\omega}{2\pi}$ is an integer multiple of f_d and it is below the Nyquist frequency. Equation (17) implies that at steady-state, zero error tracking of U_q^* can still be achieved when harmonics are present in U_q^*.

$$\lim_{\omega\to\omega_i} U_q^{err}(e^{j\omega T_S})=0,\ \omega_i=2i\pi f_d \quad \forall\, i=0,1,2,\cdots,i_{max}\ \{i_{max}f_d\le\tfrac{f_s}{2}\} \tag{17}$$

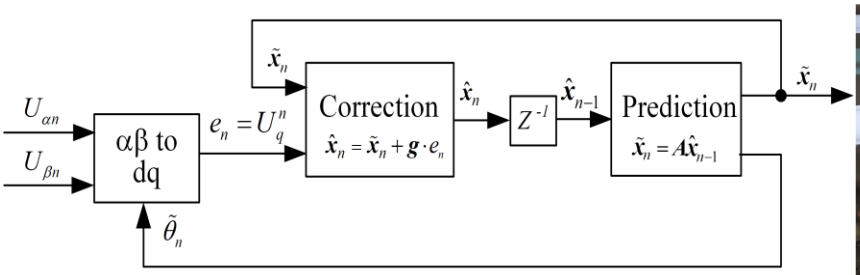


Fig. 6. Block diagram of a SSLKF-PLL.

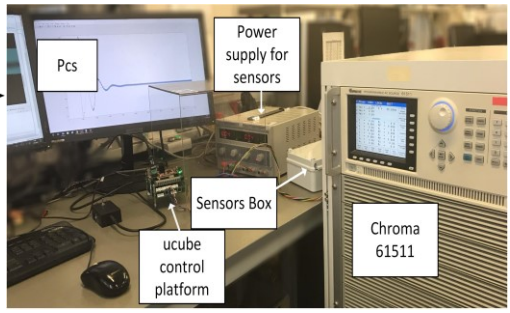


Fig. 7 Experimental rig

IV. Review of SSLKF-PLL

Fig. 6 shows the block diagram of the SSLKF-PLL system composed of a phase detector and a loop filter based on the prediction-correction filter described below. Like in a SRF-PLL, the signal error e_n is calculated by the q component of the Park Transformation applied to the measured grid voltage components $U_{\alpha n}$ and $U_{\beta n}$ and the estimated angle $\tilde{\theta}_n$ and can be approximated as follow:

$$e_n = \frac{U_{\beta n}\cos\tilde{\theta}_n - U_{\alpha n}\sin\tilde{\theta}_n}{U_S} = \sin\theta_n\cos\tilde{\theta}_n - \cos\theta_n\sin\tilde{\theta}_n = \sin(\theta_n - \tilde{\theta}_n) \approx \theta_n - \tilde{\theta}_n \quad (18)$$

where n is the sampling instant index, U_S and θ_n are the module and the phase of the grid voltage phasor, $\tilde{\theta}_n$ is the phase angle estimated by the SSLKF-PLL.

The PI regulator, used as a loop filter in a SRF-PLL, is replaced by a deterministic prediction-correction filter, composed of a prediction model followed by a correction model. The third-order physical prediction model, based on the electrical grid equations, can be written in the following discrete-time state form:

$$\begin{cases} \boldsymbol{x}_n = \boldsymbol{A}\boldsymbol{x}_{n-1} \\ y_n = \boldsymbol{c}^T\boldsymbol{x}_n \end{cases} \quad \text{where, } \boldsymbol{x}_n = \begin{bmatrix} \theta_n \\ \omega_n \\ a_n \end{bmatrix} \boldsymbol{A} = \begin{bmatrix} 1 & T_s & T_s^2/2 \\ 0 & 1 & T_s \\ 0 & 0 & 1 \end{bmatrix}$$
$$\boldsymbol{c}^T = [1 \quad 0 \quad 0] \quad (19)$$

being T_s the sampling interval, θ_n the grid voltage angle, ω_n the grid angular frequency, a_n the derivative of the grid angular frequency, y_n the computed value of the phase angle. On the basis of dynamic model (19), the prediction-correction filter performs the following two steps:

1) prediction of the state at the subsequent sampling instant:

$$\tilde{\boldsymbol{x}}_n = \boldsymbol{A}\hat{\boldsymbol{x}}_{n-1} \quad (20)$$

2) correction of predicted state on the basis of the prediction phase error $e_n = \theta_n - \boldsymbol{c}^T\tilde{\boldsymbol{x}}_n$:

$$\hat{\boldsymbol{x}}_n = \tilde{\boldsymbol{x}}_n + \boldsymbol{g}e_n \quad (21)$$

Coefficients g_1, g_2 and g_3 of the correction vector $\boldsymbol{g}^T = [g_1\ g_2\ g_3]$ can be selected following the design procedure described in [17].

V. Experimental Tests Results

An experimental test rig has been built to compare the SRF-PLL, the SSLKF-PLL, and the proposed RCA-PLL. As shown in Fig. 7, a programmable AC source (Chroma) is used to generate the distorted three-phase voltages. It is worth mentioning that, although the three-phase voltages generated by the Chroma are balanced and have no d.c. offsets, due to the inaccuracy of the measurement chain components (sensors, signals conditioning circuits and ADCs), all the tests are affected by a 1.73% unbalance in the three-phase voltage measurements, as well as by a 2.5% d.c. offset in phase A, -0.4% d.c. offset in phase B and 0.2% d.c. offset in phase C. The high performance control platform, ucube [25], is used to implement the PLL solutions, while the experimental results are plotted using Matlab.

A 50Hz, 220V (RMS) three-phase system has been tested under the following five conditions in sequence.

1) Test 1 High-order harmonics test: To emulate the distortions induced by grid-connected convertes, several odd harmonics (i.e. 1.1% 3rd harmonic, 2.8% 5th harmonics, 1.4% 7th harmonic, 2.3% 9th harmonic, 1.5% 11th harmonic, satisfying the IEEE 519 standard [26] for 1kV to 69kV systems) are added to the three-phase voltages, thus resulting in a Total Harmonic Distortion (THD) equal to 4.3%. The resultant U_{dq} have 2nd, 4th, 6th, 8th and 12th harmonics.

2) Test 2 Second-order harmonic test: On top of the harmonics in the *Test 1*, the amplitude of phase *A* in Chroma is set to 10% smaller than the other phases. This means that second harmonics are added to U_d and U_q, respectively.

3) Test 3 First-order harmonic test: To make the harmonics even more difficult to filter, additional 30 V d.c. offset is added to the phase *A*, while the other settings in *Test 2* remain unchanged. This means that first-order harmonics are added to U_d and U_q, respectively.

4) Test 4 Grid frequency variation test: Under the same conditions as in *Test 3*, a ±0.5 Hz variation in the fundamental frequency is applied to the three phase voltages.

5) Test 5 Phase jump test: Under the same conditions as in *Test 3*, and fundamental frequency equals to 50Hz, a phase jump of -50° is applied in the three-phase voltages.

The waveforms of the three-phase voltages under the aforementioned five conditions are summarized in Fig. 8.

During the tests, the natural frequencies of the closed-loop systems for the three PLLs are kept the same at 10 Hz. Since the disturbance/harmonic rejection ability of the SSLKF-PLL can be enhanced by reducing the system dynamics, the results for when the natural frequency equals to 5 Hz also have been presented. In the following, they will be denoted as "SRF-PLL

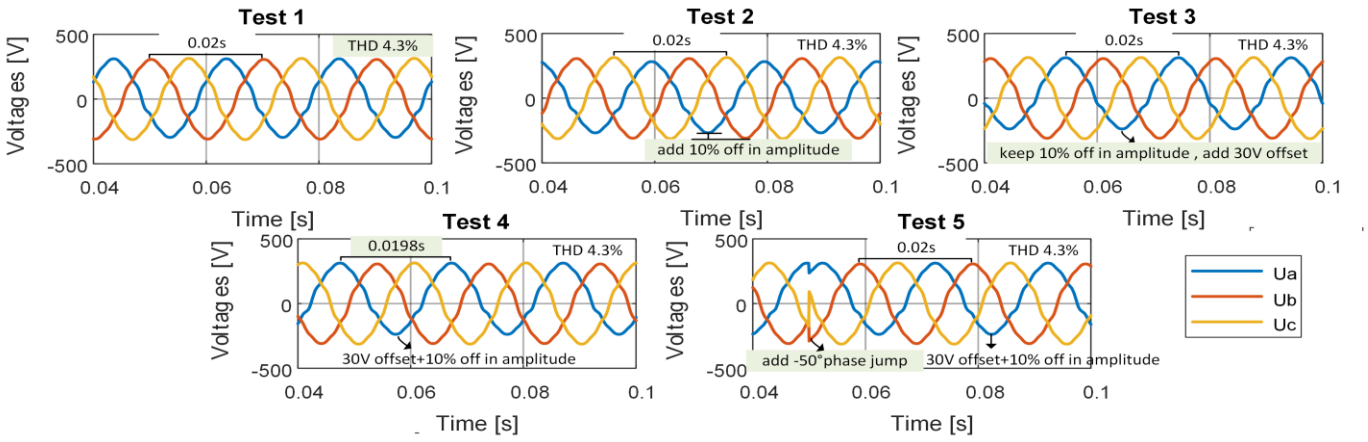


Fig. 8 Three-phase voltages under the five experimental conditions (All conditions contain additional d.c. offsets of 2.5% in phase *A*, -0.4% in phase *B*, 0.2% in phase *C* and 1.73% unbalance due to sensors and ADC limitations.)

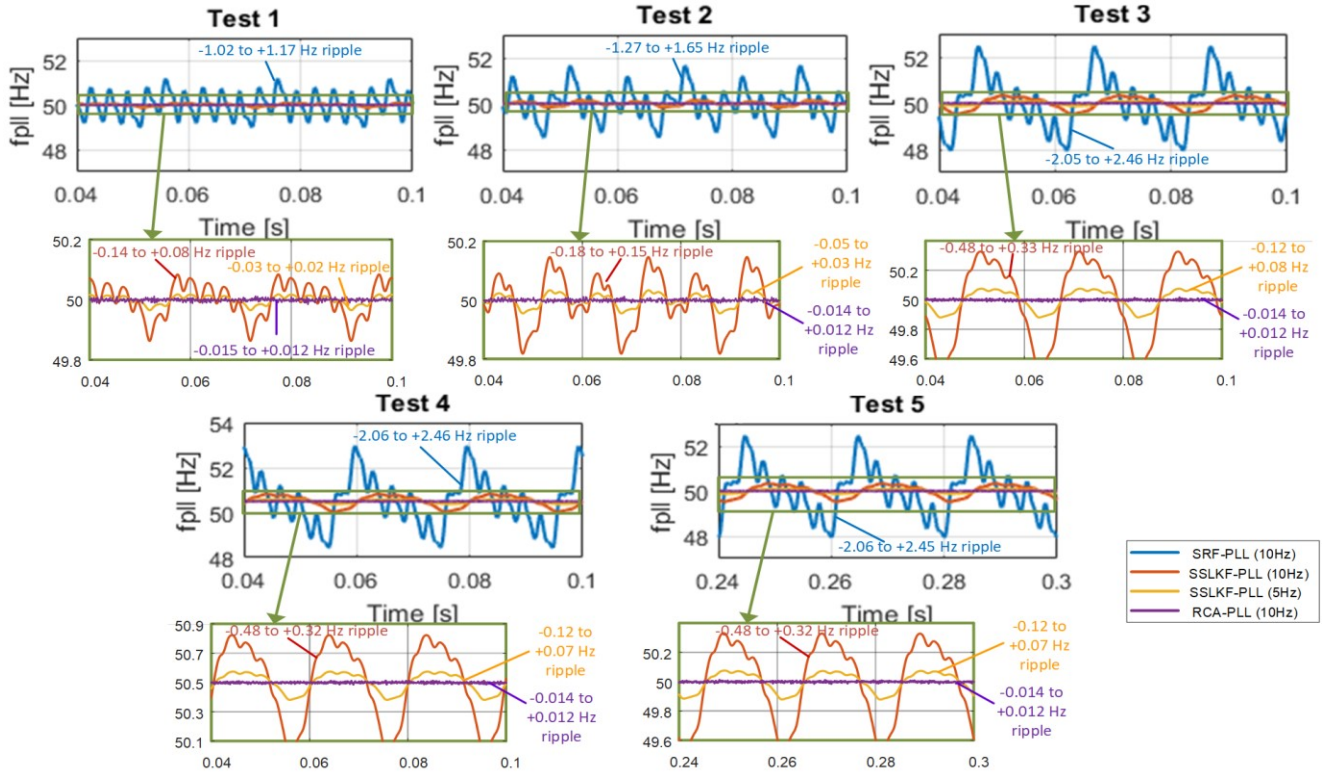


Fig. 9 Tracked frequency at steady-state under the five experimental conditions.

(10 Hz)", "SSLKF-PLL (10 Hz)", "SSLKF-PLL (5 Hz)" and "RCA-PLL (10 Hz)".

Moreover, the real phase of the phase *A* voltage at steady-state is computed offline by using Fast Fourier Transformation (FFT). The phases identified by the three PLLs are compared with this real phase to verify their effectiveness.

Overall, the frequency and phase tracking performances of the three PLLs are discussed in the following three subsections, while the benefits and the drawbacks of the tested PLLs are summarized in the fourth subsection.

A. Steay-state Performance

The tracked frequency and phase error waveforms under all the five test conditions at steady-state are shown in Fig. 9 and Fig. 10, respectively. Those results are also shown in the frequency-domain in Fig. 11 by applying FFT.

As shown in Fig. 9, the RCA-PLL has the best frequency tracking. Although the frequency tracking errors of the SSLKF-PLL (10 Hz) are already more than 80% reduced compared with the SRF-PLL, and the SSLKF-PLL (5 Hz) is even better (more than 95% error reduction), only the RCA-PLL can remove almost completely the estimation ripple and achieve remarkable frequency tracking of the fundamental frequency.

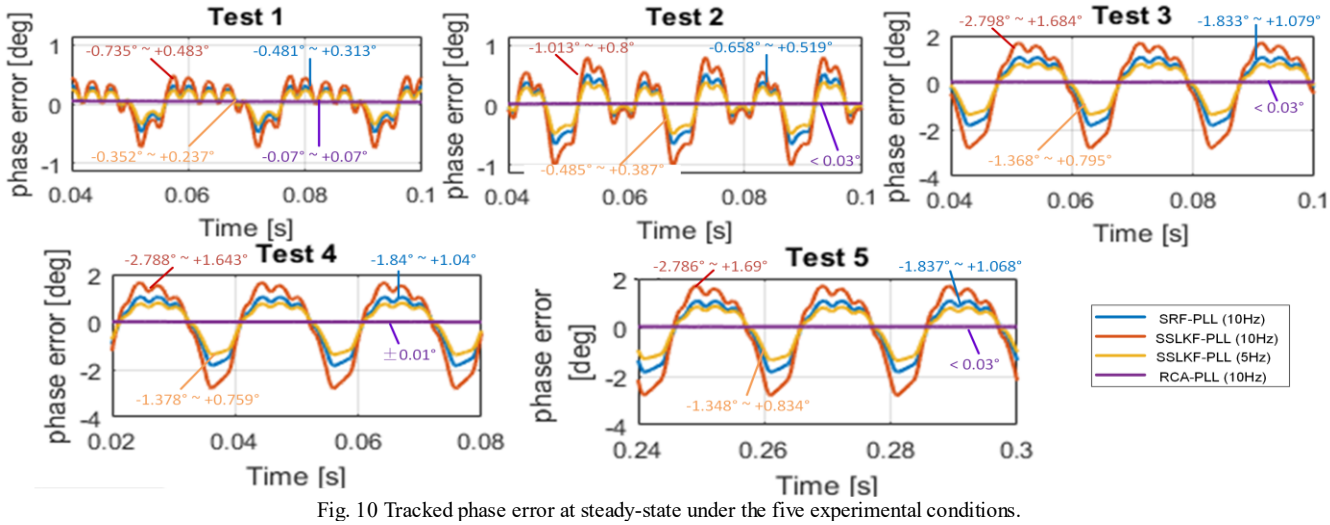


Fig. 10 Tracked phase error at steady-state under the five experimental conditions.

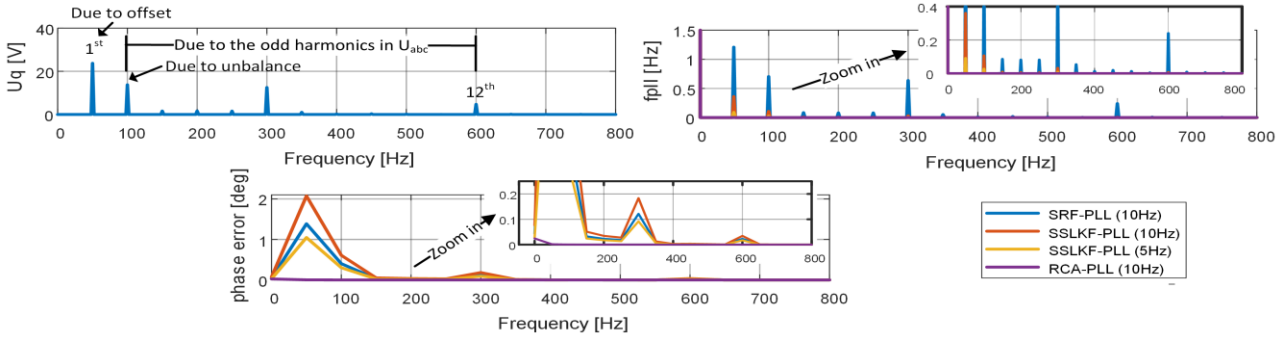


Fig. 11 FFT of the tracked frequency and phase error at steady-state in Test 3.

For comparing the phase tracking, it is more convenient to perform a comparison in the frequency-domain; to this aim, from the plots shown in Fig. 11, it can be noticed that only the RCA-PLL can remove all the undesired harmonics from the 1st order to the 12th order.

It is also worth pointing out that although the SSLKF-PLL tracks the frequency much better than the SRF-PLL, the phase tracking errors of the latter is conversely lower when their natural frequencies are both equal 10 Hz.

Besides, it is worth emphasising that the PI tuning in the RCA-PLL (10 Hz) is the same as in the SRF-PLL (10 Hz). Hence, the results prove that by adding RC, the disturbance rejection ability is effectively enhanced without changing the PI.

Overall, the RCA-PLL has the best frequency and phase tracking performances at steady-state. Its disturbance/harmonic rejection ability is the strongest among the three tested PLLs at steady-state. A clear benefit of the RCA-PLL is that its ripple reduction ability does not vary for different frequencies, whereas the SSLKF-PLL attenuates the higher order harmonics more effectively than the lower order harmonics.

B. Dymanic Performance

The initial transients of the tracked frequency and phase error waveforms in *Test 3*, the transients during the grid frequency variation in *Test 4*, and the transients due to the phase jump in *Test 5* are shown in Fig. 12 and Fig. 13, respectively.

A clear drawback of using the SSLKF-PLL (5 Hz) is that it is dynamically slow. Therefore, when tuning the SSLKF-PLL, the trade-off between the harmonic rejection ability and its dynamics need to be considered. Conversely, the RCA-PLL can reduce the harmonics without sacrificing its dynamic performance. As shown in Fig. 12 and Fig. 13, the RCA-PLL behaves the same as the SRF-PLL at the beginning, when the PLLs are initialized in the *Test 3* and when the phase jump occurs in the *Test 5*. This is because the RC is disabled during such transients. When these transients are about to terminate, the RC in the RCA-PLL takes effects and improves the steady-state performances.

Another type of transient worth mentioning is the grid frequency variation. As shown in Fig. 12 and Fig. 13 for the *Test 4*, thanks to the Lagrange fractional delay filter used, the RC is adaptive to such variation and it is effective to reject harmonics even during this transient. Fig. 13 illustrates the differential phase obtained subtracting the phase identified by the RCA-PLL from the phases identified by the SRF-PLL/SSLKF-PLL. The resultant three waveforms in Fig. 13 are like the *Test 4* results in Fig. 10. This indirectly confirms that the RCA-PLL identifies the phase more accurately. What is more, this paper focuses on the grids within the ENTSO-e standard, however, it is possible to apply the proposed RCA-PLL for larger frequency variation from 47.5 Hz to 51.5 Hz. The frequency and phase tracking performances are similar to the *Test 4* results in Fig. 12 and Fig. 13.

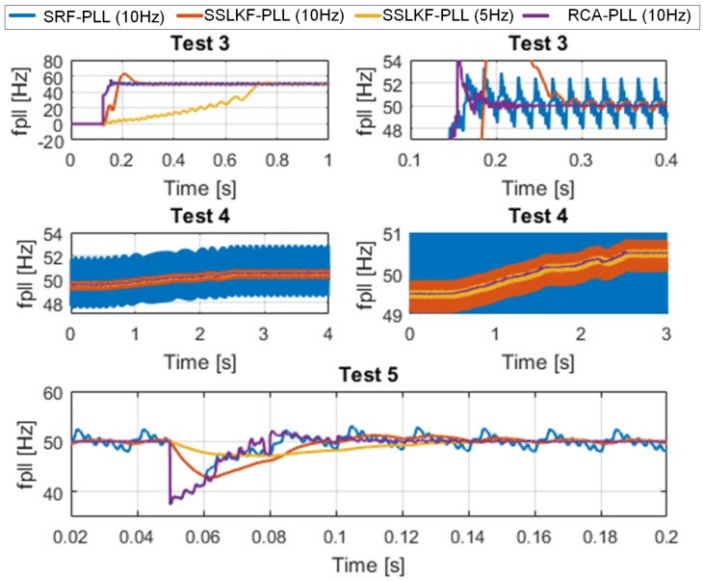


Fig. 12 Tracked frequency during transients in Tests 3,4,5.

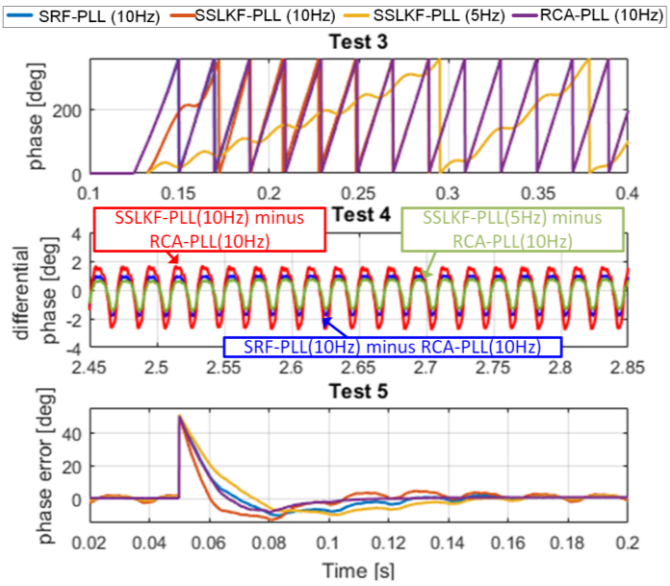


Fig. 13 Tracked phase during transients in Tests 3,4,5.

C. Computational Effort

The algorithm execution time for the three PLLs is measured within the ucube control platform, obtaining for the SRF-PLL 5 µs and for the RCA-PLL and the SSLKF-PLL around 12 µs. This confirms that the proposed method can be implemented in the most common control platforms. Some commonly used solutions have been adopted in the implementation of the RCA-PLL to reduce computational burden:

1) Reduced computation in the moving average filers: Since only one value of the 400 values in the MAF is replaced in each period, the sum can be easily updated by subtracting the value to be replaced and add the new value.

2) Use a Farrow structure for the fractional delay filter: A Farrow structure [27] is used for the fractional delay filter to make it more computationally effective. The order of the fractional delay filter is chosen to be six, considering the trade-off between the interpolating accuracy and the computational load.

3) Use of pointers for updating the arraies: In the RC, the tracked frquency f_{pll} and the error in the q axis voltage U_q^{err} are all recorded using arraies. There is no need to shift the entire array each time it updates, the arraies are updated simply by replacing the oldest values.

D. Benefits of the RCA-PLL

The RCA-PLL has fulfilled the design requirements mentioned in Section II, and its benefits can be summarized as below:

1) In order *to maximize the disturbance/harmonic rejection capability*, RC is chosen for its ability of rejecting all harmonics without pre-knowing which orders of harmonics are contained in grids. Only two parameters (i.e. G_{rc} and Q_{rc}) need to be tuned, and once they are tuned, the RC can learn the ripple component in the U_q^{err} and provide a compensation action U_q^{com} to cancel only the ripple in U_q.

2) For generating the correct compensation action, at least one cycle (i.e. 0.02s for the 50 Hz system) of learning period is required for the RC to take action. This long delay is a drawback of the RC in some applications but does not affect the performance of the proposed PLL since RC is not responsible for the system dynamics. Thus, *superior harmonic rejection is achieved at steady-state without interfering with the dynamic actions of the PI controller.*

3) The transient detector disables the RC during transients either due to the PLL start-up or due to a phase jump. For other cases, like *grid frequency variations*, there is no need to disable the RC since it is adaptive to variable frequency. The traditional RC assisted PLL in [22] can only work at fixed frequency, since its delay line must be a fixed integer. However, the RC used in this work can adapt the length D of its delay chain online by making use of the tracked frequency f_{pll} (the average value of f_{pll} is an accurate approximation of the real frequency), and D can be a fractional number due to the Lagrange fractional delay filter used.

4) In total, two MAFs and one 6th order Lagrange fractional delay filter are used in this implementation. However, the execution time of the RCA-PLL is only 12µs according to discussion in the previous subsection.

VI. Conclusion

A novel Repetitive Controller Assisted PLL adaptive to grid frequency variation has been proposed in this paper for the first time. The RCA-PLL has superior disturbance rejection capability. The orders and amplitudes of the target harmonics are not required for its design. The RCA-PLL can self-learn and cancel a wide range of harmonics from as low as the fundamental (i.e. 50 Hz) to the Nyquist frequency. In comparison to others widely used techniques, it can achieve superior frequency and phase tracking at steady-state, without compromising dynamic performances during phase jumps or other transients. Experimental test results have shown that accurate frequency and phase tracking is achieved for all tested conditions not only at steady-state, but also during grid frequency variations. As a further benefit, the computational

burden of the RCA-PLL is low. Its execution time is just 12 µs, which is feasible even using most common industrial grade microcontrollers.

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