Analysis and Experimental Evaluation of a Soft Switching Boost Converter with Unbalanced Capacitor Voltage

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***Abstract*— This paper presents a novel unbalanced capacitor voltage (UCV) soft switching boost converter under full loads range with a simple control scheme. The topology consists of a half bridge switching-leg, filter inductor, and an auxiliary circuit containing one switch and one resonant inductor. It uses the resonance between the parasitic output capacitors in parallel to each active switch and the resonant inductor to achieve zero-voltage-switching. The auxiliary circuit, acting as the resonant tank, is employed just before the main switch is turned on. It has been demonstrated that the controlled unbalancing of series connected output capacitor voltages causes the low side capacitor voltage to be less than half of the output voltage, which creates the necessary condition to achieve soft switching for the low duty ratio and low power loads. The concept is validated experimentally on a 1 kW/200 kHz prototype implemented with silicon carbide (SiC) MOSFET operated within a wide range of duty ratios and load powers. The rated efficiency of the proposed converter is 95.7% as soft switching reduces up to 60% of the total losses when compared with a hard switching converter.**

***Index Terms*— Boost converter, Resonant tank, Soft-switching, SiC MOSFET, Unbalanced capacitor voltage.**

I. Introduction

Step-up dc-dc converters are widely used in PV systems, power factor correction (PFC), and fuel cell hybrid vehicles (FCHV) [1]−[4]. The purpose of the step-up converter is to increase the output voltage and stabilize its level independent of the input variations. For example, in the FCHV system, it controls the power flow from the fuel cell stack (FCS) to DC-bus as shown in Fig. 1. Considering the need for low-cost, high-power density, and high efficiency, high switching frequency converters are promising solutions in such applications. High switching frequency benefits from minimizing the size and weight of passive components, like filter inductors and capacitors due to the reduced duration of energy storage. Nevertheless, high-switching-frequency hard switched converter brings several new challenges, such as high switching losses, high *dv*/*dt*, and switching spikes. These causes some limitations that are detrimental in some situations because of the increasing size and cost of the heatsink, amplified electromagnetic interference (EMI) problem and the potential circuit damage from voltage spikes.

Soft switching converters relying on zero-voltage switching or zero-current switching technologies have attracted much attention as these can eliminate switching losses, mitigate *dv*/*dt* and EMI of the generated waveform, increase the reliability of the system operation, and improve system efficiency [5]. Soft switching converters could be isolated or non-isolated. The isolated soft switching converters, such as dual active bridge (DAB) and LLC converters, use an AC power transformer to realize soft switching operation for the switches [6], [7].

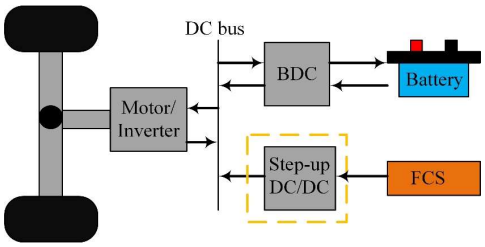

Fig. 1. Powertrain of FCHV.

Compared with the isolated topologies, the non-isolated soft switching converters feature higher power density, and they are frequently selected in high frequency applications. To realize soft switching, resonant tank is quite popular to be inserted in the converter to create inductive or capacitive load conditions. These circuits based on resonant tank could be categorized as the quasi-resonant converter (QRC), PWM-ZVS, PWM-ZCS and resonant transition converter (RTC) [8]−[15]. In the power loop, the QRC, PWM-ZVS/ZCS converters have one or multiple resonant tanks which enable soft switching under simple control system. But the devices undertake high voltage or current stress, and the hard switching happens at light loads [9]. Furthermore, the active resonant soft switching converter (such as ZCT, ZVT) combines with an additional auxiliary circuit, which conducts before or after the main switch is supposed to turn on or off. Otherwise, a large number of additional devices and additional magnetic components are used in the auxiliary loop increasing the volume and losses of the converter [10]−[12]. Complex control methods and high current stress are other challenges in high-frequency applications, which add the response time because of the complex closed-loop calculations. The four-switch buck-boost converter has a small number of semiconductors to operate in bidirectional mode [15]. The main inductor current will become negative and create zero voltage switching conditions when the switches turn on.

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However, this increases the RMS inductor current due to the high peak-to-peak ripple and the switch current stress. The complex control method also increases the calculation and response time of a microcontroller, which is a challenge to operate under a very high switching frequency. The unbalanced capacitor voltage bi-directional buck-boost converter employs back-to-back switches in the auxiliary loop [16], which uses simple control methods to achieve soft switching for all switches. But because of the opposite voltage polarity of the output unbalanced capacitors, the auxiliary switching devices experience higher voltage stress.

This paper proposes a new unbalanced capacitor voltage (UCV) boost converter, which incorporates a simple auxiliary network and two unbalanced capacitors on the output side. The small size auxiliary inductor resonates with the parasitic output capacitor of switches which forces the switching voltage to become zero before the main switch enters conduction. The unbalanced voltage capacitors assist in reducing the input resonant tank voltage and extend the ZVS turn-on range to full duty ratios and full power loads. The silicon carbide (SiC) MOSFET will be utilized in the experimental circuit because of its faster switching, smaller parasitic capacitors, and lower on-state conduction losses, which is useful in the proposed topology to reduce the turn-off switching losses and voltage spikes [18]. This paper is divided into six sections. In Section II, start-state and steady-state working processes for the converter are described. The soft switching conditions and the loss breakdowns of the proposed soft switching topology are discussed in Section III. Section IV presents a comparison of the proposed converter with previously published soft switching converters, including structures, soft switching range and efficiency, which prove the higher performance of the proposed converter. The experimental results of a laboratory prototype that validates the soft switching performance are shown in Section V. Section VI will draw a conclusion.

II. Operation of the Unbalanced Capacitor Voltage Soft Switching Boost Converter

Fig. 2 depicts the unbalanced capacitor voltage boost converter based on two sections: S_1, S_2 and L_m create the main loop of the boost converter. Synchronous rectification is adopted here to save the conduction loss. cs_1 and cs_2 are the device parasitic output capacitors for S_1 and S_2. L_m is the main loop filter inductor. The auxiliary tank combines a small-size auxiliary inductor L_a, and an auxiliary switch S_a. The output side is connected to two unbalanced voltage capacitors, C_1 and C_2, which work as filters to reduce the ripple of the output voltage and provide soft switching conditions.

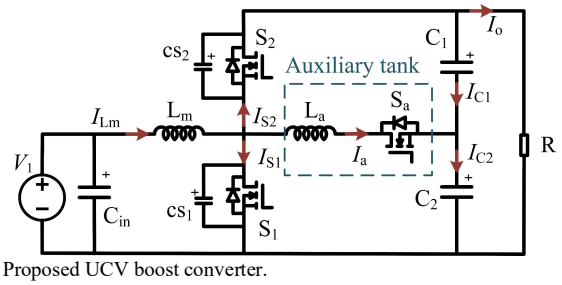
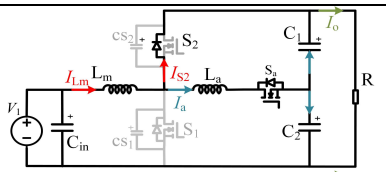
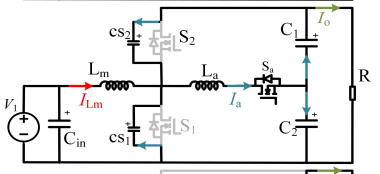
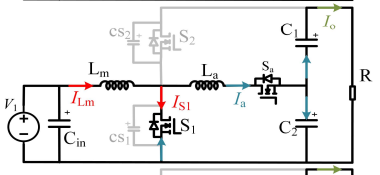
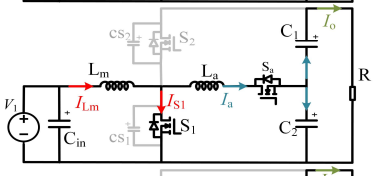
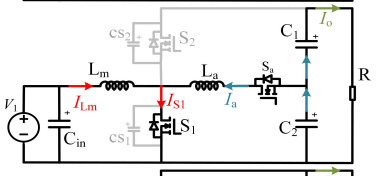
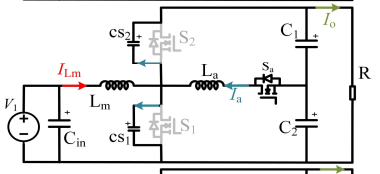
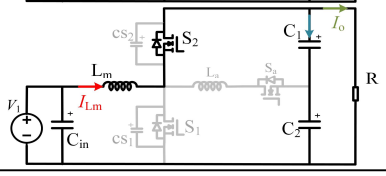


Fig. 2. Proposed UCV boost converter.

A. Steady State Operation

Considering the system reaches a steady state after the start-up process, the converter operation can be separated into seven modes, as shown in Table I. The first seven modes are described in detail below and graphical representations of each mode have been presented in Fig. 4. From t_0 to t_3, as the time is very short, and the main inductor current is considered to be fixed. The duty ratio of S_1 is D. Before the first interval, the body diode of synchronous rectifier switch S_2 conducts while the main switch S_1 and the auxiliary switch S_a are off.

TABLE I
Equivalent Sub-Circuits at Steady State

Sub-circuit	Transition time
	Mode 1 t_0~t_1
	Mode 2 t_1~t_2
	Mode 3 t_2~t_3
	Mode 4 t_3~t_4
	Mode 5 t_4~t_5
	Mode 6 t_5~t_6
	Mode 7 t_6~t_7

Mode 1 (t_0~t_1): This interval starts with turning on the auxiliary switch S_a under zero current conditions because of the discontinuous auxiliary current. The synchronous rectifier switch current I_{S2} drops to zero through the body diode and the auxiliary loop current I_a raises to $I_{Lm,min}$ with the slope V_{C1}/L_a. After t_1, no current flows into the body diode of S_2 which means S_2 turned off under zero current conditions and there is no reverse recovery current generated by the antiparallel

diode. The time for this interval is referred as T_1

$$T_1=t_1-t_0=\frac{L_a\times I_{Lm,min}}{V_{C1}}. \quad (1)$$

Mode 2 (t_1~t_2): In this mode the auxiliary inductor L_a resonates with the parasitic capacitors cs_1 and cs_2, discharging cs_1 and charging cs_2. The switch voltage V_{cs1} drops to zero and V_{cs2} climbs to the output voltage. The calculations for the resonance process are presented using (2) to (4) and at t_2 the soft switching conditions are implemented when cs_1 is completely discharged

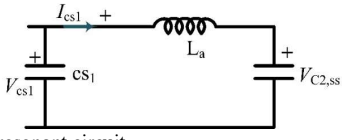


Fig. 3. Equivalent resonant circuit.

$$V_{cs1}=(V_o-V_{C2})\cos(\omega t)+V_{C2} \quad (2)$$

$$I_{cs1}=\frac{V_{C2}-V_o}{z}\sin(\omega t) \quad (3)$$

$$T_2=(t_2-t_1)=\frac{1}{\omega}\arccos\left(-\frac{V_{C2}}{V_o-V_{C2}}\right) \quad (4)$$

here, $cs_1=cs_2=cs$, z is the characteristic impedance of the resonant circuit and $z=\sqrt{(L_a/2cs)}$, ω is the natural frequency of the resonant circuit and $\omega=\sqrt{(1/2L_acs)}$.

Mode 3 (t_2~t_3): After t_2, the parasitic capacitor cs_1 is discharged completely, which provides zero-voltage conditions for S_1. The auxiliary current will first flow into the antiparallel diode and then into the channel of S_1 when the main switch starts to turn on. No overlapping area between the drain-source voltage and source current depicts no switching losses generated in this interval.

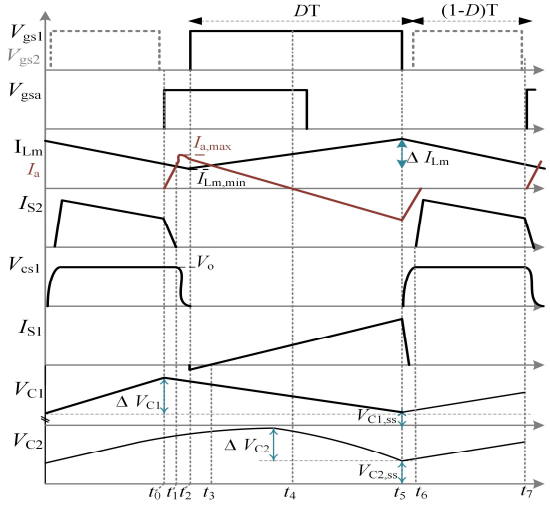


Fig. 4. Ideal waveforms of the proposed converter at steady state.

Mode 4 (t_3~t_4): At t_3, the auxiliary loop current starts decreasing to zero gradually with the slope V_{C2}/L_a. When the auxiliary current drops to the same as the output current, low-side output capacitor C_2 starts discharging, which provides energy to the load. At t_4, the auxiliary current drops to zero and the time of this interval is T_3

$$T_3=(t_5-t_4)=\frac{L_a\times I_{a,max}}{V_{C2}}\approx\frac{D}{2}T. \quad (5)$$

Mode 5 (t_4~t_5): The auxiliary loop current decreases with the same slope as mode 4 and reaches to the negative maximum value. The output capacitors C_1 and C_2 are discharged to steady state values $V_{C1,ss}$ and $V_{C2,ss}$, respectively. After t_4, the auxiliary current flows into the antiparallel diode or the channel of S_a and the auxiliary switch S_a can be turned off under zero-voltage switching. The time of this interval is the same as the mode 4

$$T_4=T_3\approx\frac{D}{2}T. \quad (6)$$

Mode 6 (t_5~t_6): The main switch S_1 turns off at t_5, and the auxiliary loop current will flow through the parasitic drain-source capacitor cs_1 and cs_2 that charges cs_1 to the output voltage and discharge cs_2 to zero. Because the parasitic capacitors have opposite charging and discharging processes compared with mode 2, turn-off losses are minimal in this topology. If additional snubber capacitors are used, cs_1 and cs_2 will minimize the slope of capacitor voltage to further reduce the turn-off losses. Once cs_2 is discharged completely, the freewheeling current flows into the body diode of S_2, and S_2 turns on under ZVS, resulting in no switching on losses for S_2.

Mode 7 (t_6~t_7): At the beginning of mode 7, the current freewheeling process starts. The main loop current flows into S_2 and the load. The output capacitors C_1 and C_2 are charged. The ripple of V_{C1} is the same as the ripple of V_{C2}, which can be calculated:

$$\Delta V_{C1}=\Delta V_{C2}=\frac{\Delta V_C}{2}=\frac{\Delta I_{Lm}}{16f_sC}. \quad (7)$$

B. Start State Operation

When the system starts, a pre-charging system charges the output capacitors to a certain ratio output voltage. C_1 and C_2 have the same capacitance, therefore, initially the output voltage will be balanced. However, during the start-up process, before the control signal is given to the auxiliary switch, the output capacitor C_1 is charged to the output voltage and C_2 is completely discharged i.e., V_{C1} will raise to the output voltage V_o and V_{C2} will drop to zero (Mode a-c). From the start until the steady state, the system can be divided into n intervals (n =1, 2, ⋯, N, ⋯). The start process duty ratio of the switch, S_1 is defined as d. The work modes are classified by a, b and c, which are described in Table II.

Mode a-This interval starts when the switch S_1 is conducting; the main loop current will flow into S_1 with the slope V_1/L_m. The current of the auxiliary loop will flow through switch S_1 with the slope V_{C2}/L_a that will discharge C_2. The two output capacitors will provide output current to the load. Equations dictating this mode are shown below:

$$I_{C1\,(n)}=I_{o\,(n)}=\frac{V_{C1\,(n)}+V_{C2\,(n)}}{R} \quad (8)$$

$$I_{C2\,(n)}=I_{o\,(n)}+I_{a\,(n)}. \quad (9)$$

Mode b-In this period, when the main switch S_1 turns off, the main inductor current freewheels through S_2 channel due to the synchronous rectification. The auxiliary loop current I_a will drop to zero with the slope V_{C2}/L_a. The source, V_1 charges C_1, C_2 and transfers energy into the load. The short time of this interval is defined as τ. The capacitor currents formulas are given below:

$$I_{C1\,(n)} = I_{Lm\,(n)} - I_{o\,(n)} + I_{a\,(n)} \quad (10)$$

$$I_{C2\,(n)} = I_{Lm\,(n)} - I_{o\,(n)} . \quad (11)$$

Mode c-The auxiliary loop will be disconnected as the body diode of S_a stops conducting while auxiliary loop current drops to zero. The source, V_1 charges the output capacitors, and transfers energy into the load. The capacitor currents are calculated by:

$$I_{C1\,(n)} = I_{C2\,(n)} = I_{Lm\,(n)} - I_{o\,(n)} . \quad (12)$$

The increment $\Delta V_{C1(n)}$ and $\Delta V_{C2(n)}$ of each period can be calculated from (13)-(14)

$$\Delta V_{C1\,(n)} = \frac{-I_{o\,(n)} \times d_{(n)}T + \frac{1}{2}\Delta I_{a\,(n)} \times \tau_{(n)} + (1-d_{(n)})T \times I_{C1(n)}}{C} \quad (13)$$

$$\Delta V_{C2\,(n)} = \frac{-\left[I_{o\,(n)} + \frac{1}{2}\Delta I_{a\,(n)}\right] \times d_{(n)}T + I_{C2(n)}(1-d_{(n)})T}{C} . \quad (14)$$

Here,

$$C_1 = C_2 = C$$

$$\Delta I_{a\,(n)} \approx \frac{V_{C2\,(n-1)}}{L_a} \times d_{(n)}T$$

$$\tau_{(n)} = \frac{C \times V_{C2\,(n-1)} \times d_{(n)}T}{C \times V_{C1\,(n-1)} - \frac{V_{C1\,(n)} + V_{C2\,(n)}}{R} \times d_{(n)}T}$$

The steady-state output capacitor voltages are expressed as:

$$V_{C1(N)} = \sum_{n=1}^{N} \Delta V_{C1\,(n)} + \frac{V_o}{2} \quad (15)$$

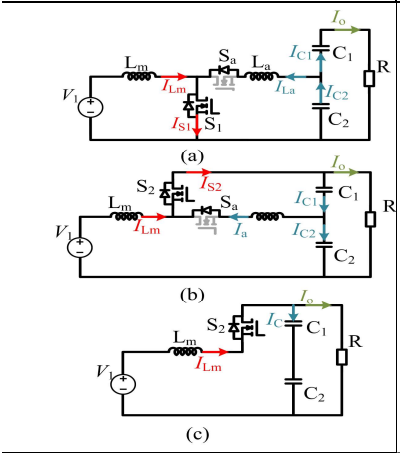
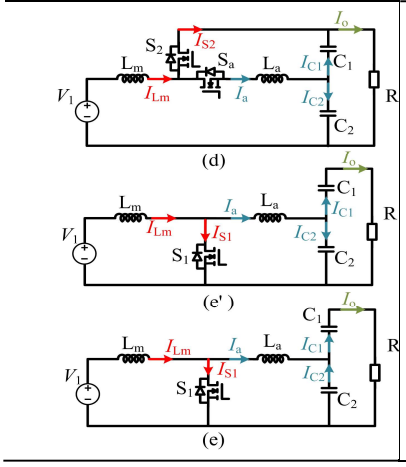
$$V_{C2(N)} = \sum_{n=1}^{N} \Delta V_{C2\,(n)} + \frac{V_o}{2} . \quad (16)$$

In mode a, C_2 discharges, which indicates the increment voltage ΔV_{C2} is negative. The voltage V_{C2} will decrease to zero gradually, whereas V_{C1} will grow up to V_o after some switching periods. The ideal current and voltage waveforms are illustrated in Fig. 5. To ensure some voltage across C_2 at the end of start-up process, the auxiliary MOSFET must be switched. This will require additional work modes such as mode d and mode e at the end of mode c and before mode a. The equivalent of sub-circuits for mode d and mode e are depicted in Table I. The ideal waveforms at a steady state with the control signals of the auxiliary switch are illustrated in Fig. 6.

Mode d-The auxiliary switch S_a is turned on before S_1 conduction, and the main loop current will now flow into the auxiliary loop as well with the slope V_{C2}/L_a. The auxiliary loop current will divide into two to charge C_2 and discharge C_1. With the current in the auxiliary loop, the current of C_1 will decrease to $-I_o$ in mode (d).

Mode e-S_1 is turned on and the output capacitor current I_{C2} gradually drops to zero (e'). The output capacitors C_2 and C_1 are still charged and discharged, respectively. The main inductor current still flows into the auxiliary loop, but the auxiliary current drops with the slop V_{C2}/L_a. At the end of mode e, the auxiliary loop current I_a reaches zero. Both output capacitors C_1 and C_2 are discharged to provide energy to the load during this interval.

TABLE II
Equivalent Sub-Circuits at Start State

Sub-circuit	Start condition
	These subcircuits work without the control signals of the auxiliary switch. The auxiliary loop current flows into the antiparallel body diode of S_a
	These subcircuits work with the control signals of the auxiliary switch. The work mode (e) ends before the work mode (a).

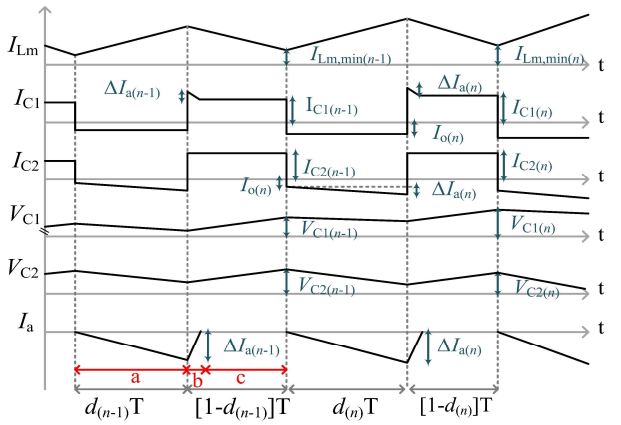


Fig. 5. Ideal waveforms without the auxiliary loop control: modes a, b and c.

When the stored and released charges in output capacitors are the same (I_a positive *area*$_1$ is equal to the negative *area*$_2$), the system reaches to steady state. The steady state values of the output capacitor voltages are defined as $V_{C1,ss}$ and $V_{C2,ss}$. Because of the additional charging of C_2 during mode d and mode e, there will be a finite steady state value for $V_{C2,ss}$. The soft switching condition for the converter is that $V_{C2,ss}$ stays less than 50% of the output voltage which will be demonstrated in section III.

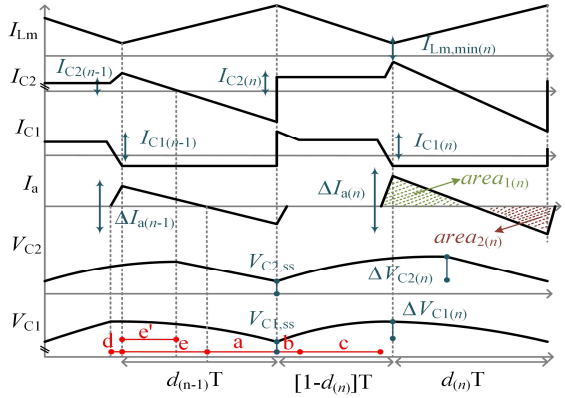


Fig. 6. Ideal waveforms with the auxiliary control: mode d, and e.

III. Soft Switching Validation and Analysis of Loss Breakdown

A. Soft Switching Validation

The main switch operates under soft-switching when the output capacitor can be discharged completely. V_{C2} must be smaller than half output voltage which can be calculated by using (11) to (14) to ensure complete ZVS. With different power loads, the maximum value of V_{C2} can be estimated using the minimum main inductor current in (18). Considering the minimum value of $I_{Lm,min}$ is $DTV_o/(4L_a)$, the maximum value of V_{C2} is $V_o/2$, which determines the voltage V_{C2} is less than 50% of the output voltage under the full range of power loads

$$V_{C2}-(V_o-V_{C2})\cos(\omega t)\le 0 \tag{17}$$
$$V_{C2}\le\frac{1}{2}V_o$$

$$V_{C2}=\frac{2I_{Lm,min}L_a}{DT}-\frac{4L_a{}^2V_o}{(DTz)^2}-\frac{2\sqrt{L_a{}^2V_o[-4DI_{Lm,min}L_a\,T\,z^2+4L_a{}^2V_o+(DTz)^2V_o]}}{(DTz)^2}. \tag{18}$$

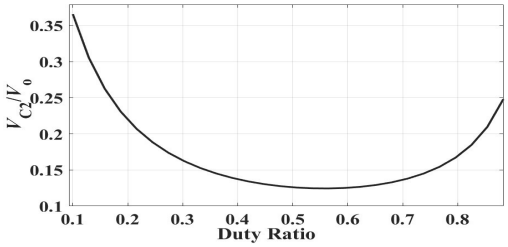


Fig. 7. The ratios of V_{C2}/V_o versus duty ratios.

For different duty ratios, the $I_{Lm,min}$ can be expressed by (19). The values of V_{C2}/V_o at different duty ratios are shown in Fig. 7. The results provide evidence that with different power loads, the maximum V_{C2} is less than half of the output voltage

$$I_{Lm,min}=\frac{P_i}{V_1}-\frac{DV_1}{2f_sL_m}. \tag{19}$$

Thus, despite no additional control scheme, soft switching can be achieved under the whole range of power loads and duty ratios.

B. Loss Breakdowns

The loss breakdown of the proposed converter is composed of the conduction losses, part switching off losses, passive component losses such as inductor losses, including the core losses, and wingding losses. The efficiency of the hard switching boost converter and the proposed soft switching converter will be evaluated under the same operation conditions using the datasheet information and the experimental results. The main switch and auxiliary switch conduction losses can be calculated from (20)-(24)

$$P_{S1,con}=R_{S1}I_{in}{}^2D\times[1+\frac{1}{12}\left(\frac{\Delta I_{Lm}}{I_{in}}\right)^2] \tag{21}$$
$$P_{S2,con}=R_{S2}I_{in}{}^2\times(1-D)\times[1+\frac{1}{12}\left(\frac{\Delta I_{Lm}}{I_{in}}\right)^2] \tag{22}$$
$$P_{S,con}=P_{S1,con}+P_{S2,con} \tag{23}$$
$$P_{Sa}=R_{Sa}\,I_{a,rms}^2 \tag{24}$$

where, R_{S1}, R_{S2}, and R_{Sa} are the conduction resistance of main switch S_1, the synchronous rectification switch S_2 and the auxiliary switch S_a, respectively (reading from the datasheets). I_{in} is the input DC current.

The converter eliminates switching losses in S_2, S_a and turn on switching losses in S_1. Stored energy in parasitic capacitors (cs_1 and cs_2) is recovered which helps to reduce the switch-off losses. The switching losses, including the switching on losses $P_{S,on}$, the switching off losses $P_{S,off}$ and the commutating body diode reverse recovery losses $P_{S2,drr}$ are calculated by:

$$P_{S,on}=\frac{1}{2}V_o\times\left(I_{in}+\frac{\Delta I_{Lm}}{2}\right)\times f_s\times t_f \tag{25}$$
$$P_{S,off}=\frac{1}{2}V_o\times\left(I_{in}-\frac{\Delta I_{Lm}}{2}\right)\times f_s\times t_r \tag{26}$$
$$P_{S2,drr}=V_o\times Q_{rr}\times f_s. \tag{27}$$

Device parasitic output capacitor cs losses happen in the hard switching converter, which can be found by:

$$P_{S,coss}=\frac{1}{2}V_oQ_{cs}f_s \tag{28}$$

where, t_f and t_r are turn-off fall time and turn-on rise time of the switches. Q_{rr} and Q_{cs} are the reverse recovery charge of the body diode and device output capacitor's charge, respectively. $R_{Lm,dc}$, $R_{Lm,ac}$, and $R_{Lm,dc}$ are wingding DC and AC resistances which were estimated using an impedance analyzer.

$$I_{a,rms}=\sqrt{\begin{aligned}&-4[T_1V_{C1}z+L_aV_{C1}\sin(T_2\omega)]^3+\frac{4T_1{}^3V_{C1}{}^2}{3L_a{}^2T}+\frac{[T_1V_{C1}z+DT(-V_1+V_{C1})z+L_aV_{C1}\sin(T_2\omega)]^3}{3L_a{}^2T(-V_o+V_{C1})z^3}\\&+\frac{V_{C1}{}^2[2L_a{}^2T_2\omega+8L_aT_1z+4T_1{}^2T_2\omega z^2-8L_aT_1z\cos(T_2\omega)-L_a{}^2\sin(T_2\omega)]}{L_a{}^2T\omega z^2}\end{aligned}} \tag{20}$$

TABLE III
EQUIVALENT SUB-CIRCUITS AT STEADY STATE

Reference	Frequency	Control method	MOS Number	Diode Number	Switch Currents Stress	Soft Switching Duty Range	Full load Efficiency
[11]	50 kHz	Simple	2	3	Normal	50% to 100%	97.1%
[12]	112 kHz	Simple	4	5	Normal	Full	98.7%
[14]	110 kHz	Complex	2	1	High	Full	95.2%
[15]	200 kHz	Complex	4	0	Very High	Full	97.8%
[17]	30 kHz	Simple	2	3	High	Full	96.23%
Proposed Topology	200 kHz	Simple	3	0	Normal	Full	95.7%

The main inductor and the auxiliary inductor are designed with ETD 54 and ETD 34 ferrite cores, respectively. The core losses can be estimated using the switching frequency, the core size and peak-to-peak current ripple. Winding losses of the main inductor and auxiliary inductor can be calculated using DC and AC winding resistances

$$P_{\mathrm{Lm,\ core}}=k_{1\mathrm{m}}f_{\mathrm{s}}^{\alpha\mathrm{m}}\times(k_{2\mathrm{m}}\Delta I_{\mathrm{Lm}})^{\beta\mathrm{m}} \tag{29}$$

$$P_{\mathrm{Lm,\ winding}}=\mathrm{R}_{\mathrm{Lm,dc}}I_{\mathrm{in}}{}^{2}+(\frac{\Delta I_{\mathrm{Lm}}}{12})^{2}\times\mathrm{R}_{\mathrm{Lm,ac}} \tag{30}$$

$$P_{\mathrm{La,\ core}}=k_{1\mathrm{a}}f_{s}^{\alpha\mathrm{a}}\times(\mathrm{k}_{2\mathrm{a}}\Delta I_{\mathrm{a}})^{\beta\mathrm{a}} \tag{31}$$

$$P_{\mathrm{La,\ winding}}=\mathrm{R}_{\mathrm{La,ac}}\times(\frac{\Delta I_{\mathrm{a}}}{12})^{2} \tag{32}$$

where $k_{1\mathrm{m}}$, $k_{2\mathrm{m}}$, $k_{1\mathrm{a}}$, $k_{2\mathrm{a}}$, α_{m}, α_{a}, β_{m}, and β_{a} depend on the core material, operation frequency and operation temperature.

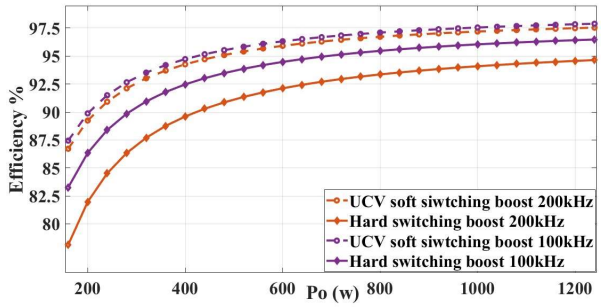


Fig. 8. Efficiency comparison between the proposed soft switching converter and hard switching converter.

The efficiency of the proposed UCV soft-switching boost converter and hard-switching boost converter with different switching frequencies and power loads are given in Fig. 8. The calculation results demonstrate that the efficiencies of the soft switch converter are still higher than the hard switching converter. For a 1.2 kW output (considering overload conditions during dynamic load changes), the maximum efficiency of the proposed soft-switching converter at both 100 kHz and 200 kHz exceeds 97.49%, whereas the maximum efficiencies of the hard switching converter with the switching frequency of 100 kHz and 200 kHz are 96.4% and 94.6%, respectively. For the light load at 200 W, the efficiencies of the soft switching converter can reach 90% at 100 kHz and 89.8% at 200 kHz, but the efficiencies of the hard switching converter are 83.2% and 78.1%, respectively for the two switching frequencies. The percentage of auxiliary loop losses to the total losses in the proposed converter are from 5.6% to 5.8%, whereas the percentages of the switching losses to the total losses at hard switching are from 44.8% to 56.8%. Considering that the turn off losses for S_1 are not completely removed in this topology, the efficiency at 200 kHz is slightly less than that at 100 kHz. If we want the same peak efficiency for the hard switching converter as the proposed converter a lower switching frequency (50 kHz) will be needed. The consequence will be a larger inductor with EE65 ferrite core which means a 220% increase in passive component volume. Although the auxiliary loop generates additional conduction losses and passive component losses, the overall auxiliary loop losses are evidently less than the switching losses of the hard switching converter and the proposed soft switching topology reduces 60% of total losses.

IV. COMPARISON BETWEEN SOFT SWITCHING BOOST CONVERTERS

This section presents a comparison of the proposed converter with the previously published soft switching boost converters. The classic soft switching boost converters [11]-[17] are compared based on the function of circuits, switching frequency, number of additional devices, switch current stress, soft switching duty ratio range and full load efficiency as shown in Table III. The snubber-assisted zero-voltage and zero-current transition (SAZZ) boost converter [11], [12] operates under simple control methods. The auxiliary loop assists zero voltage switching for the main loop switch as the freewheeling current flows into an auxiliary loop before the main switch conduction. But soft switching only happens when the duty ratio is between 50% to 100%. The interleaved SAZZ converter employs a 2:1 pulse transformer to expand the soft switching range [13]. However, the auxiliary loop needs at least three additional semiconductor devices, and the additional magnetic component generates not only more losses but also increases the size and weight of the converter.

The auxiliary resonant commutated pole (ARCP) converter uses a smaller number of devices [14]. The auxiliary switches conduct before the main switch turns on and off. But the control method is complex, and the soft switching depends on complex charges calculation. Hard switching happens when the input power changes rapidly. The four-switch bidirectional buck boost (FSBB) converter constructs a full bridge with an inductor [15]. The main inductor current will drop to negative and create zero voltage switching conditions when the main switches turn on. However, the requirement of large current ripple increases the RMS inductor current and the switch current stress, enhancing conduction losses. To minimize losses and enable soft switching, it is essential to accurately calculate the sub-periods for each stage. Additionally, the control of four switches demands precise management of their switching times to facilitate seamless transitions between distinct operating stages. This requirement underscores the need for sophisticated control algorithms and precise timing. The complex control method increases the calculation and response time of the microcontroller, which makes high

switching frequency operation quite challenging. In [17], a HI-bridge auxiliary resonant circuit is used in the boost converter. The simple control system requires the auxiliary switch to be turned on before the main switch conducts current. The resonant process assists in discharging the parasitic capacitor parallel to the main switch and helps the main switch turn on under ZVS. However, The HI-bridge auxiliary loop consists of six extra devices, which increases the size and additional conduction losses in the auxiliary loop. Although the auxiliary inductor is connected to the auxiliary loop which is separated from the power loop, the auxiliary loop RMS current is still very high and the switch undertakes high current stress. Therefore, the challenges of these converters are implementing soft switching using a smaller number of additional devices with a simple control method. Regarding the proposed UCV boost converter, only one switch is used in the auxiliary loop, and a straightforward control method is implemented for the closed loop control (Section V.B). Therefore, this is a competitive candidate to reduce device numbers, increase the system reliability, and improve efficiency.

V. Converter Soft Switching Validation

A. Prototype Description

The experimental prototype used SiC MOSFET (SCTW100N120G2AG) operating at 200 kHz. The low input voltage of 240 V was stepped up to 500 V. 22 µF MKP film capacitors were selected as the input filter capacitor and output unbalanced voltage capacitors. The main loop inductor was designed using ETD 54 ferrite core. The tested inductance was 875 µH and the DC and AC resistances were 57 mΩ and 0.86 Ω , respectively. The value of the auxiliary inductor, L_a will decide the RMS of the auxiliary loop current and the pre-open time (defined as T_{pre}), the sum of sub-periods of mode 1 and mode 2 (T_1+T_2). The relationship between L_a and RMS of the auxiliary loop current and the pre-open time are presented in Fig. 9. For the experimental prototype, A 5 µH auxiliary inductor is designed to limit the RMS auxiliary current to less than 3.2 A and to achieve a pre-open time of 0.15 µs at the rated operating condition.

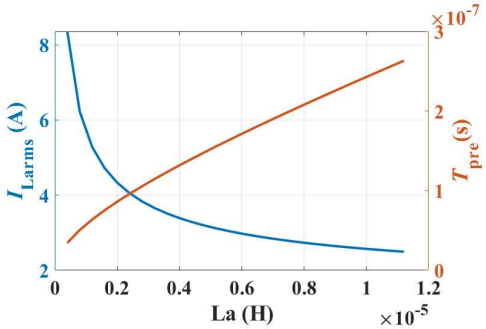


Fig. 9. Calculated the RMS auxiliary loop current and per-open times for different auxiliary inductance.

The small-size auxiliary inductor was designed using ETD 34 ferrite core which has an AC resistance of 0.61 mΩ. All inductors used Litz wires. The closed-loop control was implemented using a TI TM320F28379D launchpad. The prototype circuit parameters are presented in Table IV.

TABLE IV
Circuit Parameters

Parameters	Values
V_I	200 to 240 V
V_o	400 to 500 V
L_m	875 µH
L_a	5 µH
C_1, C_2, C_{in}	22 µF
f_s	200 kHz
P_o	1 kW
Duty ratio	0.4 to 0.52

B. Control Principle of Proposed Topology

The proposed converter employs a simple control method. The auxiliary switch is demanded to be on just before the main switch S_1 turns on. ZVS turn on of the main switch happens only when the T_{pre} is greater than T_1+T_2 calculated from (10) and (13). As after t_5, the loop current will recharge cs_1 and cause hard switching of the main switch, a range of T_{pre} are calculated from (33). The use of a look-up table method with fixed values of pre-open times proves to be effective for a wide range of conditions, offering a simple control system that achieves fast response.

$$T_1+T_2<T_{pre}<\frac{\frac{V_o-V_{C2}}{z}\sin(\omega T_2)}{\sqrt{3[(\frac{I_{in}}{DT})^2+(\frac{V_{in}}{4\sqrt{3}L_m})^2]}}+T_1+T_2\,. \quad (33)$$

The PI control is utilized to stabilize the output voltage and power. The double close loop control is presented in Fig. 10, where R_{Lm} is the inductor resistor, R is the output resistor, C is capacitance of C_{in}, C_1 and C_2. The loop-gain bode plot is given in Fig.11, which the zero-crossing point, ω_c is 7 kHz and the phase margin, φ_m is 105 degrees which ensures a fast response and good stability. The transfer functions of the converter are given by (34) and (35)

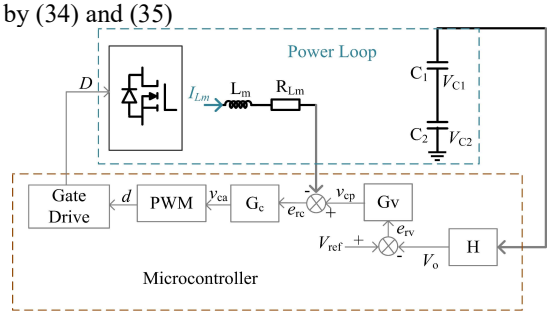


Fig. 10. Closed-loop controller.

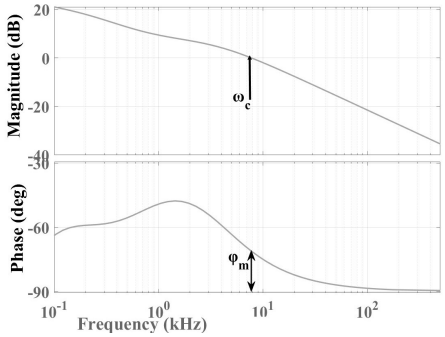


Fig. 11. Loop-gain bode plot of the proposed system (full-load condition).

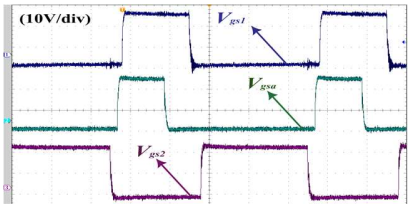


Fig. 12. Experimental results of gate source voltages.

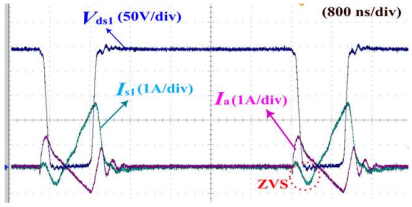
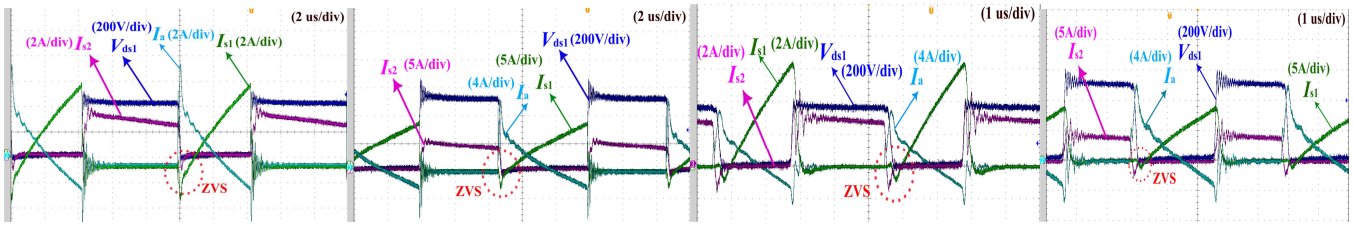


Fig. 13. Experimental results at P_o=88 W, f_s=200 kHz and V_{in} = 200V.



(a) (b) (c) (d)

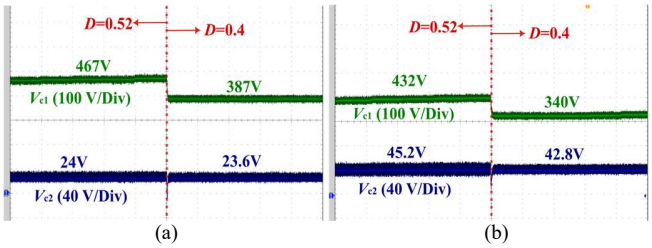
Fig. 14. Experimental results at 1kW, 240V input: (a) D=0.4, f_s=100 kHz; (b) D=0.52, f_s =100 kHz; (c) D=0.4, f_s =200 kHz; (d) D=0.52, f_s =200 kHz.

$$G_{gi}=\frac{\widehat{V}_{C1}}{\widehat{I}_L}=\frac{RL_mI_{Lm}C\times s+R[D(V_{C1}+V_{C2})C+I_{Lm}CR_{Lm}]}{(V_{C1}C^2R+V_{C2}C^2R)\times s+C(V_{C1}+V_{C2}-DI_{Lm}R)} \quad (34)$$

$$G_{id}=\frac{\widehat{I}_L}{\widehat{d}}=\frac{(V_{C1}C^2R+V_{C2}C^2R)\times s+C(V_{C1}+V_{C2}-DI_{Lm}R)}{L_mC^2R\times s^2+(L_mC+C^2RR_{Lm})\times s+CR_{Lm}+D^2CR} \quad . \quad (35)$$

C. Experimental Results

The 1 kW experimental prototype was built in the laboratory to evaluate the performance of the proposed UCV boost converter. The converter was tested with 100 kHz and 200 kHz switching frequencies. It was also tested for the full range of duty ratios and power loads. The experimental gate-source voltages for the main switch V_{gs1}, the synchronous rectification switch V_{gs2}, and the auxiliary switch V_{gsa}, are given in Fig.12. Main loop freewheeling current I_{S2}, auxiliary loop current I_a, main switch current I_{S1} and switch drain-source voltage V_{S1} are captured. The soft switching at a light load condition (88W) with 20% duty ratio has been validated (Fig.13). Fig. 14 (a) and (b) show the proposed topology operating under the switching frequency of 100 kHz. Fig. 14 (c) and (d) show the proposed circuit operating under the switching frequency of 200 kHz. For both duty ratio less than 50% and over 50%, the freewheeling current (I_{S2}) drops to zero with the auxiliary loop current gradually increasing, and the gradual charging of cs_2 eliminates the S_2 switching losses. With the assistance of the resonant link, the output capacitor of switch S_1 is discharged to zero and the auxiliary loop current flows into the antiparallel body diode of S_1. Therefore, the switch S_1 turns on under zero voltage switching.



(a) (b)

Fig. 15. Experimental results of unbalanced capacitor voltages under duty ratio from 0.4 to 0.52: (a) 100 kHz; (b) 200kHz.

The soft switching condition for this converter is that the unbalanced capacitor voltage V_{C2} is less than half of the output voltage. Fig. 15 (a) and (b) depict the unbalanced capacitor voltages, V_{C1} and V_{C2}. When the system works at 100 kHz, the ratios between the unbalanced capacitor voltage V_{C2} and the output voltage are 0.05 to 0.06, with the duty ratios from 0.4 to 0.52. For 200 kHz operation, the V_{C2} to V_o ratios are 0.09 to 0.1, with the duty ratios from 0.4 to 0.52. Evidently, the proposed converter implements soft switching at these conditions (Fig. 14).

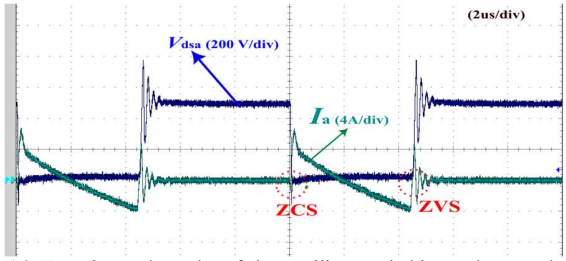


Fig. 16. Experimental results of the auxiliary switching voltage and current (100 kHz, 1 kW, D=0.42).

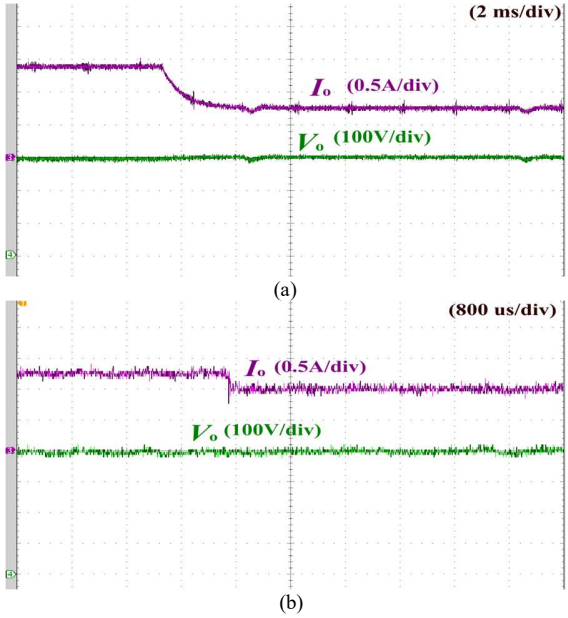


Fig. 17. Experimental results of dynamic response tests: (a) f_s=100 kHz, P_o=420 W to 230W; (b) f_s=200 kHz, P_o=520 W to 400W.

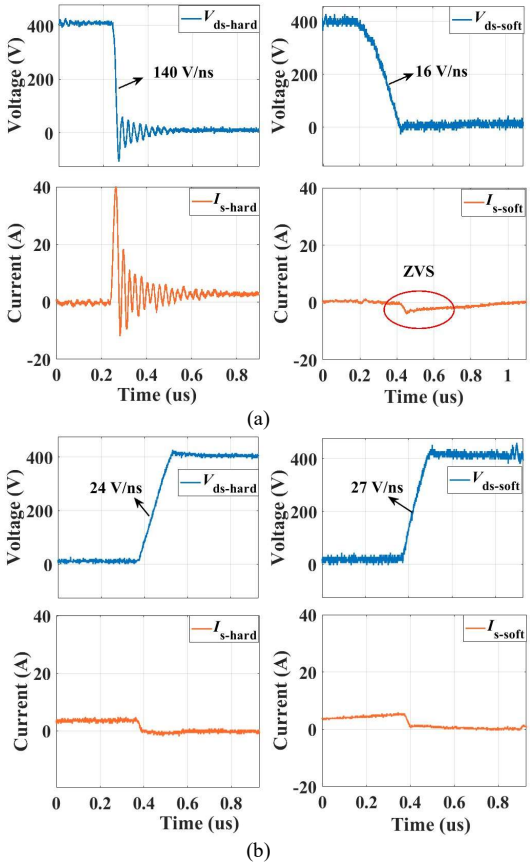


Fig.18. Switching transient voltage and current waveforms of the conventional converter and proposed converter: (a) switching on; (b) switching off. (Vin=240V, Vo=400V, Po= 1kW)

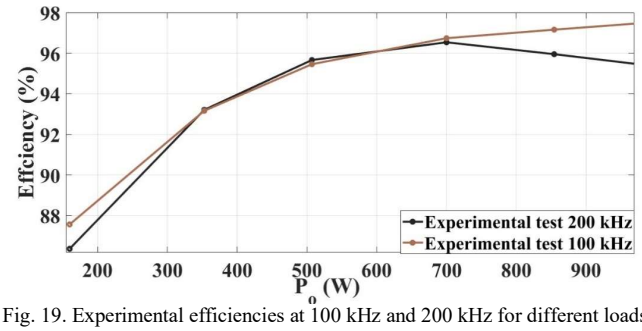


Fig. 19. Experimental efficiencies at 100 kHz and 200 kHz for different loads

The freewheeling synchronous rectification switch S_2 switching voltage is complementary to S_1 switching voltage, so only switching current is shown in this section which proves S_2 turns on under ZVS and turns off under ZCS. The auxiliary switch S_a switching voltage and current at 100 kHz are shown in Fig. 16. The auxiliary switch turns on under ZCS and turns off under ZVS. Dynamic response tests are shown in Fig. 17. When the power changes from 420 W to 230 W under 100 kHz (as shown in Fig. 17 (a)), the output current changes from 1.4 A to 0.75 A and the output voltage remains fixed to 300 V. Fig. 17 (b) shows when operating at 200 kHz, as the power changes from 520 W to 400 W, the output current changes from 1.3 A to 1 A. The faster response time and good dynamic control system keep the output voltage fixed to 400 V.

The *dv*/*dt* of the main switch voltages are compared for both the turn-on and the turn-off situations. The waveforms for the proposed converter are shown in the right-side plot whilst the waveforms of the hard switching converter are shown on the left-side plots in Fig. 18. The most significant difference can be seen in the turn-on process where a *dv*/*dt* reduction of almost an order of magnitude is achieved from 140 V/ns for the hard switched converter to 16 V/ns for the proposed converter. This significant reduction in turn-on *dv*/*dt* has another beneficial effect in the elimination of the very large resonances in the switch current and voltages which will significantly reduce the EMI. The turn-off process on the other hand sees a small (+10%) increase in *dv*/*dt* for the soft switched converter caused mainly by the auxiliary loop current flows into drain-source capacitors of S_1 and S_2. The current supports S_2 turns on under ZVS and there is no associated resonance caused. It can be concluded that the reduction in *dv*/*dt* during turn-on and elimination of the associated resonance is a significant feature of the proposed circuit that will contribute to a significant improvement in EMI. Therefore, the proposed topology does not require additional arrangements such as large gate resistors, additional sinewave EMI filters with a low cut-off frequency, or large *dv*/*dt* filters to tackle the EMI issues of the boost converter. The efficiencies are checked in experimental tests for the switching frequency 100 kHz and 200 kHz, as shown in Fig. 19. The efficiencies at full power load are 97.6% at 100 kHz and 95.7% at 200 kHz. At light load, the efficiencies are 87.7% at 100 kHz and 86.3% at 200 kHz, which reduces 36% to 59.8% of total losses compared with the estimated losses of the hard switching converter.

VI. Conclusion

This article presents the topology description, operating principle, qualitative theoretical analysis, and experimental validation for the novel unbalanced capacitor voltage soft switching boost converter. This proposed converter has several advantages over other published active resonant boost topologies:

1) The proposed topology employs a simple auxiliary circuit configuration, including a small size auxiliary inductor and an active switch. The small number of devices can reduce the size and the cost of the converter.
2) The unbalanced output capacitor structure brings soft switching benefits by getting the low-side capacitor voltage down to less than half of the output voltage. It provides sufficient soft switching conditions for full range of duty ratios and power loads.
3) Different from the ARCP and FSBB converters, a straightforward control method is realized. The pre-open time can be stored in an offline look-up table, which reduces the response time of the microcontroller and increases the reliability of the closed-loop controller.
4) Although the additional conduction losses are generated in the auxiliary loop, the elimination of switching losses reduced 60% of the total losses when compared with a 200 kHz hard switching converter. The proposed topology improves the efficiency to 97.6% at 100 kHz and 95.7% at 200 kHz switching frequency. This improvement in efficiency could allow down-sizing of the converter

heatsink and the increased switching frequency could allow down-sizing of passive components, thereby increasing power density of the converter.

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