Effect of Rapid Thermal Annealing on The Electrical Properties of Dilute GaAsPN Based Diodes.

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Abstract:

The effect of rapid thermal annealing on the electrical properties of p^{++}GaP/p^{-}GaAsPN/n^{+}GaP diodes were investigated by using Current – Voltage (I-V), Capacitance-Voltage (C-V) and Deep Level Transient Spectroscopy (DLTS) techniques in the temperature range from 100K to 440K. It was observed that rapid thermal annealing treatment improves the electrical characteristics of as-grown structures. The annealed samples showed an ideality factor lower than the as-grown samples for all temperatures. The ideality factor values from I-V characteristics has changed between 6.8 and 1.9 in the temperature range of 110-430K for as grown diode, and between 6.3 and 1.44 in the temperature range 100-400K for the annealed diode. On the other hand, the barrier height increases and the ideality factor decreases with increasing temperature for all samples. The barrier height values has changed between 0.29 eV and 0.71eV in the temperature range of 190-430K for as grown diode, and between 0.38 eV and 0.77eV in the temperature range 180-420K for the annealed diode. High values of barrier heights were observed in the annealed samples due to the barrier height in-homogeneities at the p-i-n junction.

The net acceptor concentration was calculated to be 1.18 x10^{18} cm^{-3} and 2.11x10^{18} cm^{-3} for the as-grown and annealed GaAsPN layers, respectively. The net acceptor concentration increases by ~56% and the leakage current of the GaAsPN/GaP p-i-n junction decreases by1-2 orders after RTA.

DLTS and Laplace-DLTS measurements reveal three hole traps, $H1_{an}$(0.06eV), $H2_{an}$(0.065eV) and H3(0.23eV) in the annealed samples as compared with two hole traps, $H4_{ag}$(0.07eV) and H5(0.25eV) in the as-grown samples. After rapid thermal annealing an extra shallow trap is created.**Keywords:**

GaAsPN – Deep Level Transient Spectroscopy - Rapid Thermal Annealing – Ideality factor – Barrier height – Series resistance.

1.Introduction:

Recently, III-V-N (dilute nitrides) materials classify as a new class of semiconductors due to their unusual and fascinating new physical properties that are rarely seen in other conventional alloys as well as their intriguing potentials for device applications[1]. For example, the band gap energy of III-V semiconductors can be tuned by changing the nitrogen content. Dilute nitride semiconductors can be grown by incorporating small amounts of nitrogen (1-4%) in to the III-V host lattice to form a ternary compound (III-V-N). In addition, for example by adding As in to GaPN quaternary alloys, (GaAsPN) can be fabricated[2]. These materials which can be grown by molecular beam epitaxy (MBE) and metalorganic vapor phase epitaxy (MOVPE) are very attractive for light emitting and light absorbing devices [3,4,5].These materials have highly desirable optical properties and crystal structure for lattice matching to common substrate such as Si [2] and GaP [6] substrates. For instance, the band gap energy of GaAsPN alloy with 6% nitrogen composition is 1.7eV which is ideal for efficient GaAsPN/Si tandem solar cells [7]. With the absence of a window layer and non-optimum band gap, a conversion of 7.9% was achieved for GaPN- based solar cell with N =1.8% and E_g=2.05eV on GaP substrates. Most researches on III-V-N alloys including GaAsPN depend on low nitrogen composition less than 3% because of low solubility of nitrogen in III-V compounds at thermodynamic equilibrium[8]. Theoretically, by adding Al, As, In or Sb and controlling N content in the layer lattice –matched GaAsPN alloys having bandgap around 1.7eV can be fabricated allowing the current matching with the Si-cell [9]. However, dilute III-V nitride layers with high N content are known to have poor structural quality due to the low solubility of N in GaP, However, structural optimization has been demonstrated through annealing processes[10].

The crystal defects especially misfit dislocations, generated in the matrix during metamorphic growth is responsible of carriers lifetime shortening and thus the reduction of the current extraction. These effects affect the efficiency of multi-junctions solar cells. However, post growth annealing process{11,12] have been used to reduce and remove these generated defects. Therefore, the optimization of the dilute nitride material growth and annealing condition are key points for improving their photoelectric properties[13,14,15].

In this work, we report on the effects of thermal annealing on the electrical properties of dilute Gallium Arsenide Phosphide Nitride (GaAsPN) based p-i-n diodes using current – Voltage (I-V), Capacitance-Voltage (C-V) and Deep Level Transient Spectroscopy (DLTS) techniques.

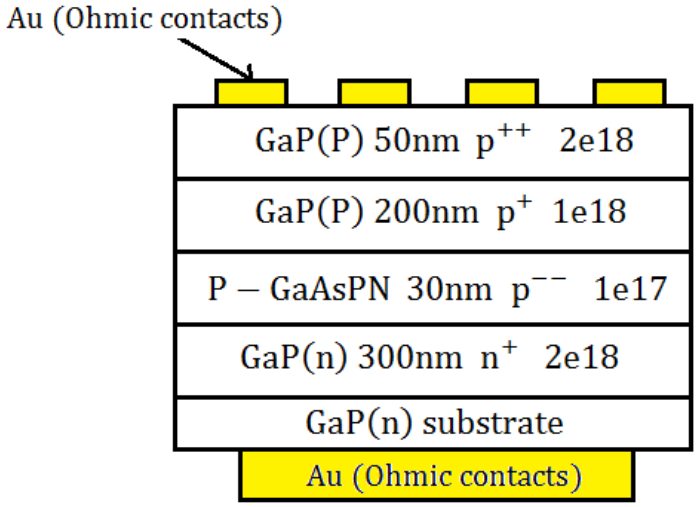
The experimental results show that the rapid thermal annealing samples have better electrical properties than the as- grown samples.

2.Experimental Details

In this study, p^{++}GaP/p^{-}GaAsPN/n^{-}GaP diodes samples were grown by molecular beam epitaxy (MBE). The epitaxial growth sequence is illustrated in Scheme.1, and consisted of 300 nm thick n^{+} GaP ($n=2x10^{18}$ cm^{-3}) on GaP substrate, followed by deposition of 30nm p-type p--GaAsPN ($p=1x10^{17}$ cm^{-3}) layer. A further 200 nm p^{+} GaP ($p=1x10^{18}$ cm^{-3}) and a 50 nm p^{++} GaP ($p=2x10^{18}cm^{-3}$) layers were deposited. Si and Zn are used as the n-type and p-type dopant for the n^{+} and p^{-} and p^{++} epitaxial layers, respectively. The growth rate was 0.2 monolayer/s (ML/s). The

V/III beam equivalent pressure (BEP) ratio has been set at 10. In order to obtain a GaAsPN compound lattice matched to the GaP substrate and the As flux has been set at 0.2 µTorr . After growth, the samples were divided in two groups, the first one was kept in the growth condition and the second one was annealed at 800°C for 5 mins under N_2 ambient in an RTA (rapid thermal annealing) system, the ramp-up temperature used is 100°C/s. For both two samples (as-grown and annealed) ,an Au circular ohmic metal contacts were then deposited by thermal evaporation on the top and the bottom of the doped epilayers.

The samples have been studied by I-V and C-V measurements using a current source unit (Keithley 236) and Boonton capacitance meter (B7200), respectively which are controlled by software. These measurements were performed in a vacuum cryostat (model Janis CCS-450) with a liquid –nitrogen cooling system. The capacitance meter (Boonon 7200) and pulse generator (Agilent 33220A) are used to get more information about defects.



Scheme.1 Devices structure of p^{++}GaP/p^{-}GaAsPN/n^{-}GaP diodes grown by MBE.

3.1 Current - voltage characteristics of as-grown and annealed diodes:

In order to study the effect of rapid thermal annealing on the electrical properties of dilute GaAsPN, The I-V measurements were performed at different temperatures. Fig.1 shows the current –voltage characteristics at room temperature for as-grown and annealed p^{++}GaP/p^{-} GaAsPN/n^{-}GaP diodes. It can be seen that the reverse current is reduced considerably when the sample is annealed. The leakage current of the annealed diodes is one to two orders of magnitude lower than the as-grown diodes. The lower reverse current observed in the annealed diodes indicates that there is a reduction of the concentration of the defects which act as generation – recombination centers[16]. The annealing process decreases the concentration of major defects and consequently contributes to the decrease of the leakage current[17].Similar observation has been reported by Xie et al [18].

The thermal annealing process is therefore an efficient way to improve the electrical properties of these devices. This improvement could be attributed to a decrease in the defects concentration and /or their transformation. This effect will be investigated further using DLTS measurements as described below. In addition, the turn on voltage (V_{on}) increases when the samples are annealed. V_{on} is 0.7V and 0.9V for as-grown sample and annealed samples, respectively. This behavior can be attributed to the increase of the excess capacitance due to the interface states[19].

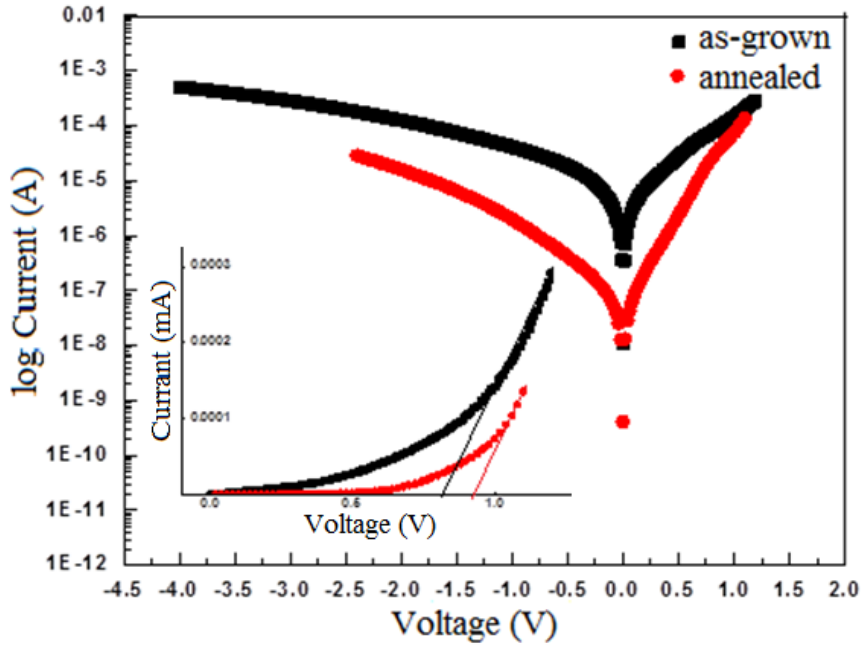


Fig.1 Plot of the log Current –Voltage characteristics of as-grown and annealed p^{++}GaP/p^{-}GaAsPN/n^{-}GaP diodes. The insert shows the turn on (V_{on}) of as-grown and annealed diodes.

The p-i-n junction current –voltage (I-V) characteristics can be described by the thermionic emission (TE) model with a series resistance (R_S)[20,21]:

$$I = I_s\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where q is the electronic charge, V is the forward applied -bias, k is the Boltzmann constant, n is the ideality factor, I_s is the saturation current and T is the absolute temperature in Kelvin.

The expression of the saturation current, I_s is given by:

$$I_s = AA^{**}T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

where A is the effective diode area and A^{**}= 98.2 $Acm^{-2}K^{-2}$ is the effective Richardson's constant for n-GaP and ϕ_B is the barrier height [22].

The semi-logarithmic I-V characteristics of the diode samples at room temperature are illustrated in figure1. Figure.2 shows the temperature dependence of the ideality factor calculated from the semi-logarithmic I-V curves for as-grown and annealed samples over the temperature range 100 - 440K. For all samples, it is evident that the ideality factor (n) increases with decreasing temperature. The ideality factor values has changed between 6.8 and 1.9 in the temperature range of 110-430K for as grown diode, and between 6.3 and 1.44 in the temperature range 100-400K for the annealed diode [23]. Similar trends have been reported by other researchers [24,25]. This is due to the current transport across the p-i-n interface which is temperature activated process [26,27]. For all samples in the temperature range of (300K to 440K), the values of ideality factor are greater than unity and close to 2. This behavior can be attributed to the generation-recombination mechanism, interface states, the series resistance and barrier height in-homogeneities[28]. However, the annealed samples have low ideality factor values compared with the as-grown samples indicating that the annealed samples are close to ideal diodes than the as-grown devices. For all samples, the higher values of ideality factor at low temperatures are caused by the presence of thermionic field emission, which contribute to the pure thermionic emission[29]. This phenomenon of the increase of the ideality factor with decreasing temperature is known as the T_o effect [30]. The ideality factor is inversely proportional with temperature as given by :

$$n(T) = n_o + \frac{T_o}{T} \dots\dots\dots (3)$$

where n_o and T_o are constant. Figure. 5 shows that the ideality factor is temperature dependent. The calculated values of n_o and T_o for as-grown and annealed samples are 0.5 and 625K and 0.25 and 366K, respectively. The higher values of n_o and T_o of the as- grown samples indicate that the annealed samples deviates less from the thermionic emission model than the as-grown samples[31].

The values of the barrier height calculated from the I-V characteristics of our $p^{++}GaP/p^{+}GaAsPN/n^{-}GaP$ diodes are shown in figure.3. The barrier height increases with increasing temperature. This temperature dependence of the barrier height is due to the effect of barrier in-homogeneities at the p-i-n interface[32].

The barrier height has the values of 0.29eV at 190K and 0.71eV at 430K for the as-grown samples while The barrier height has 0.32eV at180K and 0.77eV at 420K for the annealed samples. The decrease in barrier height with decreasing temperature due to the fact that the current prefer to flow through the lowest barrier height [33]. Figure 6 shows a linear relation between the barrier height and ideality factor. As can be seen from figure 6, the lower ideality factor the higher the barrier height. This behavior can be explained by in-homogeneities of the barrier height which arise from different factors such as the surface defect density, the deposition process and surface cleaning[34,35].

The relation between barrier height and ideality factor n for as-grown samples exhibit high values than the annealed structures. Therefore, it can be concluded that the annealing act as important process for improving the electrical properties, and this can be attributed to several

factors such as the lateral inhomogeneity along the barrier height, interfacial GaAsPN layer, grain boundaries and non-uniformly distributed dislocations (interfacial changes) [36,37].

The effect of series resistance on the electrical characteristics of p++GaP/p++GaAsPN/n-GaP structure in the temperature range 110-440K is shown in Figure .4. The series resistance plays an important role in p-i-n diodes. At low forward bias voltage, the semi-logarithmic I-V characteristics are linear and deviate significantly from linearity at high voltages. This behavior is attributed to the effect of series resistance (R_s) which is due to the interface states and the interfacial insulator layer when the applied voltage is large enough[38]. The lower values of Rs of the annealed samples as compared with the as-grown sample at all temperatures indicate that the annealing process lowers the interfaces states density[39].

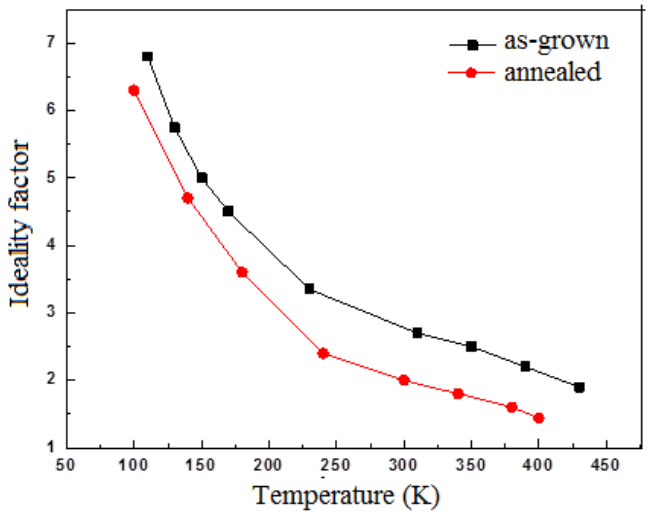


Fig.2 Temperature dependence of the experimental ideality factor from I-V characteristics of as-grown and annealed samples.

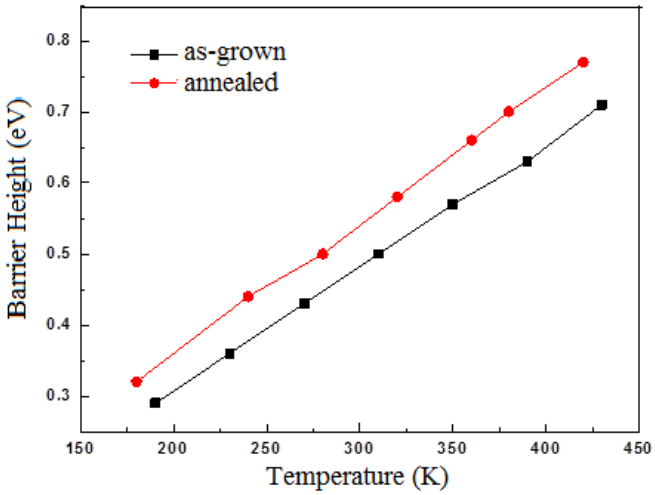


Fig.3 Temperature dependence of the experimental barrier height from I-V characteristics of as-grown and annealed samples

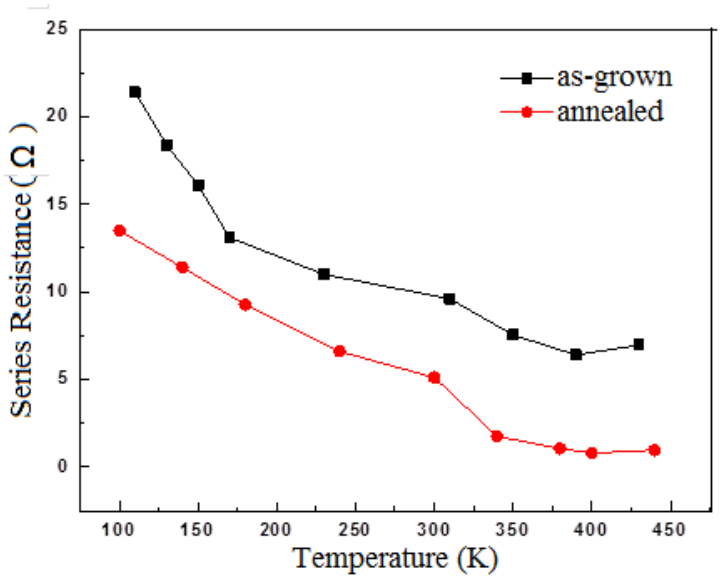


Fig.4 Temperature dependence of the experimental series resistance (Rs) from I-V characteristics of as-grown and annealed samples.

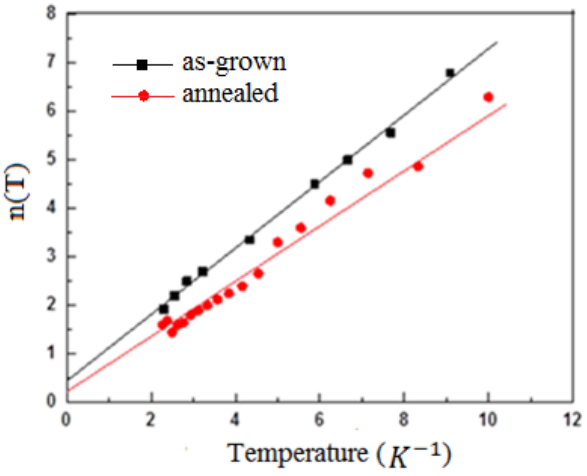


Fig.5 Experimental n(T) versus $\frac{1}{T}$ plot of as- grown and annealed samples.

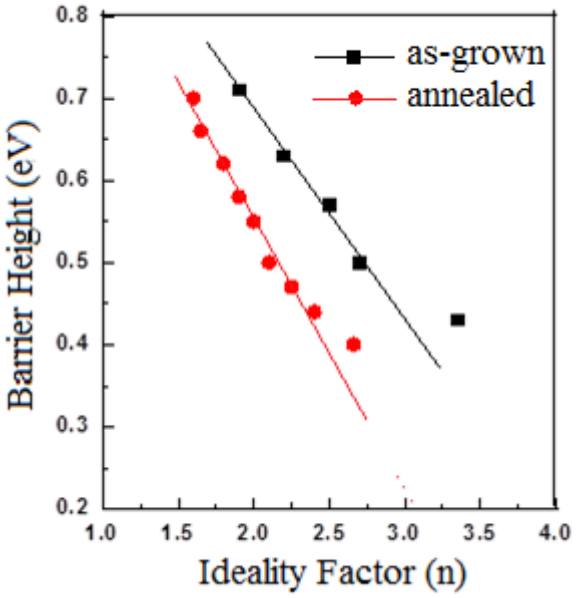


Fig.6 The barrier height (ϕ_b)values versus ideality factor (n) of as- grown and annealed samples.

3.2 Capacitance- voltage (C-V) characteristics of as-grown and annealed diodes

Figure. 7 shows the Capacitance -Voltage (C-V) characteristics of as-grown and annealed diodes which will be used to determine the net acceptor concentration in the p^-GaAsPN layer). The plot of $1/C^2$ vs V is a straight line for both diodes indicating that the doping is uniform throughout the measured region of p^-GaAsPN layer. The net acceptor concentration was calculated to be 1.18 $x10^{18}$ cm^{-3} and $2.11x10^{18}$ cm^{-3} for the as-grown and annealed GaAsPN layers, respectively. The annealed diodes exhibit higher values of free carrier concentration as compared with the as-grown samples. This increase in the net acceptor concentration could be attributed to a de-passivation of acceptors during thermal annealing[18].

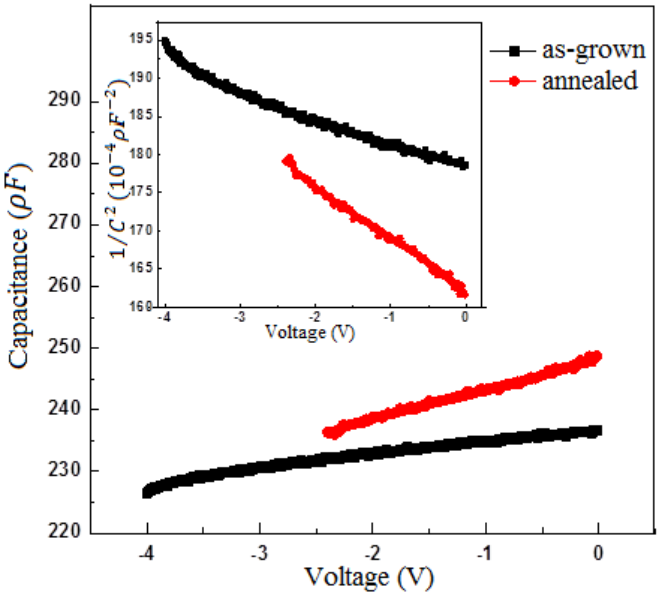


Fig.7 Plot of C-V characteristics and $^{1}/_{C^{2}}$ vs V plots for as-grown and annealed GaAsPN based diodes at room temperature (RT)..

3.3 Deep Level Transient Spectroscopy characteristics of as-grown and annealed diodes:

The DLTS measurements were performed to elaborate further on the role of rapid annealing on the electrically active defects in p-i-n GaAsPN based diodes. In addition, Laplace DLTS(LDLTS) was used to separate the DLTS signals due to defects with closely spaced energy levels. The DLTS spectra in the region close to the interface of the p-i-n junction are obtained by applying a small reverse bias of $V_r = -1V$, a rate window of 200Hz, a filling pulse $V_p = 0V$ and filling pulse duration $t_p = 1msec$. The samples were scanned from 10K to 450K.

The depletion width extend from 0.2µm from equilibrium condition (0V) to 0.63µm at reverse bias $V_R = -1V$. For clarify Figure.8 display the peaks detected in the temperature range (150K-450K). The annealed and as-grown samples exhibit three and two hole traps labeled as $H1_{an}$, $H2_{an}$ and $H3_{an}$ and $H4_{ag}$ and $H5_{ag}$, respectively. These are related to hole emitting defect states[40].

As seen in Figure 8, $H4_{ag}$ and $H1_{an}$ traps, which are detected in the temperature range (150K-230K) could have the same nature. Similarly, $H5_{ag}$ and $H3_{an}$ detected in the temperature range (320K-450K) could originate from the same defect. The $H2_{an}$ peak detected in the temperature range (250K-300K) in the annealed samples is absent in the as- grown samples.

High-resolution Laplace (DLTS) technique is used to analyze the DLTS peaks, which were obtained from DLTS measurements. The emission rates of carriers are given by [41]:

$$e_h = \left[\frac{\sigma_n < V_{th} > N_D}{g}\right] \exp\left\{\frac{\Delta E}{kT}\right\} \ldots\ldots\ldots\ldots (4)$$

where $< V_{th} >$ is the carrier average thermal velocity, N_D effective carrier density, k is Boltzmann constant and g is the trap degeneracy. Arrhenius plot gives the activation energy of the corresponding deep level. Emission rate signatures of each trap are plotted in Figure.9 Assuming that the capture cross section σ_n is temperature-independent, σ_n for each trap has also been calculated from the slope of the respective Arrhenius plots. The values of activation energies, capture cross-section and concentration of traps are given in Table.1.

Shallow and deep traps were observed in the annealed and the as- grown samples in the temperature range (150K- 450K) . $H3_{an}$ and $H5_{ag}$ deep traps have activation energies of 0.23eV and 0.25eV, respectively. These values are close to nitrogen- related hole trap with activation energy of 0.22eV that was reported by Abulfotuh *et al*[42]. Both samples exhibit shallow traps namely $H1_{an}$(0.06eV), $H2_{an}$(0.065eV) and $H4_{ag}$(0.07eV).

To the best of our knowledge, no deep level studies have been reported on MBE—grown GaAsPN/GaP. Therefore, we can only compare the results with those obtained for MBE—grown GaPN/GaP structures without As. It is worth pointing out that our layers contain a very low As composition. In a previous study, Rumyantsev et al[43] found two types of deep levels in lattice-mismatched GaPN/GaP heterostructures with activation energies and capture cross- sections of ($5.5x10^{-15}$, $4.8\ x10^{-18}cm^2$) and (0.17eV , 0.08eV). Incorporation of As atoms in to group V- sub-lattice compensates for elastic stresses emerging during epitaxial growth of the nitrogen containing layer. Generally, the annealed sample exhibits traps with activation energies lower than those in the as- grown diodes. It is important to point out that the capture cross-section and the trap concentrations decrease when the samples are annealed. In general, the concentration of traps increases with nitrogen content or any impurity associated with it due to more defects created that behave as deep level centers[44]. It was also demonstrated that the concentration of defects decreases with annealing temperature due to the decrease of these traps in GaAsPN quaternary alloys[45,46].

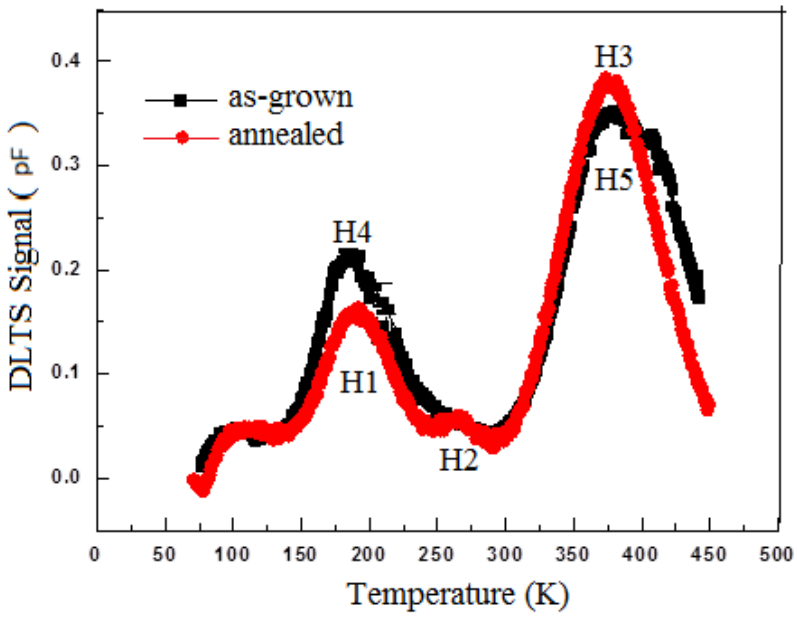


Fig.8 DLTS spectra for as-grown and annealed GaAsP-based diodes using a reverse bias of -1V, a rate window of 200Hz, a filling pulse V_p=0V and filling pulse duration is t_p=1msec.

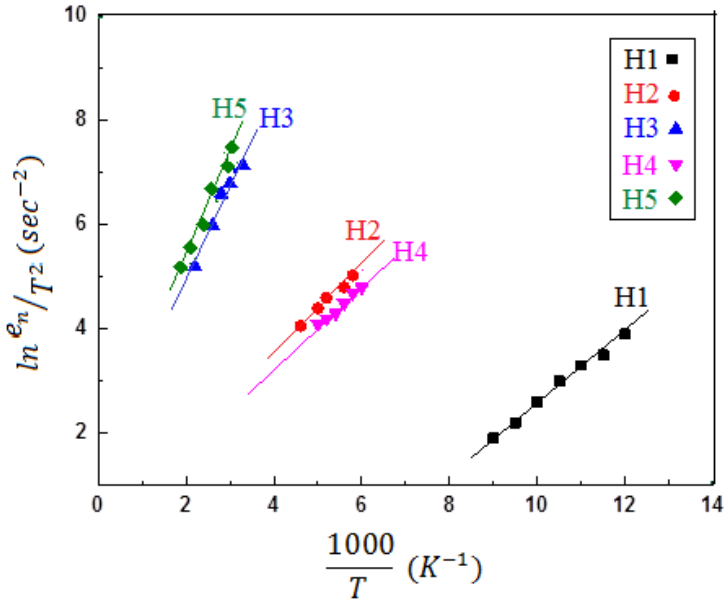


Fig.9 Arrhenius plots of the peak data extracted from DLTS of as-grown and annealed GaAsPN based diodes.

Table.1 Activation energies, capture cross-sections and concentration of traps observed in as-grown and rapid thermal annealed samples.

Trap Label	Activation Energy (eV)	Capture Cross-Section (cm^2)	Trap concentration (cm^{-3})
$H1_{an}$	(0.06 ± 0.01)	0.13×10^{-21}	2.4×10^{15}
$H2_{an}$	(0.07 ± 0.03)	0.1×10^{-21}	0.9×10^{15}
$H3_{an}$	(0.23 ± 0.07)	0.4×10^{-21}	3.5×10^{15}
$H4_{ag}$	(0.07 ± 0.02)	0.18×10^{-21}	2.7×10^{15}
$H5_{ag}$	(0.25 ± 0.05)	0.46×10^{-21}	7.2×10^{15}

4.Conclusion

In summary, I-V, C-V, DLTS and LDLTS were used to investigate the effect of rapid thermal annealing process on p-i-n GaAsPN based diodes grown by solid source MBE. Deep and shallow traps were detected in the annealed and as-grown samples. However, an additional trap was created after annealing. The improvement of the electrical properties of p-i-n GaAsPN based diodes with annealing process can be attributed to the decrease of the concentration and /or capture cross- section values of major defects measured by DLTS and Laplace DLTS.

Using thermionic theory, the calculated I-V barrier height and ideality factor values showed that the ideality factor increases and the barrier height decreases with decreasing temperature. The observed correlation between barrier height and ideality factor values of the diodes was explained by the lateral inhomogeneity of barrier height in these structures. Additionally, the annealed samples showed an ideality factor lower than the as-grown diodes and the barrier height increased after annealing process due to the effect of barrier in-homogeneities at the p-i-n interface. Using C-V characteristics , the net acceptor trap concentrations and turn on voltage were increased after rapid thermal annealing.

One can therefore conclude that rapid thermal annealing is an efficient treatment process to improve the electrical properties of devices.

Acknowledgments

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