On the Impedance and Stability Analysis of Dual-Active-Bridge-Based Input-Series Output-Parallel Converters

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***Abstract*—The power electronics are supposed to be popularized in the electrical grid to facilitate the integration of renewable energy units, leading to a cleaner and more efficient electrical power distribution system. In addition, the modularity feature of power electronics enables the potential of high voltage/current conversion ratio to replace the conventional transformer in grid. As more power electronics are going to be added into the system, the system stability can be a main concern due to the non-linear characteristic of power-electronic devices. Therefore, the stability-oriented modeling of power-electronic devices is always necessary for system integration. This paper investigates the impedance models of dual-active-bridge (DAB) based input-series output-parallel (ISOP) converters by considering the promising features of modular power electronics and the advantages of DAB converter. By applying the small-signal analysis methodology, the input impedance and output impedance of DAB-based ISOP converter are derived and validated in simulation and experiment. Based on the validated impedance models, the instability phenomenon can be accurately predicted at the source side and load side of converter respectively.**

***Index Terms*—Impedance modeling, stability analysis, dual-active-bridge, input-series output-parallel converter.**

I. Introduction

DUE to the fast consumption of the finite conventional energies, the installation and utilization of renewable energy systems are increasing continuously worldwide. In an integrated system with a variety types of energy producers, consumers and storage units, the power electronics become a necessary part that are interfaced with these units to achieve power conversion, regulation and harmonic suppression [1]–[3]. With the power semiconductors (active components) and energy storage components (passive components), different power converter topologies can be designed referring to the application scenario. The power converters can be further integrated together to enable more functionalities and higher efficiency. For instance, the back-to-back converter which consists of two dc-ac converters sharing the same dc-link, is commonly applied in wind power systems and other ac systems [4], [5]; The dual-active-bridge (DAB) converter containing two dc-ac converters with a high frequency transformer is supposed to be used for the charging station for electric vehicles and other kinds of microgrids to interlink the dc buses. Compared to other mainstream dc-dc topologies, the DAB converter takes advantages of high power density, galvanic isolation, soft switching and bidirectional power flow [6], [7]; The solid-state transformer or smart transformer formed by two dc-ac converters and a dc-dc converter was proposed to replace the conventional 50/60 Hz transformer which links medium-voltage (MV) stages and low-voltage (LV) ac stages in the future electrical grid [8], [9]. When the voltage conversion ratio is high, the modularization of converters becomes a popular way to cope with the problem of high voltage stress on the power semiconductors [10], [11]. With this consideration, the multilevel converter was proposed, which has the series-connected submodules on the arms and has benefits of high quality output voltage and current, high modularity and low stresses of switches [12]. Another feasible topology is the converter whose submodules are connected in series/parallel, e.g. input-series output-parallel (ISOP) converters [13].

As more power electronics are installed into the electrical power distribution systems, the system structure becomes more flexible and complex. Regarding the non-linear characteristic of power electronics, the system stability becomes one main concern during system integration, especially with the presence of constant power loads (CPL) which can easily introduce right-hand plane poles [14]. Hence, the modeling of power electronics is always necessary which can be the indicator of stability. The converter impedance-based stability analysis is one of the most popular small-signal approaches preferred by researchers and system designers considering it only requires magnitude and phase information of converter impedance at the operating point. For the stability criteria of the impedance analysis approach, the Nyquist Criterion was proposed first as a sufficient and necessary condition by checking if the minor loop gain (MLG) encircles (-1, 0) in complex plane [15]. Based on that, several criteria were proposed such as Middlebrook Criterion, Gain Margin and Phase Margin Criterion and Passivity-based Criterion which are sufficient condition to system stability [16]–[18]. However, these criteria are applicable for the dc or single-input single-output (SISO) systems only. To analyze the stability of ac systems and other multivariable systems which are multi-input multi-output (MIMO) systems, the Generalized Nyquist Criterion (GNC) was proposed that the system will be unstable if at least one of characteristic loci of the MLG matrix encircles (-1, 0) [19]. The theory of converter impedance modeling and stability analysis has been successfully implemented in existing literature, such as [20]–[25].

Although the modular power electronics are attractive with the aforementioned benefits, the addition of multiple sub-modules makes the converter model more complex as well

as the stability analysis. The impedance models of modular multilevel converters have been investigated in [26]–[28], by contrast, the impedance models of converters where the submodules connected in series/parallel are rarely discussed in existing literature. To fill the blank and regarding the promising features of DAB converter, this paper explores the impedance modeling of DAB-based ISOP converter. With the revealed impedance models, the stability analysis at the converter input and output are carried out. The content is organized as follows. Section II proposes the impedance models of closed-loop controlled DAB-based ISOP converters. Section III validates the impedance models with switching model in simulation. Section IV analyzes the system stability based on the proposed impedance models. Section V presents the experimental results of impedance-based stability analysis. Section VI draws the conclusions.

II. Impedance Modeling of DAB-based ISOP Converter

In this section, the impedance models of DAB-based ISOP converter are derived. Before that, it can be better to start with the impedance of a single DAB converter. Fig. 1 shows the schematic of DAB converter, where the single-phase shift modulation and output voltage control (OVC) are adopted to facilitate the derivation. Assuming the power is transferred to the load, the power equation is given as (1) and the small signal gains can be obtained as (2). Fig. 2 shows the transfer function block scheme of the DAB converter with the resistive load and OVC. With the transfer function block scheme, the input impedance of DAB converter can be obtained, which has been validated with the switching model simulation in [23].

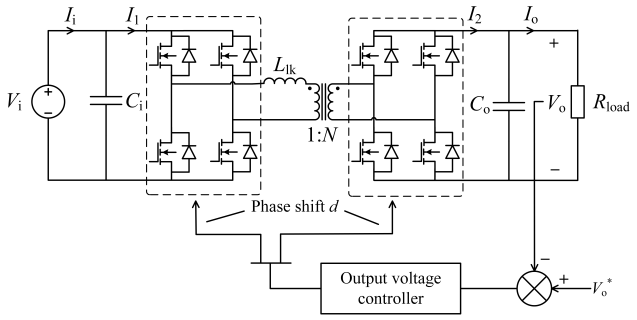


Fig. 1. The schematic of a DAB converter

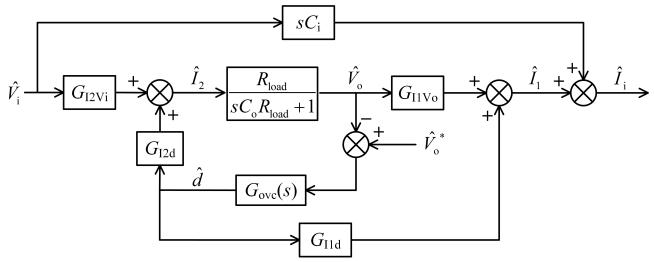


Fig. 2. The transfer function block scheme for the input impedance of DAB converter

$$P = \frac{V_\mathrm{i} V_\mathrm{o}}{2N f_\mathrm{s} L_\mathrm{lk}} d(1-d) \tag{1}$$

$$\begin{aligned} G_\mathrm{I1Vo} &= \frac{1}{2N f_\mathrm{s} L_\mathrm{lk}} d(1-d), G_\mathrm{I1d} = \frac{V_\mathrm{o}}{2N f_\mathrm{s} L_\mathrm{lk}} (1-2d) \\ G_\mathrm{I2Vi} &= \frac{1}{2N f_\mathrm{s} L_\mathrm{lk}} d(1-d), G_\mathrm{I2d} = \frac{V_\mathrm{i}}{2N f_\mathrm{s} L_\mathrm{lk}} (1-2d) \end{aligned} \tag{2}$$

A. Input Impedance Modeling

When it comes to the DAB-based ISOP converter, the power equation of each DAB submodule still holds. Fig. 3 shows the schematic of the DAB-based ISOP converter. Assume there are n DAB submodules inside the ISOP converter, the power of each DAB submodule is given as

$$P_j = \frac{V_{\mathrm{i},j} V_{\mathrm{o},j}}{2N_j f_{\mathrm{s},j} L_{\mathrm{lk},j}} d_j(1-d_j),\ j = 1,2,...,n \tag{3}$$

On the other hand, because of IS structure, the dynamics of input voltage are distributed to the input capacitor of DAB submodules. It is noted that the dynamics can be unevenly distributed due to the different value of input capacitors and different power transfer of DAB submodules, which leads to the unbalanced input voltage of each DAB submodule, and the control could fail as the input voltage diverges. To overcome this issue, the input voltage balancing control (IVBC) of ISOP converter was proposed in [13], [29], [30]. With the IVBC, the input voltage of each submodule is supposed to be same and constant at the steady state, and the mean value of current going through the input capacitors is zero. Hence, the input current of each submodule is same due to the cascaded structure of input terminals, leading to equal power transfer of each submodule. At the same time, the output current sharing is automatically achieved due to the same output voltage of

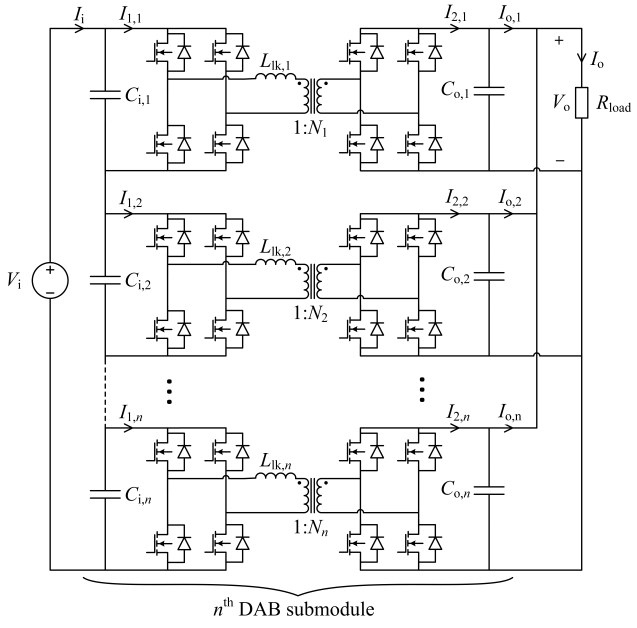


Fig. 3. The schematic of the DAB-based ISOP converter

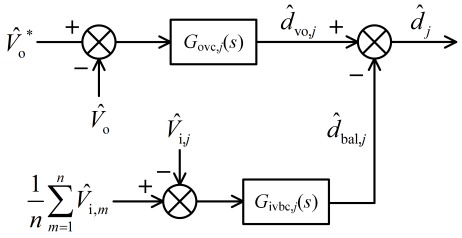


Fig. 4. The simplified control structure of each DAB submodule

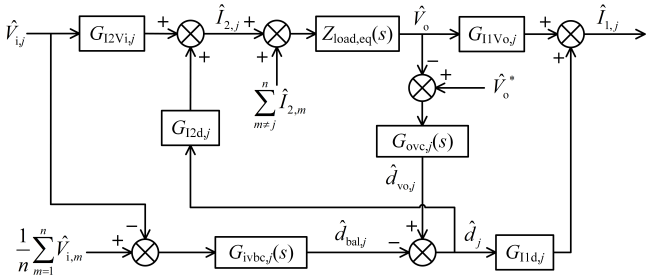


Fig. 5. The transfer function block scheme of DAB submodule j

each submodule considering the parallel structure of output terminals. In the grid application, the input voltage balancing control can be applied by the front-end converter such as the cascaded H-bridge converter, or the ISOP converter itself. By comparison, the input voltage balancing implemented by the ISOP converter can benefit the design of dc smart distribution system [31]. Hence, in this paper, the input voltage balancing control is included in the ISOP converter. Fig. 4 shows the simplified control structure of each DAB submodule, where the reference voltage of IVBC in small signal is given as

$$\hat{V}_{\mathrm{ivbc}}^{*}=\frac{1}{n}\hat{V}_{\mathrm{i}}=\frac{1}{n}\sum_{m=1}^{n}\hat{V}_{\mathrm{i},m} \tag{4}$$

With the addition of IVBC, the input capacitors can be actively charged/discharged by referring to the voltage dynamics on them. Assuming the controllers are classical PI structure, the transfer function of $G_{\mathrm{ovc}}(s)$ and $G_{\mathrm{ivbc}}(s)$ are given as

$$G_{\mathrm{ovc}}\left(s\right)=(k_{\mathrm{p,ovc}}+\frac{k_{\mathrm{i,ovc}}}{s})G_{\mathrm{zoh}}(s) \tag{5}$$

$$G_{\mathrm{ivbc}}\left(s\right)=(k_{\mathrm{p,ivbc}}+\frac{k_{\mathrm{i,ivbc}}}{s})G_{\mathrm{zoh}}(s) \tag{6}$$

where $k_{\mathrm{p,ovc}}$ and $k_{\mathrm{i,ovc}}$ are the PI parameters of OVC, $k_{\mathrm{p,ivbc}}$ and $k_{\mathrm{i,ivbc}}$ are the PI parameters of IVBC, $G_{\mathrm{zoh}}(s)$ is the zero-order hold (ZOH) in continuous form, given as

$$G_{\mathrm{zoh}}(s)=\frac{1-e^{-T_{\mathrm{s}}s}}{T_{\mathrm{s}}s} \tag{7}$$

where T_{s} is the sampling time. To make the following analysis less complex as well as to mitigate the influence of discretization, only one ZOH module with sampling time of one switching period is added into the feedback control path to represent the digital pulse width modulation process. Considering the cases with unequal input capacitors and the dynamics of each DAB submodule interacts other DAB submodules, the input impedance of DAB-based ISOP converter cannot be directly obtained from the impedance model of a single DAB converter. Also, considering the DAB submodules share the output current, the coupling effect among the output current of each DAB submodule cannot be neglected. These all factors make the impedance modeling of ISOP converter more challenging. According to the practical experience of hardware design, the dc link capacitors are usually integrated with H-bridges. Hence, each submodule is equipped with the output capacitor individually which is shown in Fig. 3, and the equivalent RC load needs to be worked out considering the coupling effect among the output current of each DAB submodule. For the sake of simplicity, the intrinsic properties of components such as the equivalent series resistance (ESR) are neglected in the derivation process. The dynamics in load current can be given as

$$\hat{I}_{\mathrm{o}}=\sum_{m=1}^{n}\hat{I}_{\mathrm{o},m}=\frac{\hat{V}_{\mathrm{o}}}{R_{\mathrm{load}}},\ m=1,2,...,n \tag{8}$$

The output current provided by each submodule is given as

$$\hat{I}_{2,m}=\hat{I}_{\mathrm{o},m}+sC_{\mathrm{o},m}\hat{V}_{\mathrm{o}} \tag{9}$$

Based on (8) and (9), the equivalent RC load at output terminal can be given as

$$Z_{\mathrm{load,eq}}(s)=\frac{\hat{V}_{\mathrm{o}}}{\sum_{m=1}^{n}\hat{I}_{2,m}}=\frac{R_{\mathrm{load}}}{R_{\mathrm{load}}\sum_{m=1}^{n}sC_{\mathrm{o},m}+1} \tag{10}$$

On the other side, according to Fig. 4, the IVBC links the dynamics of input voltage to phase shift. The output of IVBC of submodule j can be represented by the input voltage of each DAB submodule, given as

$$\hat{d}_{\mathrm{bal},j}=G_{\mathrm{ivbc},j}(s)(\frac{1}{n}\sum_{m=1}^{n}\hat{V}_{\mathrm{i},m}-\hat{V}_{\mathrm{i},j}) \tag{11}$$

By considering all these factors, the transfer function block scheme of DAB submodule j with the load, OVC and IVBC can be simplified as Fig. 5. The gain of sum of current output by the lagging H-bridges $\hat{I}_2$ to the output of OVC $\hat{d}_{\mathrm{vo},j}$ can be calculated as

$$A_j=\frac{\hat{d}_{\mathrm{vo},j}}{\sum_{m=1}^{n}\hat{I}_{2,m}}=-G_{\mathrm{ovc},j}(s)Z_{\mathrm{load,eq}}(s) \tag{12}$$

The equation of the loop closed by input voltage $\hat{V}_{\mathrm{i},j}$, output of IVBC $\hat{d}_{\mathrm{bal},j}$ and $\hat{I}_2$ can be obtained as

$$G_{\mathrm{I2Vi},j}\hat{V}_{\mathrm{i},j}-G_{\mathrm{I2d},j}\hat{d}_{\mathrm{bal},j}=\hat{I}_{2,j}-G_{\mathrm{I2d},j}A_j\sum_{m=1}^{n}\hat{I}_{2,m} \tag{13}$$

The input current of the j^{th} leading H-bridge $\hat{I}_{1,j}$ can be represented by $\hat{I}_2$ and $\hat{d}_{\mathrm{bal},j}$, which can be written as

$$\hat{I}_{1,j}=(B_j+G_{\mathrm{I1d},j}A_j)\sum_{m=1}^{n}\hat{I}_{2,m}-G_{\mathrm{I1d},j}\hat{d}_{\mathrm{bal},j} \tag{14}$$

where

$$B_j=G_{\mathrm{I1Vo},j}Z_{\mathrm{load,eq}}(s) \tag{15}$$

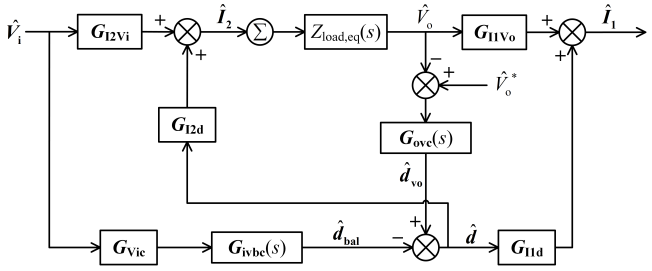


Fig. 6. The transfer function block scheme for the input impedance of DAB-based ISOP converter

Since all DAB submodules have same control structure, the equations (11), (13) and (14) can be generalized to the whole system, shown as

$$\begin{cases} \hat{\boldsymbol{d}}_{\mathbf{bal}} = \boldsymbol{G}_{\mathbf{ivbc}}(s)\boldsymbol{G}_{\mathbf{Vic}}\hat{\boldsymbol{V}}_{\mathbf{i}} \\ \boldsymbol{G}_{\mathbf{I2Vi}}\hat{\boldsymbol{V}}_{\mathbf{i}} - \boldsymbol{G}_{\mathbf{I2d}}\hat{\boldsymbol{d}}_{\mathbf{bal}} = \boldsymbol{G}_{\mathbf{I2c}}\hat{\boldsymbol{I}}_{\mathbf{2}} \\ \hat{\boldsymbol{I}}_{\mathbf{1}} = \boldsymbol{G}_{\mathbf{I1I2}}\hat{\boldsymbol{I}}_{\mathbf{2}} - \boldsymbol{G}_{\mathbf{I1d}}\hat{\boldsymbol{d}}_{\mathbf{bal}} \end{cases} \tag{16}$$

The bold symbols in the above equations represent the vectors/matrices of small signal variations and gains. $\hat{\boldsymbol{d}}_{\mathbf{bal}}$ is the vector of IVBC output. $\boldsymbol{G}_{\mathbf{ivbc}}(s)$ is the diagonal matrix of controller transfer functions of IVBC. $\hat{\boldsymbol{V}}_{\mathbf{i}}$ is the vector of input voltage of submodules, $\hat{\boldsymbol{I}}_{\mathbf{1}}$ and $\hat{\boldsymbol{I}}_{\mathbf{2}}$ are the vectors of input current of leading H-bridges and output current of lagging H-bridges. $\boldsymbol{G}_{\mathbf{Vic}}$ is the correction factor matrix of $\hat{\boldsymbol{V}}_{\mathbf{i}}$ as input of IVBC. $\boldsymbol{G}_{\mathbf{I2c}}$ is the gain matrix of $\hat{\boldsymbol{I}}_{\mathbf{2}}$ as output of the closed loop of input voltage to output current. $\boldsymbol{G}_{\mathbf{I1I2}}$ is the transfer function matrix of output current to input current. $\boldsymbol{G}_{\mathbf{I1d}}$, $\boldsymbol{G}_{\mathbf{I2d}}$ and $\boldsymbol{G}_{\mathbf{I2Vi}}$ are the diagonal matrices of small signal gains in (2) respectively. Their details can be found in Appendix A. With the generalized equations, the transfer function block scheme for the input impedance of DAB-based ISOP converter can be figured out, shown in Fig. 6. Elimination of $\hat{\boldsymbol{d}}_{\mathbf{bal}}$ by combining the generalized equations in (16) returns the input admittance matrix of DAB submodules excluding the input capacitors, which shows the multi-input multi-output (MIMO) characteristic, given as

$$\hat{\boldsymbol{I}}_{\mathbf{1}} = \boldsymbol{Y}_{\mathbf{i,DABsub}}(s)\hat{\boldsymbol{V}}_{\mathbf{i}} \tag{17}$$

where

$$\begin{aligned} \boldsymbol{Y}_{\mathbf{i,DABsub}}(s) =& \boldsymbol{G}_{\mathbf{I1I2}}\boldsymbol{G}_{\mathbf{I2c}}{}^{-1}\left(\boldsymbol{G}_{\mathbf{I2Vi}} - \boldsymbol{G}_{\mathbf{I2d}}\boldsymbol{G}_{\mathbf{ivbc}}(s)\boldsymbol{G}_{\mathbf{Vic}}\right) \\ & - \boldsymbol{G}_{\mathbf{I1d}}\boldsymbol{G}_{\mathbf{ivbc}}(s)\boldsymbol{G}_{\mathbf{Vic}} \end{aligned} \tag{18}$$

Based on the input admittance matrix and consider the input capacitors, the input impedance matrix of DAB submodules can be obtained as

$$\hat{\boldsymbol{V}}_{\mathbf{i}} = \boldsymbol{Z}_{\mathbf{i,MIMO}}(s)\hat{\boldsymbol{I}}_{\mathbf{i}} \tag{19}$$

where

$$\boldsymbol{Z}_{\mathbf{i,MIMO}}(s) = \left(\boldsymbol{Y}_{\mathbf{i,DABsub}}(s) + s\boldsymbol{C}_{\mathbf{i}}\right)^{-1} \tag{20}$$

Note that $\boldsymbol{C}_{\mathbf{i}}$ here is the diagonal matrix of input capacitors of each DAB submodules which are given in Appendix A.

Considering the input terminal of each DAB submodule is connected in series, the MIMO chacacteristic of input impedance can be transformed to single-input multi-output (SIMO) characteristic regarding the input impedance of each DAB submodule, shown as Fig. 7. It can be seen from the view of the input terminal of ISOP converter all submodules are cascaded together, meaning that the source current going through each submodule is same. The input impedance matrix obtained in (20) can be assumed as

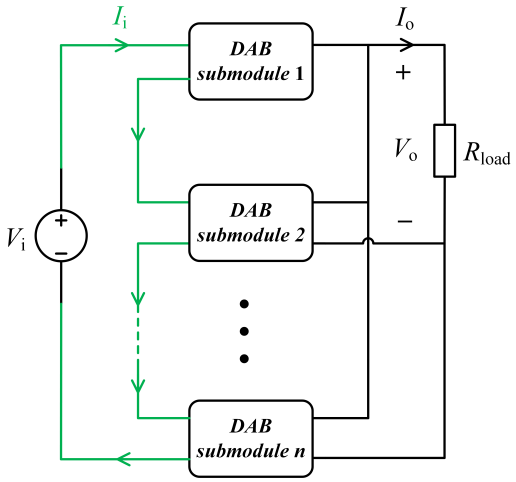


Fig. 7. The simplified schematic of ISOP converter represented by 'units'

$$\boldsymbol{Z}_{\mathbf{i,MIMO}}(s) = \begin{bmatrix} Z_{\mathrm{i},11}(s) & Z_{\mathrm{i},12}(s) & \cdots & Z_{\mathrm{i},1n}(s) \\ Z_{\mathrm{i},21}(s) & Z_{\mathrm{i},22}(s) & \cdots & Z_{\mathrm{i},2n}(s) \\ \vdots & \vdots & \ddots & \vdots \\ Z_{\mathrm{i},n1}(s) & Z_{\mathrm{i},n2}(s) & \cdots & Z_{\mathrm{i},nn}(s) \end{bmatrix} \tag{21}$$

According to the simplified structure of submodules shown in Fig. 7, the elements in source current vector I_i are equal, and the input impedance matrix $\boldsymbol{Z}_{\mathbf{i,MIMO}}(s)$ can be further simplified to the SIMO form, given as

$$\boldsymbol{Z}_{\mathbf{i,SIMO}}(s) = \frac{\hat{\boldsymbol{V}}_{\mathbf{i}}}{\hat{I}_{\mathrm{i}}} = \sum_{m=1}^{n} \begin{bmatrix} Z_{\mathrm{i},1m}(s) \\ Z_{\mathrm{i},2m}(s) \\ \vdots \\ Z_{\mathrm{i},nm}(s) \end{bmatrix} = \begin{bmatrix} Z_{\mathrm{i},1}(s) \\ Z_{\mathrm{i},2}(s) \\ \vdots \\ Z_{\mathrm{i},n}(s) \end{bmatrix} \tag{22}$$

where

$$\hat{I}_{\mathrm{i}} = \hat{I}_{\mathrm{i},1} = \hat{I}_{\mathrm{i},2} = ... = \hat{I}_{\mathrm{i,n}} \tag{23}$$

Furthermore, the cascaded structure at the input terminal of ISOP converter also enables the SISO characteristic. By summing all elements of $\boldsymbol{Z}_{\mathbf{i,SIMO}}(s)$ in (22), the input impedance of ISOP converter can be represented as

$$\boldsymbol{Z}_{\mathbf{i,SISO}}(s) = \frac{\hat{V}_{\mathrm{i}}}{\hat{I}_{\mathrm{i}}} = \sum_{k=1}^{n}\sum_{m=1}^{n} Z_{\mathrm{i},km}(s) \tag{24}$$

where

$$\hat{V}_{\mathrm{i}} = \sum_{m=1}^{n} \hat{V}_{\mathrm{i},m} \tag{25}$$

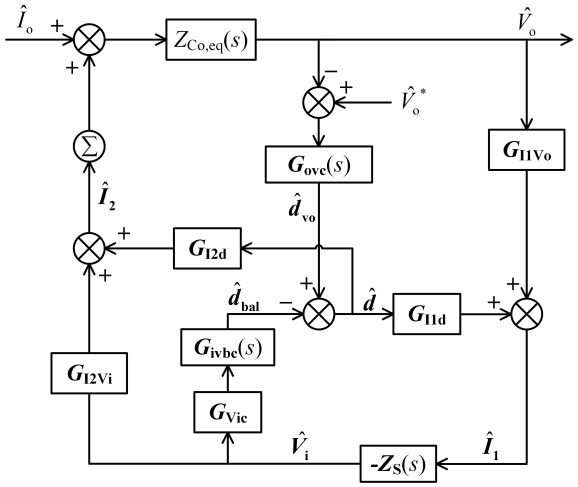


Fig. 8. The transfer function block scheme for the output impedance of DAB-based ISOP converter

B. Output Impedance Modeling

Since the output terminal of DAB submodules are parallelly connected, the output impedance of ISOP converter features the SISO characteristic. By transforming Fig. 6, the transfer function block scheme for output impedance of DAB-based ISOP converter can be obtained as Fig. 8, where $Z_{\mathrm{Co,eq}}(s)$ is the total impedance of output capacitors, given as

$$Z_{\mathrm{Co,eq}}(s) = \frac{1}{\sum_{m=1}^{n} \mathrm{sC}_{\mathrm{o},m}} \tag{26}$$

And $\boldsymbol{Z}_{\mathbf{S}}(s)$ is the equivalent source impedance in MIMO form, given as

$$\boldsymbol{Z}_{\mathbf{S}}(s) = \left[s\boldsymbol{C}_{\mathbf{i}} + \frac{1}{Z_{\mathrm{S}}(s)} \begin{bmatrix} 1 & 1 & \cdots & 1 \\ 1 & 1 & \cdots & 1 \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & \cdots & 1 \end{bmatrix} \right]^{-1} \tag{27}$$

where $Z_{\mathrm{S}}(s)$ is the impedance of input voltage source. Referring to the general rule for system-level design, the magnitude of source impedance is supposed to be designed as small as possible to acquire a larger gain margin. Meanwhile, by observing transfer function block scheme in Fig. 8, one conclusion is that the output voltage of ISOP converter can hardly affect its input voltage if the magnitude of source impedance is very low. This indicates the transfer function block scheme can be significantly simplified by neglecting the paths including $\boldsymbol{Z}_{\mathbf{S}}(s)$, which has been revealed in [32]. With this consideration, the simplified transfer function block scheme is shown in Fig. 9, from where the output impedance of ISOP converter can be derived as

$$Z_{\mathrm{o,ISOP}}(s) = \frac{1}{\sum_{m=1}^{n} G_{\mathrm{I2d},m} G_{\mathrm{ovc},m}(s) + \sum_{m=1}^{n} sC_{\mathrm{o},m}} \tag{28}$$

III. Impedance Model Validation

In this section, the input impedance and output impedance of DAB-based ISOP converter derived in previous section are validated with the switching model in PLECS. Before the validation, feasible feasible simulation parameters are given as Table I, and the converter containing two submodules is considered for facilitating the following analysis.

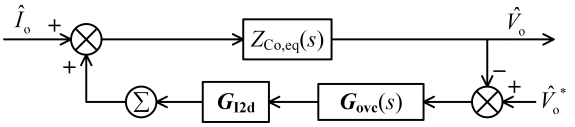


Fig. 9. The simplified transfer function block scheme for the output impedance of DAB-based ISOP converter

TABLE I
Simulation Parameters of Submodule j

Symbol	Definition	Value
$V_{\mathrm{i},j}$	Input voltage	750 V
V_{o}	Output voltage	750 V
N_j	Turn ratio of transformer	1
$L_{\mathrm{lk},j}$	Leakage inductance	10 μH
$f_{\mathrm{s},j}$	Switching frequency	50 kHz
$k_{\mathrm{p,ovc},j}$	Proportional gain of OVC	0.001
$k_{\mathrm{i,ovc},j}$	Integral gain of OVC	10
$k_{\mathrm{p,ivbc},j}$	Proportional gain of IVBC	0.001
$k_{\mathrm{i,ivbc},j}$	Integral gain of IVBC	2
$C_{\mathrm{i},j}$	Input capacitor	1 mF
$C_{\mathrm{o},j}$	Output capacitor	0.5 mF

A. Input Impedance Validation

To validate the input impedance model of a dc system, a general way is adding the AC sinusoidal voltage with specific frequency into the dc voltage source. By capturing the input voltage and current of the converter switching model, the input impedance can be calculated and compared with the proposed model. Since it is mentioned in the previous section that the input impedance of DAB-based ISOP converter can show SISO and SIMO characteristics, both characteristics of input impedance can be validated. Fig. 10 shows the input impedance of DAB-based ISOP converter with SISO characteristic in Bode diagram. It can be seen that the proposed model is consistent with the simulation results, where the input impedance behaves as CPL at low frequencies and behaves as capacitor at high frequencies.

Considering the SISO input impedance model is transformed from the MIMO form, the MIMO characteristic is inherited thereby. Hence, the proposed SISO input impedance model remains valid for the cases of DAB submodules with different parameters. On the other hand, it is worth mentioning that the input impedance model can be different when there are deviations between the input capacitors. Fig. 11 shows the Bode diagram of SISO input impedance when $C_{\mathrm{i},1}$ is 1.5 mF and $C_{\mathrm{i},2}$ is 0.75 mF, where the total equivalent input capacitance keeps same if the converter is ignored. It can be seen that the deviations of input capacitors introduce a

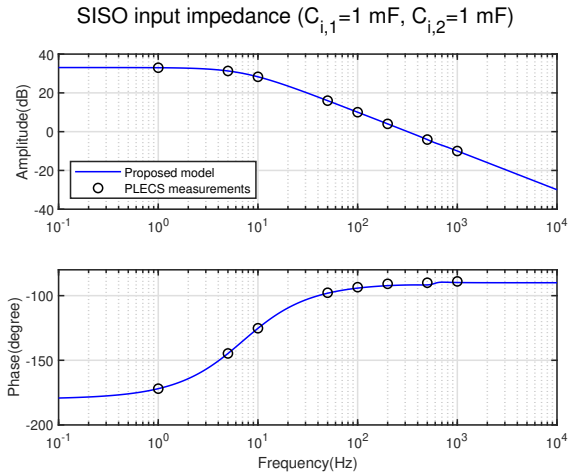


Fig. 10. The SISO input impedance of DAB-based ISOP converter

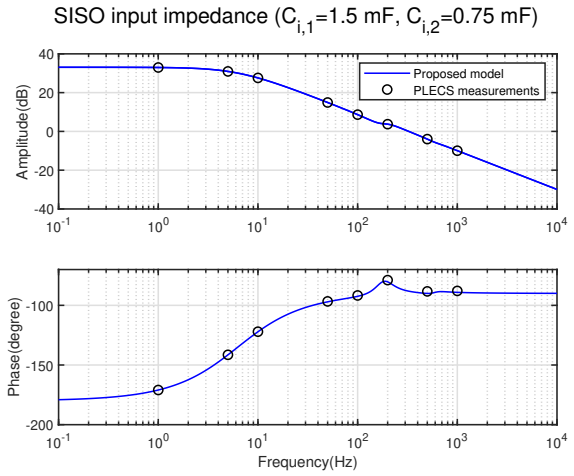


Fig. 11. The SISO input impedance of DAB-based ISOP converter with different value of input capacitors

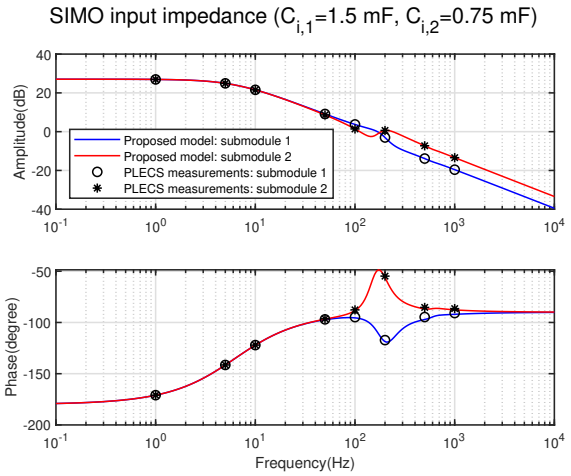


Fig. 12. The SIMO input impedance of DAB-based ISOP converter with different value of input capacitors

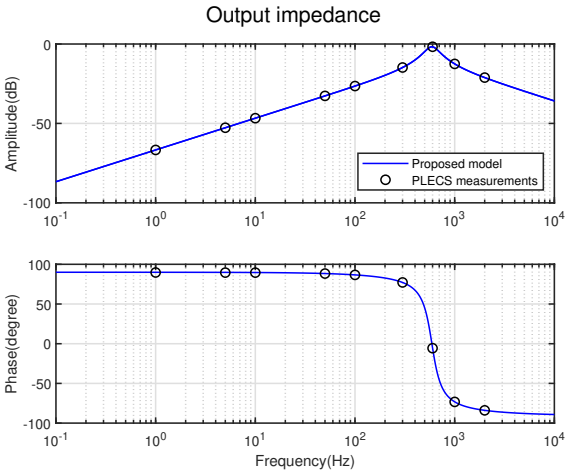


Fig. 13. The output impedance of ISOP converter

different behavior at high frequencies, which can be attributed to the coupling effect between submodules. The proposed model can be used in SIMO form to check the dynamics at the input terminal of each submodule individually, especially when the input capacitors are unequal. Fig. 12 shows the input impedance of submodules when input capacitors $C_{\mathrm{i},1}$ and $C_{\mathrm{i},2}$ are 1.5 mF and 0.75 mF. It can be seen the proposed model is also well matched with simulation results, proving the validity of the proposed model.

B. Output Impedance Validation

Different from the validation of input impedance model, the validation of output impedance model requires to add an ideal AC sinusoidal current source at the output terminal of converter switching model, meanwhile the output voltage and current are monitored to calculate the output impedance and compared with the proposed model. Since the output of the submodules are connected in parallel, the output impedance of ISOP converter exhibits SISO characteristic. Fig. 13 shows the output impedance of DAB-based ISOP converter with load power of 50 kW. It can be easily observed that the output impedance has inductive behavior at low frequencies and has capacitive behavior at high frequencies. Also, a good match is presented by comparing the proposed simplified model and simulation measurements.

IV. Stability Analysis

In this section, a comprehensive stability analysis of DAB-based ISOP converter is carried out at both source side and load side with the simulation parameters in Table I.

A. Source Side Stability

It has been proved in the previous section that the input impedance model of DAB-based ISOP converter can exhibit MIMO and SISO characteristic. Therefore, the source side stability of DAB-based ISOP converter can be analyzed by either MIMO form or SISO form. In this subsection, stability analysis is carried out in both forms to show their equivalence. The source impedance is assumed to be a simple RL circuit. Fig. 14 shows the Nyquist plot of MLG with different source

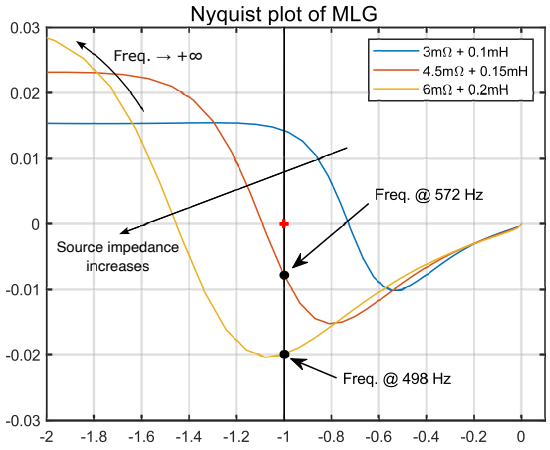


Fig. 14. The Nyquist plot of MLG with different source impedance

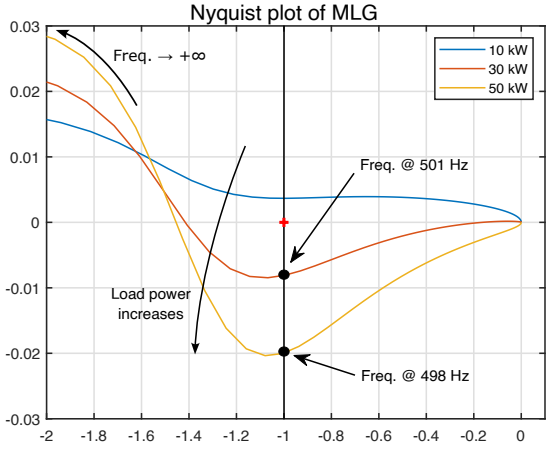


Fig. 15. The Nyquist plot of MLG with different load power

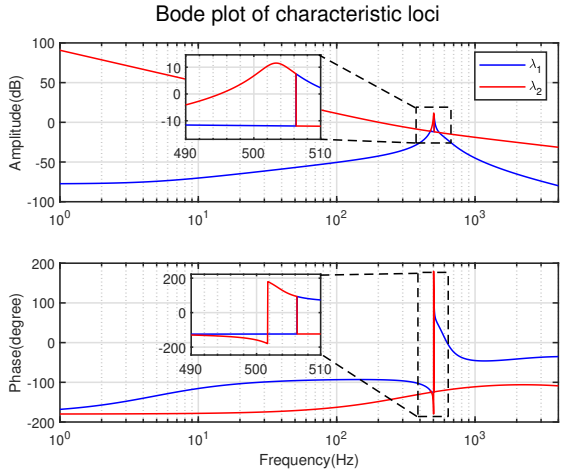


Fig. 16. The Bode diagram of characteristic loci of MLG matrix

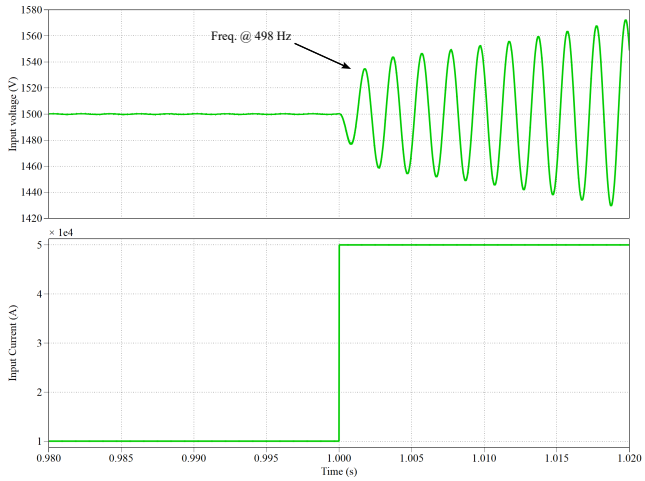


Fig. 17. The simulation waveforms for the input voltage and load power of DAB-based ISOP converter

impedance in SISO form, where the RL circuit is regarded as the source subsystem while the DAB-based ISOP converter including the input capacitors is regarded as the load subsystem. It can be seen that the system tends to instability as the source impedance increases, and the instability happens when the source impedance is either 4.5 mΩ + 0.15 mH or 6 mΩ + 0.2 mH, with oscillating frequency of 572 Hz and 498 Hz respectively. In addition, the influence of load power on system stability is carried out. Fig. 15 shows the Nyquist plot of MLG with different load power when the source impedance is fixed as 6 mΩ + 0.2 μH. It can be seen the Nyquist contour does not encircle (-1, 0) at load power of 10 kW, indicating the system will remain stable. Once the load power increases, the Nyquist contour start to encircle (-1, 0), indicating the system tends to instability.

As for the stability analysis in MIMO form, the RL circuit and the input capacitors of DAB-based ISOP converter are grouped together to be the source subsystem which is already been given in (27), and the rest of DAB-based ISOP converter becomes the load subsystem. To analyze the stability in a clearer way, the characteristic loci of the MLG matrix are represented in Bode diagram instead of Nyquist plot, shown in Fig. 16 where the source impedance is 6 mΩ + 0.2 mH and the load power is 50 kW. It can be seen that for λ_2 the amplitude at phase crossover frequency is larger than 0 dB, indicating that λ_2 encircles (-1, 0) which means system will be instable. In addition, the gain crossover frequency of λ_2 is exactly the oscillation frequency during instability. Fig. 17 shows the simulation waveforms for the input voltage and load power of converter. The instability in the input voltage with oscillating frequency of 498 Hz can be observed when load power is stepped up to 50 kW at $t = 1$ s, showing a good match with the predicted results.

B. Load Side Stability

By observing the output impedance of DAB-based ISOP converter shown in Fig. 13, it can be known the peak of amplitude can most easily challenge the system stability with lower gain margin, which is actually located at the resonant frequency. The resonant frequency can be approximated

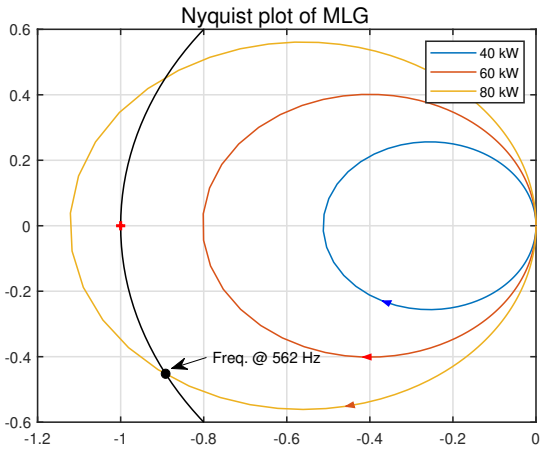


Fig. 18. The Nyquist plot of MLG with different load power

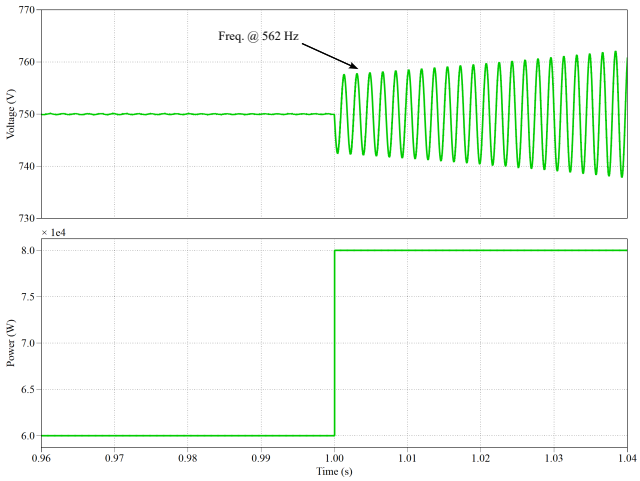


Fig. 19. The simulation waveforms for the output voltage and load power of DAB-based ISOP converter

through (28), given as

$$\omega_{\text{res}} \approx \sqrt{\frac{\sum_{m=1}^{n} G_{\text{I2d},m} k_{\text{i,ovc},m}}{\sum_{m=1}^{n} C_{\text{o},m}}} \tag{29}$$

By observing the equation above, it can be known that the resonant frequency is mainly affected by the small signal gain G_{I2d}, the integral coefficient of OVC and the output capacitance. With the obtained resonant frequency, the peak of amplitude can be approximated as

$$|Z_{\text{o,ISOP}}(s)|_{s=j\omega_{\text{res}}}| \approx \frac{1}{\sum_{m=1}^{n} G_{\text{I2d},m} k_{\text{p,ovc},m}} \tag{30}$$

where an inference can be obtained that the peak of amplitude is influenced by the small signal gain G_{I2d} and the proportional coefficient of OVC. However, the approximations in (29) and (30) will be less accurate as frequency and peak amplitude increase respectively, due to the existence of discrete modules in the control path [32]. To find the instability at the load side of DAB-based ISOP converter, an ideal constant power load is added to the output of converter in simulation

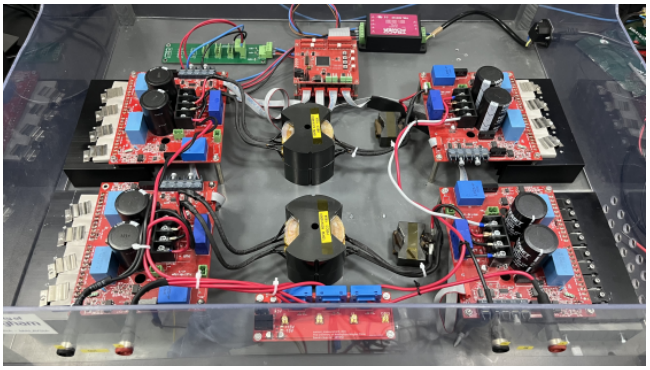


Fig. 20. The experimental setup of DAB-based ISOP converter

TABLE II
EXPERIMENTAL PARAMETERS OF SUBMODULE j

Symbol	Definition	Value
$V_{\text{i},j}$	Input voltage	30 V
V_{o}	Output voltage	30 V
N_j	Turn ratio of transformer	1
$L_{\text{lk},j}$	Leakage inductance	20 μH
$f_{\text{s},j}$	Switching frequency	50 kHz
$k_{\text{p,ovc},j}$	Proportional gain of OVC	0.1
$k_{\text{i,ovc},j}$	Integral gain of OVC	10
$k_{\text{p,ivbc},j}$	Proportional gain of IVBC	0.1
$k_{\text{i,ivbc},j}$	Integral gain of IVBC	2
$C_{\text{i},j}$	Input capacitor	0.34 mF
$C_{\text{o},j}$	Output capacitor	0.34 mF

while the proportional gain of OVC is reduced to 0.0002 for a less gain margin according to (30). With the validated output impedance model, the Nyquist plot of MLG given in Fig. 18. It is predicted that the system will be unstable when the load power reaches 80 kW with oscillating frequency of 562 Hz. Fig. 19 presents the simulation waveforms that the output voltage starts oscillating with frequency of 562 Hz once the load power steps from 60 kW to 80 kW, which is consistent with the predicted result.

V. EXPERIMENTAL RESULTS

In this section, the experiments are carried out based on hardware setup consisting of two DAB submodules, shown as Fig. 20. The experimental parameters are listed as Table II. A PLECS RTBox is chosen for rapid control prototyping and waveform capturing for impedance measurement. Fig. 21 shows the transient response of input voltage during a load step. It can be seen the input voltage of two DAB submodules diverge first and then converge to the reference value at steady state, proving the validity of IVBC.

A. Input Impedance Validation

To create a voltage perturbation at the input terminal of converter, the Chroma 61512 programmable ac power supply

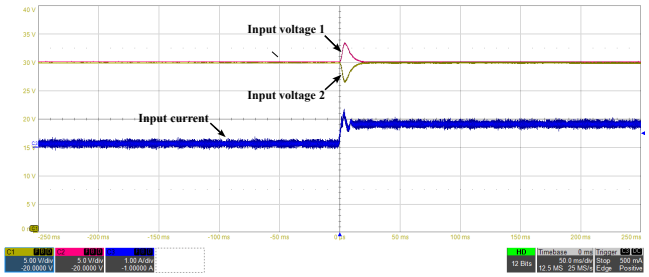


Fig. 21. The transient response of input voltage during a load step

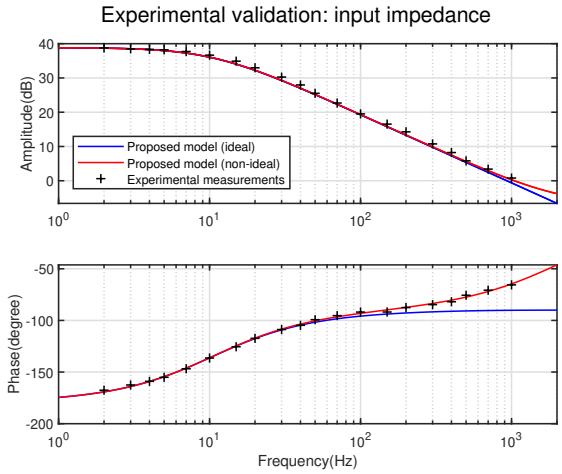


Fig. 22. Experimental verification for the input impedance of DAB-based ISOP converter

is chosen which has extremely low output impedance. In this case, the impedance in SISO form is measured. The results with the load power of 40 W are shown in Fig. 22 where the blue curve is the proposed model which is ideal and the '+' sign annotates the experimental measurements. The error between the proposed ideal model and experimental measurements can be seen as frequency increases to a few hundred Hertz. Considering the gradient for the amplitude of experimental measurements gets gently while the phase climbs toward zero degree at high frequencies, the error can be reasonably attributed to the ESR of input capacitors which are electrolytic capacitors and the contact resistance of cables and connectors/terminal blocks. To prove the hypothesis, the proposed model is modified by setting ESR of each electrolytic capacitor to be 0.2 Ω and the contact resistance to be 0.05 Ω, shown as the red curve. It can be seen that the modified model and experimental measurements matched well by considering these non-ideal characteristics.

B. Stability Analysis at the Source Side

To trigger the instability at the source side, inductors having total impedance of 0.1 Ω + 3.6 mH are connected to the input of DAB-based ISOP converter. A Chroma 63804 Programmable Electronic Load performing at constant resistance mode is connected in parallel with a 22 Ω resistive load to the output of converter to enable a further increase of load. Based on the proposed impedance model, the MLG is obtained

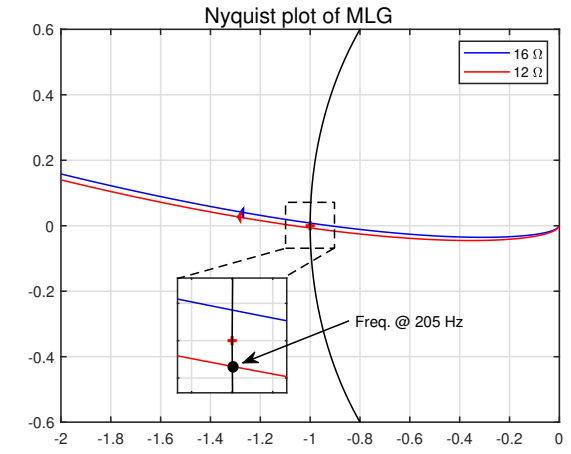
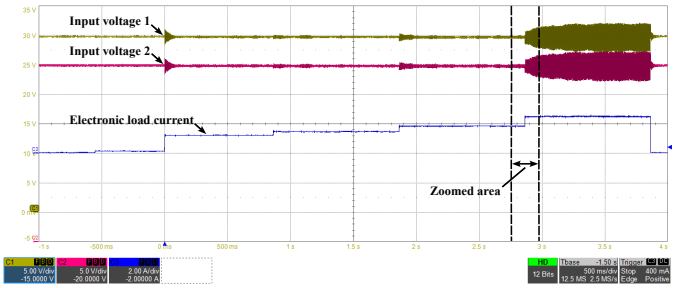
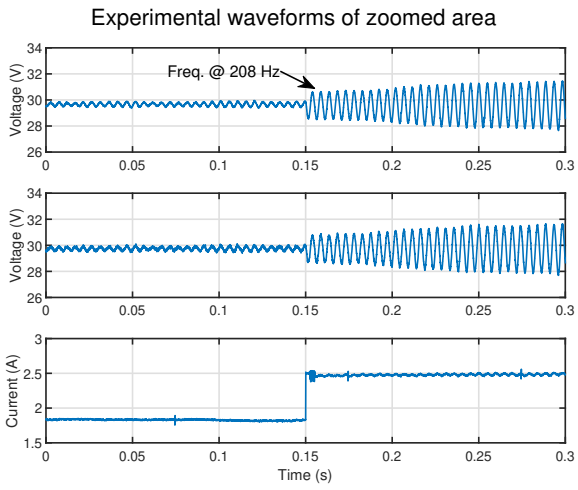


Fig. 23. The Nyquist plot of MLG with different resistance of electronic load



(a)



(b)

Fig. 24. The experimental waveforms for input voltage of each submodule and current of electronic load: (a) Full view and (b) Zoomed area

and plotted in Nyquist diagram, shown as Fig. 23. It can be concluded that the system will remain stable when electronic load is 16 Ω and will become unstable as electronic load steps to 12 Ω. Moreover, the oscillating frequency during instability is 205 Hz. To validate the predication, A degression of the load resistance from 24 Ω to 12 Ω is set for electronic load, by four steps. Fig. 24(a) shows the experimental waveforms for input voltage of each submodule and current of electronic load. An obvious oscillation in input voltage can be seen once

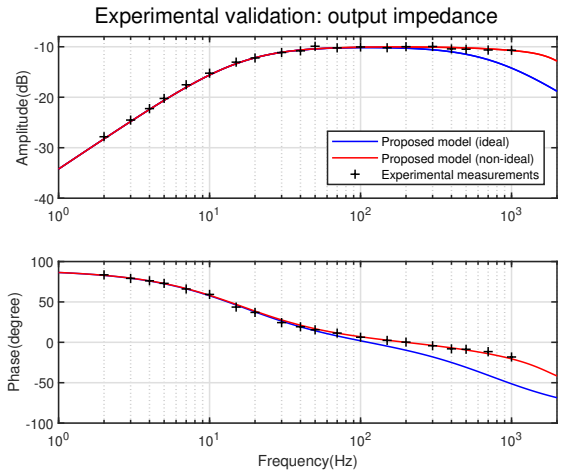


Fig. 25. Experimental verification for the output impedance of DAB-based ISOP converter

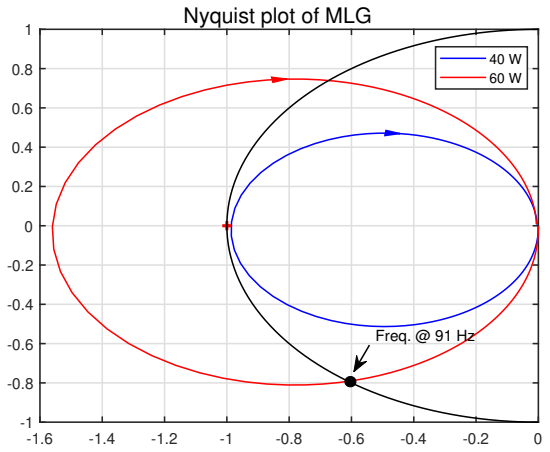


Fig. 26. The Nyquist plot of MLG when the electronic load operates at different power

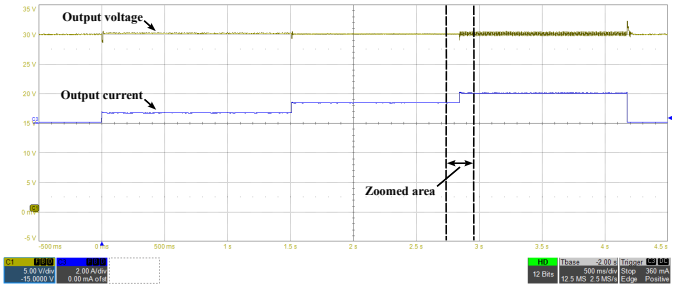
the electronics load steps from 16 Ω to 12 Ω. The zoomed waveforms of oscillations is shown in Fig. 24(b) where the oscillating frequency is around 208 Hz, showing a good match with predicted result.

C. Output Impedance Validation

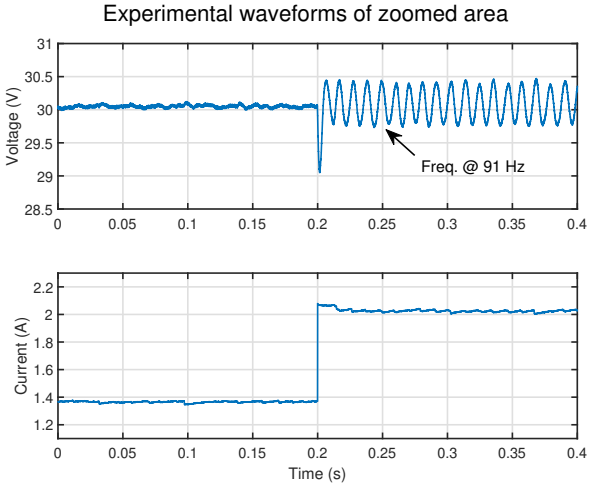
It is aforementioned in previous section that the current source load is needed to validate the output impedance of DAB-based ISOP converter. In this case, a classical boost converter is connected to the output of DAB-based ISOP converter, and the output impedance can be measured by varying the output voltage of boost converter periodically. Fig. 25 shows the experimental measurements for the output impedance of DAB-based ISOP converter when the load power is 16 W. Similar to Fig. 22, The error will become obvious as frequency reaches hundreds of Hertz where the measurements are higher in both amplitude and phase, however, the error of phase appears while the phase does not reach -90 degree, ruling out the possibility of being influenced by the ESR of output capacitance. By contrast, the delay introduced by the discretization of controllers with discrete modules (e.g. ZOH and digital delay z^{-1}) and signal processing modules (e.g. moving/periodic averaging) can be the possible reason. These discrete modules are necessary in the digital-controlled power electronics. Considering the perturbation amplitude is very small and the output of DAB-based ISOP converter contains significant switching harmonics introduced by the boost converter, the periodic averaging is adopted to sample the signals in this case. The transfer function of periodic averaging in continuous form can be approximated as

$$G_{\text{avg,periodic}}(s) = \frac{1 + (T_s s - 1)\, e^{-T_s s}}{2 T_s s} \tag{31}$$

Beside the hardware filter components on the sensor boards, the discrete modules in signal processing and control of the boost converter can also contribute to the delay of whole system, resulting in the total delay time much larger than a switching period. The red curve shows the model by adding the periodic averaging into the control path which has the sampling rate of 10 times the switching period. As a good match is observed, the effect of the equivalent delay introduced by the discrete modules of whole system on measuring the converter impedance can be evaluated thereby.



(a)



(b)

Fig. 27. The experimental waveforms for output voltage of DAB-based ISOP converter and current of electronic load: (a) Full view and (b) Zoomed area

D. Stability Analysis at the Load Side

The instability at the load side of DAB-based ISOP converter is supposed to be captured by setting the electronic load working at constant power mode. Meanwhile, according to (30), the proportional gain of voltage controller is reduced to 0.001 to trigger the instability easier. Assuming the electronic load can perfectly work as CPL at all frequencies, the MLG is calculated and plotted in Fig. 26. It can be seen that the system will be unstable if the power of electronic load steps from 40 W to 60 W, and the oscillating frequency of during instability will be around 91 Hz. Fig. 27(a) shows the experimental waveforms for output voltage of DAB-based ISOP converter and current of electronic load. An oscillation in output voltage can be observed when the power of electronic load steps from 40 W to 60 W. The detailed waveforms can be checked in Fig. 27(b), and the oscillation with frequency of 91 Hz in output voltage can be observed which is consistent with the predicted result.

VI. Conclusion

This paper explores the impedance modeling of DAB-based ISOP converter with small-signal analysis methodology, where the input impedance model and output impedance model of converter are proposed. Due to the input-series connection, the input impedance model reveals both SISO and MIMO characteristics, and the equivalence between these two characteristics is proved. The output impedance model only has SISO form, and it can be significantly simplified if the magnitude of source impedance is very low. The proposed impedance models are validated through the switching model of simulation and the hardware setup of experiment. Based on the validated impedance models, a comprehensive stability analysis is carried out at the source side and load side of converter. The results predicted by the impedance models are compared to the instability waveforms of simulation and experiment, showing a good match. As the accuracy of the proposed impedance models is confirmed, improvement of control strategy, fine selections of control and circuit parameters are supposed to be investigated to achieve system-level optimization in further study.

Appendix A

The vectors of small signal variations are listed below:

$$\hat{\boldsymbol{V}}_{\mathbf{i}} = \begin{bmatrix} \hat{V}_{\mathrm{i},1} \\ \hat{V}_{\mathrm{i},2} \\ \vdots \\ \hat{V}_{\mathrm{i},n} \end{bmatrix}, \hat{\boldsymbol{I}}_{\mathbf{i}} = \begin{bmatrix} \hat{I}_{\mathrm{i},1} \\ \hat{I}_{\mathrm{i},2} \\ \vdots \\ \hat{I}_{\mathrm{i},n} \end{bmatrix}, \hat{\boldsymbol{d}}_{\mathbf{bal}} = \begin{bmatrix} \hat{d}_{\mathrm{bal},1} \\ \hat{d}_{\mathrm{bal},2} \\ \vdots \\ \hat{d}_{\mathrm{bal},n} \end{bmatrix}$$

$$\hat{\boldsymbol{I}}_{\mathbf{1}} = \begin{bmatrix} \hat{I}_{1,1} \\ \hat{I}_{1,2} \\ \vdots \\ \hat{I}_{1,n} \end{bmatrix}, \hat{\boldsymbol{I}}_{\mathbf{2}} = \begin{bmatrix} \hat{I}_{2,1} \\ \hat{I}_{2,2} \\ \vdots \\ \hat{I}_{2,n} \end{bmatrix}$$

The aforementioned diagonal matrices in (16) and (20) are:

$$\boldsymbol{G}_{\mathbf{I1d}} = \mathrm{diag}(G_{\mathrm{I1d},1}, G_{\mathrm{I1d},2}, ..., G_{\mathrm{I1d},n})$$
$$\boldsymbol{G}_{\mathbf{I2d}} = \mathrm{diag}(G_{\mathrm{I2d},1}, G_{\mathrm{I2d},2}, \ldots, G_{\mathrm{I2d},n})$$
$$\boldsymbol{G}_{\mathbf{I2Vi}} = \mathrm{diag}(G_{\mathrm{I2Vi},1}, G_{\mathrm{I2Vi},2}, \ldots, G_{\mathrm{I2Vi},n})$$
$$\boldsymbol{G}_{\mathbf{ivbc}}(s) = \mathrm{diag}(G_{\mathrm{ivbc},1}(s), G_{\mathrm{ivbc},2}(s), ..., G_{\mathrm{ivbc},n}(s))$$
$$\boldsymbol{C}_{\mathbf{i}} = \mathrm{diag}(C_{\mathrm{i},1}, C_{\mathrm{i},2}, ..., C_{\mathrm{i},n})$$

The correction factor matrix of $\hat{\boldsymbol{V}}_{\mathbf{i}}$ as input of IVBC is given as

$$\boldsymbol{G}_{\mathbf{Vic}} = \frac{1}{n} \begin{bmatrix} 1-n & 1 & \cdots & 1 \\ 1 & 1-n & \cdots & 1 \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & \cdots & 1-n \end{bmatrix}$$

The gain matrix of $\hat{\boldsymbol{I}}_{\mathbf{2}}$ as output for the closed loop of input voltage to output current is given as

$$\boldsymbol{G}_{\mathbf{I2c}} = \mathbf{I} + \boldsymbol{G}_{\mathbf{I2d}}\boldsymbol{G}_{\mathbf{ovc}}(s) Z_{\mathrm{load,eq}}(s) \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix} = \begin{bmatrix} 1-G_{\mathrm{I2d},1}A_1 & -G_{\mathrm{I2d},1}A_1 & \cdots & -G_{\mathrm{I2d},1}A_1 \\ -G_{\mathrm{I2d},2}A_2 & 1-G_{\mathrm{I2d},2}A_2 & \cdots & -G_{\mathrm{I2d},2}A_2 \\ \vdots & \vdots & \ddots & \vdots \\ -G_{\mathrm{I2d},n}A_n & -G_{\mathrm{I2d},n}A_n & \cdots & 1-G_{\mathrm{I2d},n}A_n \end{bmatrix}$$

where $\mathbf{I}$ is the identity matrix, $\boldsymbol{G}_{\mathbf{ovc}}(s)$ is the vector of OVC as follows:

$$\boldsymbol{G}_{\mathbf{ovc}}(s) = \begin{bmatrix} G_{\mathrm{ovc},1}(s) & G_{\mathrm{ovc},2}(s) & \cdots & G_{\mathrm{ovc},n}(s) \end{bmatrix}^{\mathrm{T}}$$

The transfer function matrix of output current to input current for DAB submodules is:

$$\boldsymbol{G}_{\mathbf{I1I2}} = [\boldsymbol{G}_{\mathbf{I1Vo}} - \boldsymbol{G}_{\mathbf{I1d}}\boldsymbol{G}_{\mathbf{ovc}}(s)] Z_{\mathrm{load,eq}} \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix} = \begin{bmatrix} B_1 + G_{\mathrm{I1d},1}A_1 & B_1 + G_{\mathrm{I1d},1}A_1 & \cdots & B_1 + G_{\mathrm{I1d},1}A_1 \\ B_2 + G_{\mathrm{I1d},2}A_2 & B_2 + G_{\mathrm{I1d},2}A_2 & \cdots & B_2 + G_{\mathrm{I1d},2}A_2 \\ \vdots & \vdots & \ddots & \vdots \\ B_n + G_{\mathrm{I1d,n}}A_n & B_n + G_{\mathrm{I1d,n}}A_n & \cdots & B_n + G_{\mathrm{I1d,n}}A_n \end{bmatrix}$$

where $\boldsymbol{G}_{\mathbf{I1Vo}}$ is the small signal gain vector of input current to output voltage, given as

$$\boldsymbol{G}_{\mathbf{I1Vo}} = \begin{bmatrix} G_{\mathrm{I1Vo},1} & G_{\mathrm{I1Vo},2} & \cdots & G_{\mathrm{I1Vo},n} \end{bmatrix}^{\mathrm{T}}$$

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