# A Novel Phase-lock Loop with Feed-back Repetitive Controller for Robustness to Periodic Disturbance in Three-phase Systems


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***Abstract*—While power networks evolve towards the new concept of smart grids, with the proliferation of power electronics embedded systems and distributed generation, the insurgence of system unbalance and voltage harmonic distortion, become more and more frequent. Also, often a noisy voltage sampling system can produce offsets in measurements. Such imperfections bring challenges to the phase identification using a traditional phase-lock loop (PLL), utilized in the control of all grid connected converters. However, since the imperfections lead to periodic harmonics in the corresponding dq-axis voltages, the repetitive controller (RC) can be useful for harmonic suppression. This paper presents a three- phase PLL using a feed-back RC. Specially, a novel running mean filter has been added to minimize the interaction between RC and the Proportional-Integral (PI) controller in the PLL. Simulation results show that the proposed PLL can track the phase of the three-phase voltage without being influenced by harmonic distortion.**



***Keywords— repetitive control, phase-lock loops, power system harmonics, fault tolerant control, three-phase electric power***


## I. INTRODUCTION

More and more power electronics are involved the power networks with development of smart grids including distributed generation. Harmonics introduced by the power converters, short circuits, the unbalanced load among the three phases, as well as the measurement offset and noise may result in variety of harmonics in the dq-axis voltage, and bring challenges for the phase identification using a traditional phase-lock loop (PLL).

Many PLL solutions have been proposed in literature in the past decades. For example, four different structures of three-phase PLLs are found and compared in [1], while two three-phase PLL systems are compared in [2]. In this paper, the simplest PLL configuration, as shown in Fig.1, is considered as a basis of the proposed implementation.

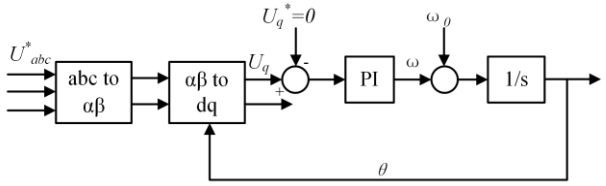



Fig. 1 Block diagram of a basic phase-lock loop.

Considering a reference frame in which the *d*-axis aligns with the *a*-axis of the three-phase when the phase angle is zero, and assuming phase *a* voltage is at its maximum value when the phase angle is zero, if the tracked phase $\theta$ (as drawn in Fig.1) equals the phase angle, $U_q$ should equal zero. Since the proportional integral (PI) controller forces the *q*-axis voltage $U_q$ to be zero in the steady state, eventually, the phase $\theta$ equals to the phase angle between the *d*-axis and the *a*-axis.

However, the *q*-axis voltage $U_q$ may contain harmonics, therefore will not be zero even when phase angle $\theta$ is correct. In another words, $U_q$=0 cannot be used as a sign for indicating the correctness of phase tracking. For example, harmonics can be generated in $U_q$ from the following three sources, and these harmonics bring periodic errors in the tracked phase $\theta$ of the PLL:

1) if 5$^{th}$, 7$^{th}$ harmonics are present in $U^*_{abc}$, 6$^{th}$ harmonics will be present in $U_{dq}$ (as well as multiple of the 6$^{th}$ harmonic in the presence of higher order harmonics in the system);

2) if there is a ground fault on one of the three phases, 2$^{nd}$ harmonics will be present in $U_{dq}$;

3) if the voltage amplitudes of any two phases are wrongly measured or in the presence of voltage sags, 2nd harmonics will be produced in $U_{dq}$.

Therefore, it is necessary to enhance the robustness of PLL against harmonics or faults with other advanced algorithms [3-6]. Discrete Fourier Transform algorithms are used for identifying the fundamental frequency in [3, 4]. A complex Hilbert filter, is proposed for the PLL in [5].

Alternatively, the PLL in Fig.1 will be able to operate correctly if the PI controller is "blind" for the harmonics and only works to bring the d.c. part of $U_q$ to zero. This harmonic rejection feature can be achieved using a repetitive controller (RC).

RC is originally proposed in 1981 for motor control application in order to track periodic reference [7-10]. RC is a perfect tool for periodic signals tracking or periodic harmonics rejection. As shown in Fig.2, it memorizes the periodic error with a delay chain $z^{-N}$, where $N$ is the closest integer of the ratio between the sampling frequency $f_s$ and the frequency of the target periodic error. The periodic error is amplified by the gain $G_{rc}$. The robustness filter $Q_f(z)$ is generally a low-pass filter with the function of attenuating the amplitude of the controller gains at high frequency harmonics. In this paper, it is chosen to be a gain in the range of zero to one (called forgetting factor $Q_{rc}$) providing an equal attenuation at all frequencies. The stability filter $G_f(z)$ is commonly required for removing the phase shift between the compensation action and the target error. $G_f(z)$ needs to be carefully designed to ensure not only the stability, but also higher performance.

Authors in [6] have proposed a feed-forward multi-band-pass filter based PLL configuration. The pass bands of the filter are some selected even harmonics. Although, this multi-band-pass filter is also named RC, it is totally different from the conventional RC as in Fig.2.

The feed-back conventional RC based structure in Fig.3 is instead adopted for this paper. The working principle of the proposed PLL will be discussed in the next section.

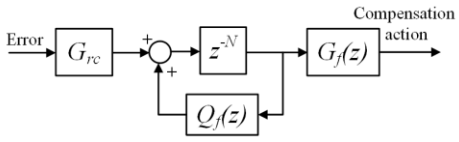



Fig. 2 Block diagrams of a repetitive controller.

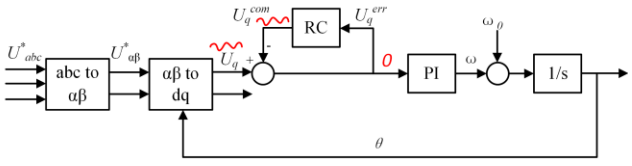



Fig. 3 Block diagrams of the proposed PLL with feed-back RC.

Overall, the aim of this paper is to propose a novel PLL which can track the correct fundamental frequency and phase even under extreme conditions such as odd harmonic distortion, single phase to ground fault, two-phase voltage sags, frequency variation and phase jumps. Two main points are considered in the development of the intended PLL:

- To enhance the robustness of the PLL in Fig.1 against harmonics in $U_q$, a feed-back RC as in Fig.3 is proposed to cancel the ripple component in $U_q$.
- To ensure that the RC only cancels the ripple in $U_q$, the stability filter $G_f(z)$ of the proposed RC is chosen to be a running mean filter $G_{rmf}(z)$ to filter out the d.c. value.

The performance of the proposed PLL is confirmed in the simulation tests.

## II. The Proposed PLL with Feed-back RC

The diagram of the proposed PLL is shown in Fig.3. Theoretically, at steady state, the input of PI controller and repetitive controller (RC) will be zero, whereas the ripple components contained in $U_q$ are stored in RC through the learning process, and are cancelled by the output $U_q^{com}$ of RC. $\omega_0$ is the initial value for the output of PI ω.

The equation of the RC in Fig.3 can be expressed as in (1).

$$RC=\frac{U_q^{com}}{U_q^{err}}=\frac{G_{rc}G_f(z)z^{-N}}{1-Q_{rc}z^{-N}} \tag{1}$$

Where, $U_q^{err}$ is the input of RC, $U_q^{com}$ is the output of RC. Again, $Q_{rc}$ is the forgetting factor of RC ($Q_{rc}\in[0,1]$), $G_{rc}$ is the gain of RC, $G_f(z)$ is the robustness filter. $N$ is the closest integer of the ratio between the sampling frequency $f_s$ and the fundamental frequency $f_d$ of the three-phase voltages.

The PI controller is expressed as in (2). Where, $k_p$ is the proportional gain of PI, and $k_i$ is the integral gain. $T_s$ is the sampling period, and $T_s=1/f_s$.

$$PI=k_p+k_i\cdot\frac{T_s}{z-1} \tag{2}$$

As may have been noticed, the parameters free for tuning are the $G_{rc}$, $Q_{rc}$ of RC, and $k_p$, $k_i$ of PI. These parameters can be chosen according to the system stability. Before the stability of the system can be analyzed, it is worth now deriving the equivalent diagram for the proposed PLL with feed-back RC as in Fig.3.

### A. Equivalent Diagram and Working Principle of the Proposed PLL with Feed-back RC

The $\alpha\beta$-axis voltages $U_{\alpha\beta}^*$ can be expressed as in (3). Where, $A$ denotes the peak value of the three-phase voltages. Phase $\theta^*$ denotes the actual phase of the three-phase system.

$$\begin{cases}U_\alpha^*=A\cos\theta^*\\U_\beta^*=A\sin\theta^*\end{cases} \tag{3}$$

Hence, the real $dq$-axis voltages $U_{dq}^*$ after the $\alpha\beta$ to $dq$ transformation are defined in (4).

$$\begin{bmatrix}U_d^*\\U_q^*\end{bmatrix}=\begin{bmatrix}\cos(\theta^*) & \sin(\theta^*)\\-\sin(\theta^*) & \cos(\theta^*)\end{bmatrix}\begin{bmatrix}U_\alpha^*\\U_\beta^*\end{bmatrix} \tag{4}$$

Substituting (3) into (4), we can know that, ideally, $U_d^*=A$ and $U_q^*=0$. Assuming the tracked phase $\theta$ in the PLL has a small error $\delta\theta$ when compared with the actual phase $\theta^*$, i.e. $\theta=\theta^*+\delta\theta$. The "feedback" $dq$-axis voltages $U_{dq}$ are defined as in (5).

$$\begin{bmatrix} U_d \\ U_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} U_\alpha^* \\ U_\beta^* \end{bmatrix} \tag{5}$$

The relationship between $U_{dq}^*$ and $U_{dq}$ can be derived from (4) and (5). As shown in (6), the magnitude of $U_q$ depends on $A$ and $\delta\theta$.

$$\begin{bmatrix} U_d \\ U_q \end{bmatrix} = \begin{bmatrix} \cos(\delta\theta) & \sin(\delta\theta) \\ -\sin(\delta\theta) & \cos(\delta\theta) \end{bmatrix} \begin{bmatrix} U_d^* \\ U_q^* \end{bmatrix} = \begin{bmatrix} \cos(\delta\theta) & \sin(\delta\theta) \\ -\sin(\delta\theta) & \cos(\delta\theta) \end{bmatrix} \begin{bmatrix} A \\ 0 \end{bmatrix} \tag{6}$$

Since $\delta\theta$ is assumed to be small, $\sin(\delta\theta)\approx\delta\theta$ is hold. Therefore, $q$-axis voltage $U_q=-A\sin(\delta\theta)\approx -A\cdot\delta\theta$. Based on this conclusion, the equivalent circuit (in discrete form) of Fig.3 can be drawn as in Fig.4.

Again, the $U_q^*$ in Fig.4 is defined as in (4). It is the $q$-axis voltage when the phase used for the $\alpha\beta$ to $dq$ transformation is correct. As discussed after (4), $U_q^*=0$ is hold when the $\alpha\beta$-axis voltages are as ideal as in (3), i.e. when the three-phase voltages are perfectly balanced and pure sinusoidal. However, if the three-phase system is not balanced or contains ripple, $U_q^*$ will contain ripple as well.

As illustrated in Fig.4, the working principle of the proposed PLL with feed-back RC is to use the RC to track the a.c. part (i.e. ripple part) of $U_q^*$, whereas, the PI controller is used to track the d.c. part (equals zero) of $U_q^*$. Ideally, at steady state, $U_q^{com}$ cancels all the ripple in $U_q^*$, so that the input of PI equals zero, and indicates $\delta\theta=0$, i.e. the correctly tracking of the phase.

### B. *Tuning of the Proposed PLL with Feed-back RC*

Following the system diagram in Fig.4, the closed loop transfer function $G_{closed}(z)$ can be derived as in (7), where $G_p(z)=AT_s/(z-1)$.

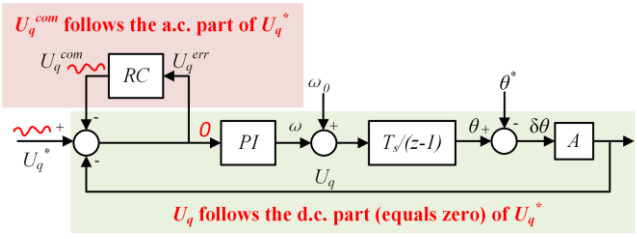



Fig. 4 Equivalent diagram of the proposed PLL with feed-back RC.

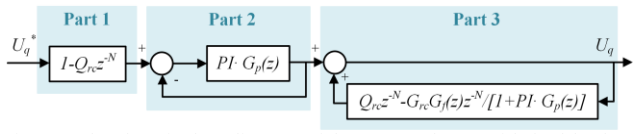



Fig. 5 Updated equivalent diagram of the proposed PLL with feed-back RC

$$G_{closed}(z)=\frac{\frac{1}{1+RC}\cdot PI\cdot G_p(z)}{1+\frac{1}{1+RC}\cdot PI\cdot G_p(z)}$$

$$=\left(1-Q_{rc}z^{-N}\right)\cdot\frac{PI\cdot G_p(z)}{1+PI\cdot G_p(z)}\cdot\frac{1}{1-\left[Q_{rc}z^{-N}-\frac{G_{rc}G_f(z)z^{-N}}{1+PI\cdot G_p(z)}\right]} \tag{7}$$

According to (7), the proposed PLL-RC system can be divided into three parts as shown in Fig.5. The stability can be ensured if each part of the three is designed to be stable [11, 12].

In fact, the part 2 in Fig.5 is the closed loop system without the RC. Therefore, the first step of tuning the proposed PLL is to tune the PI controller without considering the RC.

The relationship between the proportional gain $K_p$, integral gain $K_i$ of PI and the natural frequency $\omega_n$, damping $\zeta$ is given by (8), which can be derived from the equivalent circuit in Fig. 4 and Fig.5.

$$k_p=\frac{2\zeta\omega_n}{A},\ k_i=\frac{\omega_n^2}{A} \tag{8}$$

The part 1 in Fig.5 is actually the denominator of the RC equation in (1). By substitution $z$ with $e^{j\omega Ts}$, the term $1-Q_{rc}z^{-N}$ can be expressed as $1-Q_{rc}e^{-jN\omega Ts}$. Again, $N=f_s/f_d=1/(T_sf_d)$, $T_s$ is the sampling period. Therefore, the boundary of $(1-Q_{rc}e^{-jN\omega Ts})$ can be calculated. Its minimum value $(1-Q_{rc})$ is achieved when $N\omega T_s=2\pi k$, $k=0, 1, 2\ldots$, i.e. $\omega=2\pi kf_d$. Since the design intention is to reject all periodic harmonics at the fundamental frequency and its multiple frequencies, $Q_{rc}$ is chosen to be one for the maximum attenuation, and consequently, the system response will be zero for inputs at the fundamental frequency and its multiple frequencies.

From the discussions above for the part 2 and part 1, we can know that the input and output of the part 3 is bounded. For bounded system, the small gain theorem [13] can be applied to ensure the stability. The part 3 will be stable if (9) is hold (when $Q_{rc}=1$).

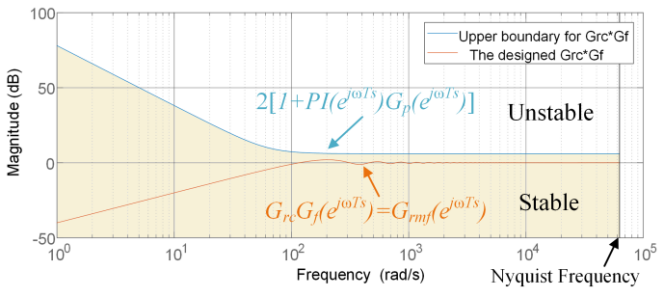
$$|S(e^{j\omega Ts})|=\left|1-\frac{G_{rc}G_f(e^{j\omega Ts})}{1+PI(e^{j\omega Ts})\cdot G_p(e^{j\omega Ts})}\right|\cdot|e^{-jN\omega Ts}|<1 \tag{9}$$

Where, $\omega\in[0, \pi/T_s]$, $\pi/T_s$ is the Nyquist frequency in rad/s. Eq. (9) can be used as the stability criterion for choosing the gain $G_{rc}$ and robustness filter $Q_f(z)$ of RC. Since $|e^{-jN\omega Ts}|$ is within zero to one. Equation (9) can be simplified into (10).

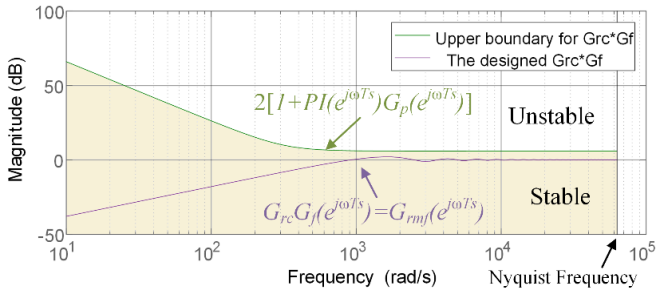
$$\left|1-\frac{G_{rc}G_f(e^{j\omega Ts})}{1+PI(e^{j\omega Ts})\cdot G_p(e^{j\omega Ts})}\right|<1$$

$$0<\left|\frac{G_{rc}G_f(e^{j\omega Ts})}{1+PI(e^{j\omega Ts})\cdot G_p(e^{j\omega Ts})}\right|<2 \tag{10}$$

In this paper, the natural frequency $\omega_n$ and damping $\zeta$ are chosen to be 62.83rad/s (i.e.10Hz) and 0.791 respectively for the condition when the fundamental frequency $f_d$ of the three-phase voltages is 50Hz. Calculating from (8), $k_p=1$ and $k_i=40$. Similarly, when $f_d=400$Hz, choose $\omega_n=314$rad/s (i.e.50Hz), $\zeta=0.791$, such that $k_p=5$, $k_i=1000$. The peak value of the fundamental component in the three-phase system $A$ is 100V. Substituting $A$, $k_p$, $k_i$ into $PI(e^{j\omega Ts})G_p(e^{j\omega Ts})$, we can find that




(a) When $f_d$=50Hz and $N$=400




(b) When $f_d$=400Hz and $N$=50

Fig. 6 Magnitude response of the $G_{rc}G_f(z)$ if $G_{rc}$=1, $G_f(z)$= $G_{rmf}(z)$.

$PI(e^{j\omega Ts})G_p(e^{j\omega Ts})$ is always above zero. Consequently, it can be derived from (10) that the system will be sufficiently stable if (11) is hold.

$$0<\left|G_{rc}G_f(e^{j\omega T_s})\right|<2[1+PI(e^{j\omega T_s})\cdot G_p(e^{j\omega T_s})] \quad (11)$$

Another point need to be considered is that $Q_{rc}$, $G_{rc}$ and $G_f(z)$ not only affect the stability of the system, but also the performance. As aforementioned, the maximum attenuation of periodic harmonics can be achieved when $Q_{rc}$=1. The gain $G_{rc}$ mainly affects the converge speed of the RC[14]. The robustness filter $G_f(z)$ is designed to be a running mean filter as below.

### C. Running Mean Filter

As described in the working principle in section II-*A*, it is desired that RC would only react to the a.c. part of $U_q^*$. However, steady state error in the tracked phase θ may occur in the following scenario.

For example, when the fundamental frequency $f_d$ of the three-phase voltages varies, a d.c. offset will be present in $U_q$ due to the sudden mismatch between the tracked frequency and $2\pi f_d$. Consequently, the sudden voltage error in $U_q^{err}$ will be recorded in the delay chain of RC, and therefore, be cancelled or partly cancelled by $U_q^{com}$. Meanwhile, PI will also react on this voltage error until the offset is reduced to zero. Eventually, due to the present of a d.c. component in $U_q^{com}$, $U_q$ will not be zero at steady state, and the remaining offset in $U_q$ is responsible for the steady state error in the tracked phase $\theta$.

To remove the d.c. component in $U_q^{com}$, the robustness filter $G_f(z)$ is chosen to be the running filter $G_{rmf}(z)$ as expressed in (12), where, $z^{-N}G_{rmf}(z)$ can be understood as the $z^{-N}$ minus a moving average filter, of which the window size is $N$.

$$z^{-N}G_{rmf}(z)=z^{-N}-\frac{1}{N}(z^{-(N-1)}+\cdots+z^{-2}+z^{-1}+1)$$

$$G_{rmf}(z)=1-\frac{1}{N}(z+\cdots+z^{N-2}+z^{N-1}+z^N) \quad (12)$$

Fig.6 shows the magnitude response of $G_{rc}G_f(z)$ when $G_f(z)=G_{rmf}(z)$, and $G_{rc}=1$. As shown, the design satisfies the stability condition given by (11).

The problem of having steady state error in the tracked phase and the effectiveness of the running mean filter will be simulated in section III-*E*. The performance when $G_f(z)=1$ and when $G_f(z)=G_{rmf}(z)$ are compared.

## III. Simulation Results

Simulation tests are carried out to verify the proposed PLL system performance under five non-ideal conditions as follows, including both grids at 50Hz and 400Hz. The control parameters for the tests are defined in Table I. The natural frequency of the PI is chosen to be smaller than $f_d$.

### A. Condition 1: Odd Harmonics in $U^*_{abc}$ and with Fundamental Frequency (50Hz) Variation

In this test, 10% 5th and 5% 7th harmonics are included in the three-phase voltages $U^*_{abc}$ as given in (13). The total harmonic distortion (THD) is 11.18%.

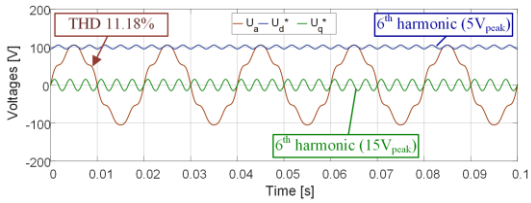
$$\begin{cases} U_a^*=100\cos(\theta^*)+10\cos(5\theta^*)+5\cos(7\theta^*) \\ U_b^*=100\cos(\theta^*-\frac{2\pi}{3})+10\cos(5\theta^*-\frac{10\pi}{3})+5\cos(7\theta^*-\frac{14\pi}{3}) \\ U_c^*=100\cos(\theta^*+\frac{2\pi}{3})+10\cos(5\theta^*+\frac{10\pi}{3})+5\cos(7\theta^*+\frac{14\pi}{3}) \end{cases} \quad (13)$$

Where, $d\theta^*/dt=2\pi f_d$, again, $f_d$ is the fundamental frequency of the three-phase voltages $U^*_{abc}$, and $f_d$ varies from 49.5Hz to 50.5Hz during the test. The initial angular frequency $\omega_0$ shown in Fig.3 and Fig.4 is set to be 100π rad/s for the 50 Hz system.

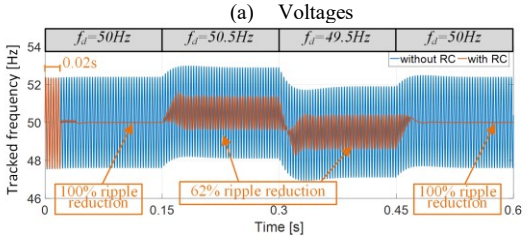
Fig.7a shows the real *dq*-axis voltages (i.e. $U_{dq}^*$) as defined in (4). Fig.7b and Fig.7c show respectively the tracked frequency and phase calculated by the PLL with/without the proposed RC (includes the running mean filter).

The waveforms in Fig.7 confirms the following points:

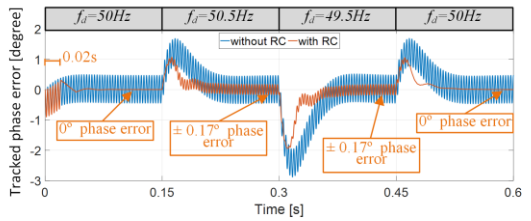
- The 5th and 7th harmonics in the three-phase system leads to 6th harmonics in its *dq*-axis voltages. However, the d.c. part of the real *q*-axis voltage $U_q^*$ is still zero. This motivates the use of RC to cancel the a.c. component in $U_q^*$.
- The performance is the best when $f_d$=50 Hz, and perfect frequency tracking and zero phase tracking error are achieved. The performance degrades slightly to ±0.17° phase tracking error, as shown in Fig.6c, when $f_d$ varies from 49.5 Hz to 50.5 Hz. This is due to the mismatch between the actual period of the three phases and the corresponding fixed value $N$ used in the delay chain.
- The RC is activated at 0s, and starts to take effect after the first period (i.e. 0.02s)




(a) Voltages

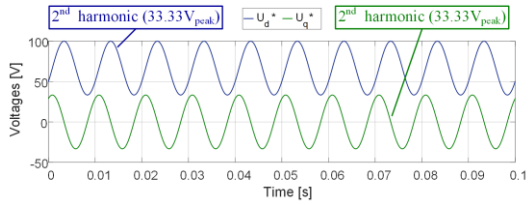



(b) Tracked frequency

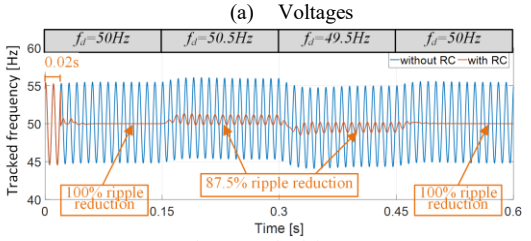



(c) Tracked phase error in degree

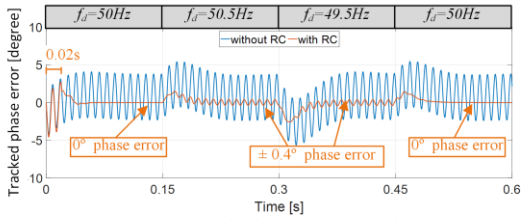
Fig. 7 Performance of PLL with/without the proposed RC when $U^*_{abc}$ have 5th, 7th harmonics and during fundamental frequency variation ($f_d$=49.5~50.5 Hz).




(a) Voltages




(b) Tracked frequency




(c) Tracked phase error in degree

Fig. 8 Performance of PLL with/without RC under phase *c* to ground fault and during fundamental frequency variation ($f_d$=49.5~50.5Hz).

### *B. Condition 2: Phase c to Ground Fault and with Fundamental Frequency (50Hz) Variation*

In this test, the three-phase voltages as in (14) are considered, where, the phase *c* is missing. $d\theta^*/dt=2\pi f_d$, $f_d$ varies from 49.5Hz to 50.5Hz during the test. The initial angular frequency $\omega_0$ shown in Fig.3 and Fig.4 is set to be 100π rad/s.

$$\begin{cases} U_a^*=100\cos(\theta^*) \\ U_b^*=100\cos(\theta^*-\frac{2\pi}{3}) \\ U_c^*=0 \end{cases} \quad (14)$$

Fig.8a shows the real *dq*-axis voltages (i.e. $U_{dq}{}^*$) as defined in (4). Fig.8b and Fig.8c show respectively the tracked frequency and phase calculated by the PLL with/without the proposed RC (includes the running mean filter).

It can be seen from Fig.8:

- Single phase to ground fault in the three-phase system leads to 2nd harmonics in its *dq*-axis voltages.
- The performance is the best when $f_d$=50 Hz, and perfect frequency tracing and zero phase tracing error are achieved. The performance degrades to ±0.4° phase tracing error as shown in Fig.7c when $f_d$ varies from 49.5 Hz to 50.5 Hz.

### *C. Condition 3: Wrong Voltage Amplitude in $U_a{}^*$, $U_b{}^*$ and with Fundamental Frequency (50Hz) Variation*

In this test, the three-phase voltages as in (15) are considered, where, the amplitudes of phase *a* and phase *b* are half. $d\theta^*/dt=2\pi f_d$, $f_d$ varies from 49.5Hz to 50.5Hz during the test. The initial angular frequency $\omega_0$ shown in Fig.3 and Fig.4 is set to be 100π rad/s.

$$\begin{cases} U_a^*=50\cos(\theta^*) \\ U_b^*=50\cos(\theta^*-\frac{2\pi}{3}) \\ U_c^*=100\cos(\theta^*+\frac{2\pi}{3}) \end{cases} \quad (15)$$

Fig.9a shows the real *dq*-axis voltages (i.e. $U_{dq}{}^*$) as defined in (4). Fig.9b and Fig.9c show respectively the tracked frequency and phase calculated by the PLL with/without the proposed RC (includes the running mean filter).

Similar to the results in section III-*B*, the proposed PLL-RC system works better than the original PLL for both frequency and phase tracking when the amplitudes of $U^*_a$ and $U^*_b$ are half of the amplitude of $U^*_c$.

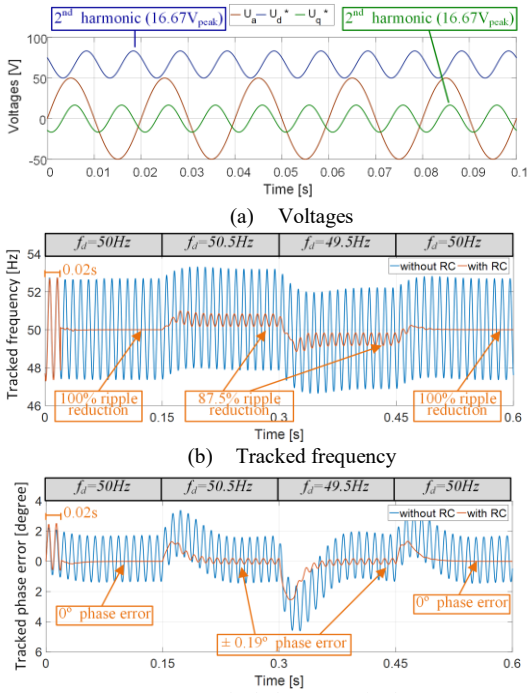
### *D. Condition 4: Odd Harmonics in $U^*_{abc}$ and with Fundamental Frequency (400Hz) Variation*

In this test, the same three-phase voltages as in (13) are considered. However, $f_d$ varies from 399 Hz to 401 Hz during the test. The initial angular frequency $\omega_0$ shown in Fig.3 and Fig.4 is set to be 800π rad/s for the 400 Hz system.

Fig.10a shows the real *dq*-axis voltages (i.e. $U_{dq}{}^*$) as defined in (4). Fig.10b and Fig.10c show respectively the tracked frequency and phase calculated by the PLL with/without the proposed RC (includes the running mean filter).

Similar to the results in section III-*A*, the RC starts to take effect after one cycle (1/400=0.0025s). The proposed PLL and RC works significantly better than the original PLL for both

frequency and phase tracing for a 400Hz distorted three-phase system.

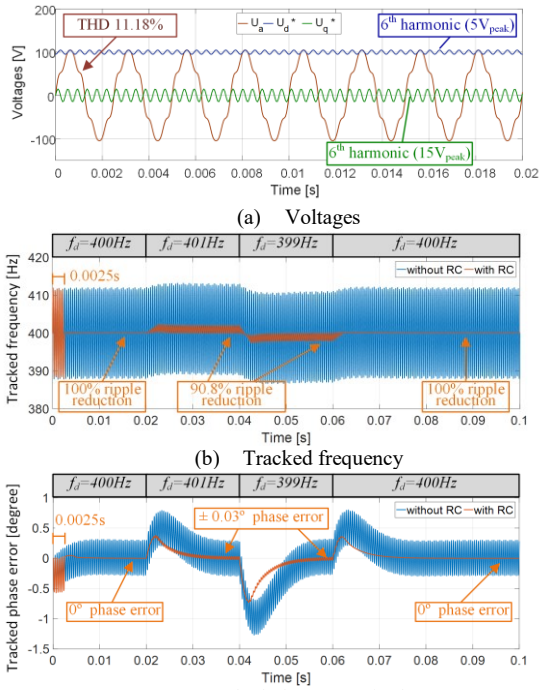



(a) Voltages

(b) Tracked frequency

(c) Tracked phase error in degree

Fig. 9 Performance of PLL with/without RC when $U_a^*$ and $U_b^*$ are half the amplitude of $U_c^*$ and with fundamental frequency variation($f_d$=*49.5~50.5Hz*).




(a) Voltages

(b) Tracked frequency

(c) Tracked phase error in degree

Fig. 10 Performance of PLL with/without the proposed RC when $U^*_{abc}$ have

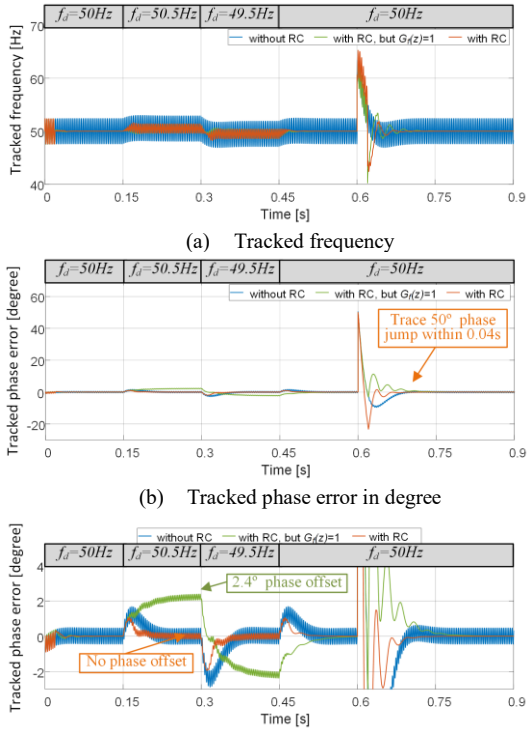
### *E. Condition 5: Phase Jump and Fundamental Frequency (50Hz) Variation*

In this test, the same three-phase voltages as in (13) are considered. $f_d$ also varies from 49.5 Hz to 50.5 Hz during the test as in section III-*A*. Additionally, a 50º phase jump in the three-phase voltages are applied at 0.6s. The initial angular frequency $\omega_0$ shown in Fig.3 and Fig.4 is set to be 100π rad/s. The performance of the proposed RC (i.e. $G_f(z)=G_{rmf}(z)$) is compared with the RC when $G_f(z)$=1.

Fig.11a shows that comparable frequency tracking performance is achieved when with and without the running mean filter $G_{rmf}(z)$.

The advantage of using $G_{rmf}(z)$ can be seen from Fig.11b and Fig.11c for the phase tracking. As shown, large phase offset is present only when $G_{rmf}(z)$ is not used. Again, such phase offset is caused by the d.c. offset in the output $U_q^{com}$ of RC. The phase offset is removed by the proposed running mean filter.

Fig.11 also confirms that the proposed PLL with feed-back RC can track the 50º phase jump within 0.04s (i.e. two periods).




(a) Tracked frequency

(b) Tracked phase error in degree

(c) Zoom in of (b)

Fig. 11 Performance of PLL with the RC (but $G_f(z)=1$) and the proposed RC ($G_f(z)=G_{rmf}(z)$) when $U^*_{abc}$ have 5th, 7th harmonics, during fundamental frequency variation ($f_d$=*49.5~50.5 Hz*) and during 50º phase jump at 0.6s.

## IV. Conclusions

This paper aims at improving the frequency and phase tracking performance of a PLL in distorted three-phase system. Five non-ideal grid conditions are considered in this paper in order to test the effectiveness of the proposed solution, including harmonics in the three-phase voltages, the single phase to ground fault, the two-phase sag fault or sampling error, slight frequency variations, and phase jumps. It is found that certain

harmonics will be generated in the $q$-axis voltage $U_q$ for these conditions, and the perfect phase tracking can be achieved by controlling the d.c. value of $U_q$ to zero. This motivates the use of a repetitive controller (RC) within a traditional PLL configuration to remove the a.c. component in $U_q$. Furthermore, a running mean filter based RC is proposed in order to make sure the RC only compensates the a.c. part of $U_q$.

The tuning of the PI controller and RC in the proposed PLL have been demonstrated according to the stability analysis.

As verified in five selected non-ideal conditions, the proposed PLL with feed-back RC can improve frequency and phase tracking with respect to the traditional three-phase PLL under periodic disturbance conditions. Although the proposed PLL is mainly designed for fixed frequency systems, it works effectively even under slight frequency variations as previously demonstrated.

TABLE I
CONTROL PARAMETERS FOR SIMULATION TESTS

| Symbol | Quantity | Value |
|---|---|---|
| $T_s$ | Sampling period | 0.00005 s |
| $f_s$ | Sampling frequency | 20 kHz |
| $f_d$ | Fundamental frequency of the three-phase voltages | 50 or 400 Hz |
| $A$ | Peak value of the fundamental component in three-phase | 100 V |
| $N$ | Length of delay chain in RC | 400 (if $f_d$ =50 Hz)<br>50 (if $f_d$ =400 Hz) |
| $G_{rc}$ | Gain of RC | 0.888 |
| $Q_{rc}$ | Forgetting factor of RC | 1 |
| $\zeta$ | Damping | 0.791 |
| $\omega_n$ | Natural frequency of PI | 62.83 rad/s (if $f_d$ =50 Hz)<br>314 rad/s (if $f_d$ =400 Hz) |
| $k_p=2\zeta\omega_n/A$ | Proportional gain of PI | 1 (if $f_d$ =50 Hz)<br>5 (if $f_d$ =400 Hz) |
| $k_i=\omega_n^2/A$ | Integral gain of PI | 40 (if $f_d$ =50 Hz)<br>1000 (if $f_d$ =400 Hz) |

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