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Phase-Shift-Modulation for a Current-Fed Isolated DC-DC Converter in More Electric Aircrafts

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***Abstract*—A Phase-Shift-Modulation (PSM) technique is proposed for an Active-Bridge-Active-Clamp (ABAC) topology. This topology is aimed for high power more-electric-aircraft applications. The proposed PSM has a complete switching harmonics cancellation on the low voltage terminal, independently of the operating conditions by effectively interleaving inductor currents. This results in a DC current at the low voltage terminal without any AC components, thus minimizing the passive filtering requirements. Additionally, when terminal voltages vary from their nominal values, the maximum power transfer capability of the ABAC converter can be greatly improved by using the proposed PSM. In this paper, the limitations of the conventional modulation technique for the ABAC converter are introduced and analysed. Then, a PSM scheme is proposed, which can provide high quality power on the low voltage terminal whilst maintaining high power transfer capability and efficiency in a wide operating range. The theoretical claims are validated by both simulation and experimental results on a 10kW 270V/28V ABAC converter.**

***Index Terms*— Isolated DC-DC converter, Current-Fed Dual Active Bridge (CF-DAB), Active-Bridge-Active-Clamp (ABAC) converter.**

I. Introduction

A DC voltage level of 270V is currently being adopted in modern civil aircrafts like, for example, the Airbus A380 and the Boeing B-787 and in fighters like the Lockheed Martin F-35. Many large aircrafts use a combination of voltage levels, with 28VDC frequently being used to power critical loads, such as avionics [1]. Therefore, a high step up/down DC/DC converter is needed to interface the high and low DC buses. Amongst other DC/DC converters [2], the Dual-Active-Bridge (DAB) is often investigated for its bidirectional power flow and galvanic isolation [3]. The DAB also features high efficiency when input and output voltages are kept at their nominal values. This is benefited from the inherent Zero Voltage Switching (ZVS) in all the semiconductor devices [4]. However, large current ripple is expected on the Low Voltage (LV) converter terminal [5]. This poses requirement for large passive filters. In addition, active suppression techniques are required to mitigate potential resonances between LV terminal and LV source/load [6].

Different topologies derived from the DAB concept have been extensively studied. A series resonant DC/DC converter is analysed in [7], where all the switches can achieve both ZVS and Zero Current Switching (ZCS). A hybrid between a LLC resonant and a DAB converter is proposed in [8], where the LLC is responsible for low power operation while the DAB contributes to the high power range. Tapped transformer and resonant tanks are employed in [9] to widen ZVS range. A fixed-frequency controlled series-resonant converter and its centre aligned modulation are studied in [10], which decouples the voltage gain from operating power and frequency. However, none of the research contributions mentioned above can deal with the LV current ripple effectively. To cope with the stringent power quality requirement in More-Electric-Aircraft (MEA), a DC inductor can be connected in series to the LV bridge [11] to suppress the current ripple. However, this poses difficulties in current commutation. Therefore, instead of configuring the inductor in series to the LV bus, it can be placed between the pole of the LV bridge and LV source/load. A soft-switched bidirectional half-bridge DC-DC converter is proposed in [12]. This configuration not only can reduce the current ripple on the LV terminal, but can also increase the voltage step up/down capability, making the transformer easier to design. However, capacitors in the half bridge circuit need to handle the current flowing through the transformer. This requires capacitors with large current rating, thus making the topology less attractive in high power applications. Additionally, two inductors can be placed between LV source/load and LV bridge poles, and they are interleaved at the LV terminal [13]–[15]. This type of current-fed DAB converter can provide interleaved current paths on the LV terminal, reducing requirement for passive filtering. The S-DAB topology proposed in [16] features also an interleaved structure, which incorporates two half bridges on the LV side. Diodes are used to achieve zero current switching (ZCS). In this configuration, DC transformer bias can be naturally suppressed without applying active controls [17], [18].

In this paper, a topology named Active-Bridge-Active-Clamp (ABAC) is introduced. It is a viable alternative to classical DAB in MEA applications [15], [19]. The term "active bridge" refers to the H-bridge on the primary side of the transformer, and "active clamps" describes the four half bridge clamp circuits on the secondary. The ABAC topology provides bidirectional power transfer capability and extra degrees of

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freedom to effectively cancel the LV terminal current ripple. In fact, when the single secondary winding structure of the ABAC converter is considered for high power low voltage applications, the high current on the LV side requires the paralleling of semiconductor devices. Alternatively, an increased number of transformer secondaries can be introduced to reduce the current stress in each switching devices, thus reducing the requirements in terms of paralleling active devices. Thus, when the ABAC converter is considered for high power applications, a dual transformer secondary structure can be adopted. It is important to highlight that this configuration does not increase the number of active devices with respect to a single secondary structure at the same power rating. However, it provides an extra degree of freedom which can be used to thoroughly cancel switching harmonics on the LV terminal current in all operating conditions.

In fact, past investigations on modulation for similar converters mainly focused on Phase-Shifting-Pulse-Width-Modulation (PS-PWM) techniques. In [20], the phase shifts between the LV side half bridges are fixed at 180 degree while the duty cycles vary in order to control the clamp voltages. The clamp voltages determine the voltage magnitude of the quasi-square wave on the transformer LV port. Voltage magnitude on the transformer LV port is manipulated to match with the transformer HV port value to enhance the efficiency. Moreover, authors in [21] proposed an alternative PS-PWM technique where a fixed deviation is imposed between the duty cycles for HV and LV bridges to achieve wider ZVS regions. Authors in [22] introduced another degree of freedom by controlling the duty cycle of the HV bridges independently of LV bridges, with the aim of optimising the transformer current. Furthermore, The work presented in [16] adapts the concept of trapezoidal current modulation usually used in a DAB [23] to a current-fed type. However, in this approach. maximum power transfer capability [24] is limited. Additionally, authors in [25] carried out an optimization on transformer RMS current by breaking the clamp voltage matching principle investigated in [20]. However, common issues with above mentioned PS-PWM methods are increased LV current ripple and limited power transfer capability when the terminal voltages vary from their nominal values.

With the aim of providing a current-fed, bidirectional and isolated solution which is able to retain the aforementioned advantages of DAB, the Active Bridge Active Clamp (ABAC) converter with a dual secondary structure, shown in Figure 1, is introduced in this paper. The dual secondary structure of the ABAC provides enhanced LV terminal current quality at all operating points. A Phase-Shift-Modulation (PSM) technique is proposed in this paper with the goal of supplying a pure DC LV terminal current without AC components even before being filtered by the LV capacitors. The proposed PSM maintains the switching duty cycles at 50% of the sampling interval. It splits and shifts the active states of devices in one switching period to achieve complementary switching between the two secondaries. As a result, the proposed PSM is able to obtain complete inductor current interleaving. For this reason, it can achieve higher power transfer capability with respect to classical PS-PWM. On the other hand, PSM can cause higher transformer current stress when compared to PS-PWM. Hence, an optimisation of transformer current stress is also carried out with the proposed PSM technique. Closed-form expressions of operating phase shifts trajectories are derived. Consequently, efficiency can be improved, especially when HV and LV voltages vary from their nominal values. For this reason, a ZVS analysis is also carried out for the proposed converter, identifying factors that affect the soft switching region.

The main contribution of this paper can be summarised as follow: 1) Drawbacks of conventional PS-PWM techniques for current-fed DAB are quantitatively analysed; 2) A PSM modulation technique is proposed for the dual secondary ABAC converter; 3) Transformer current stress and ZVS region analysis are carried out for the proposed PSM technique. It is also important to highlight that the proposed approach can be still applied to other current-fed topologies [13]–[16] in order to expands their maximum power capability when operating in voltage conditions which differ from their nominal values. In addition, when enough degrees of freedom are provided, complete current ripple cancellation can be achieved with the proposed method.

The paper is structured as follows: in Section II, the ABAC operated with PS-PWM is described, and the issue of increased LV current harmonics when DC voltages are not at the nominal values is analysed. In Section III, a PSM technique is proposed that overcomes the limitations of PS-PWM. Operation analysis is conducted, and maximum power transfer capabilities of both PSM and PS-PWM are derived and compared. Moreover, transformer current stress is optimised, and a closed-form expression of the operation trajectories is derived. Finally, ZVS constraints for the ABAC converter are derived and discussed. Simulation and experimental results are presented for a 10-kW ABAC, reported in Section V and Section VI, respectively.

II. ABAC CONVERTER STRUCTURE AND CONVENTIONAL MODULATION TECHNIQUE

The ABAC topology is presented in Figure 1. A three port high frequency transformer with turn ratio N:1 is used. A full bridge circuit, associated with the high voltage side of the converter is connected to the primary winding of the transformer and generates the voltage v_{ac1}. On the low voltage side of the transformer, two interleaved half bridge clamp circuits are connected to each secondary through power transfer inductors L_s. The two secondary circuits are able to work independently, generating different voltages, v_{ac2} and v_{ac3}. However, in applications where equal power sharing is required between the two secondary ports, the condition $v_{ac2} = v_{ac3}$ is imposed. C_c are the clamp capacitors which serve as energy buffer between the transformer and the LV load. L_o are the output filter inductors, used to suppress the current ripple. Finally, the LV current I_{LV} is filtered by LV capacitor C_o before flowing into the LV load R_L.

There are several modulation schemes available for the ABAC converter [16], [22]. However these techniques present two main issues when V_{HV} or V_{LV} vary far from their nominal operating values. The first issue is that maximum power transfer capability is reduced. This will be discussed in section III.B. Another issues is that they present large current ripple on I_{LV}, which can increase the requirement on passive filtering and potentially introduce resonance between the LV terminal and the LV source/loads [6]. As an example, one of the PS-PWM

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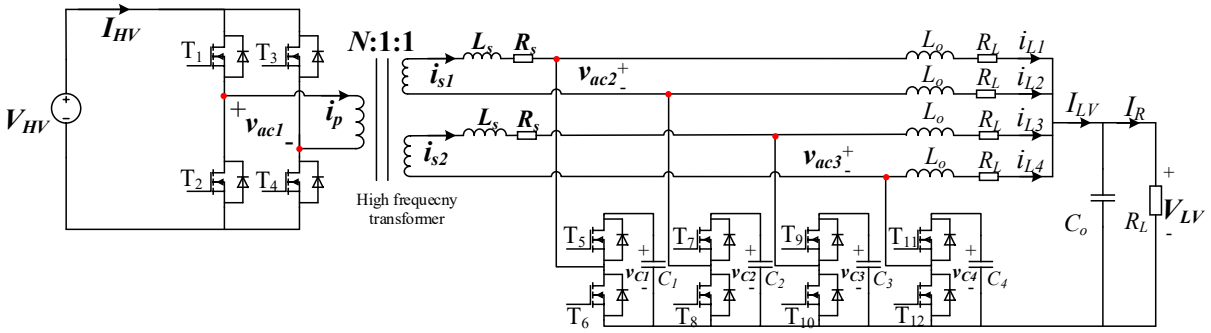

Figure 1: The ABAC converter topology with a dual secondary structure.

techniques [20] is discussed herein for the ABAC converter as depicted in Figure 2.

Considering the structure of the ABAC converter in Figure 1, the power transfer inductance L_s is placed on the LV side in order to provide decoupling between the two transformer secondaries. Due to this design constraint, in high power applications the value of L_s is usually of few hundreds of nH [15]. As a consequence, inductance with litz wires [26], in combination with the leakage inductance of the transformer can be used to implement the power transfer inductance.

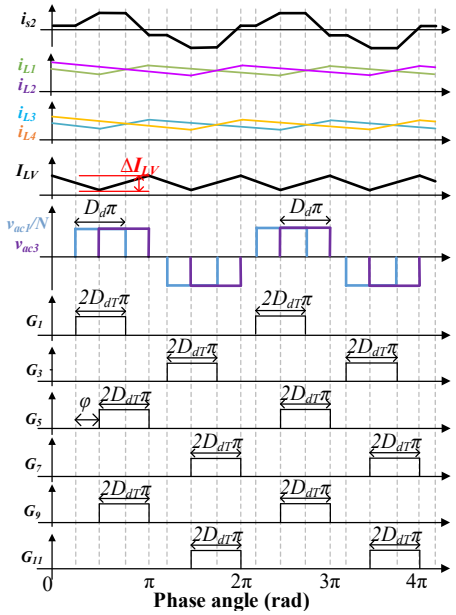

Figure 2: Conceptual waveforms for the PS-PWM scheme in the ABAC converter where D_{dT} is the duty cycle of switches. G_1-G_{12} drive T_1-T_{12} with $G_4=G_1$, $G_2=G_3=not(G_1)$, $G_6=not(G_5)$, $G_8=not(G_7)$, $G_{10}=not(G_9)$ and $G_{12}=not(G_{11})$. $0< D_{dT}<0.5$.

In the PS-PWM scheme shown in Figure 2, the inner phase shift between G_1 and G_3, G_5 and G_7, and G_9 and G_{11}, is always fixed at π. Therefore, LV inductor current pair i_{L1}, i_{L2} and i_{L3}, i_{L4} are interleaved with a phase shift of π. The outer phase shift φ between G_1 and G_5 (G_9) is used to control power transferred between transformer primary and secondary ports. The duty cycles of all switches are fixed at D_{dT}. Referring to Figure 2, the relationships between duty cycle of the transformer quasi-square wave voltages D_d and duty cycle of switches D_{dT} are expressed as follow

$$D_d = \begin{cases} 2D_{dT}, & 0 < D_{dT} < 0.5 \\ 2(1-D_{dT}), & 0.5 < D_{dT} < 1 \end{cases} \tag{1}$$

Clamp voltages (v_{c1}-v_{c4}) are controlled by the duty cycle D_{dT}. If clamp voltages are designed to match with the primary transformer voltage magnitude V_{HV}/N, the voltage ratio r_V can be calculated as

$$r_V = \frac{NV_{LV}}{V_{HV}} = D_{dT} \tag{2}$$

The use of PS-PWM can reduce the transformer current stress and its RMS value [22]. Additionally, Zero Voltage Switching (ZVS) operating region can also be expanded [21]. When D_{dT}=0.5, the current ripples on LV currents i_{L1}-i_{L4} are well cancelled and I_{LV} is free of switching ripple. However, when $D_{dT}\neq$0.5 as shown in Figure 2, the current ripple cancellation for i_{L1}-i_{L4} is compromised. Analysis is carried out here to evaluate the peak-to-peak variation of current I_{LV} when $D_{dT}\neq$0.5. In steady state the following equations are satisfied:

$$I_{LV}(\pi) = \sum_{n=1}^{4} i_{Ln}(\pi) \tag{3}$$

$$I_{LV}(\pi) = \overline{I_{LV}} + \frac{\Delta I_{LV}}{2} \tag{4}$$

$$i_{Ln}(\pi) = \frac{\overline{I_{LV}}}{4} + \frac{V_{HV}/N - V_{LV}}{L_o}\frac{D_{dT}}{2f_s}; n = 1,3 \tag{5}$$

$$i_{Ln}(\pi) = \frac{\overline{I_{LV}}}{4} - \frac{V_{LV}}{L_o}\frac{D_{dT}}{2f_s}; n = 2,4 \tag{6}$$

where $\overline{I_{LV}}$ is the DC component of the load current I_{LV}, and f_s is the switching frequency. L_o is the LV side output filter inductance. Substituting equations (2), (4)-(6) into (3), and conducting similar calculations for operation $0.5<D_{dT}<1$, expressions for ΔI_{LV} are reported in (7)

$$\Delta I_{LV} = \begin{cases} \left| \frac{2V_{LV}}{L_o f_s}\left(1 - 2\frac{NV_{LV}}{V_{HV}}\right) \right|, & \text{when } \frac{NV_{LV}}{V_{HV}} \le 0.5 \\ \left| \frac{2(V_{HV}/N - V_{LV})}{L_o f_s}\left(2\frac{NV_{LV}}{V_{HV}} - 1\right) \right|, & \text{when } \frac{NV_{LV}}{V_{HV}} > 0.5 \end{cases} \tag{7}$$

According to equation (7), transformer turn ratio N is usually designed to match the following condition

$$V^*_{HV} = 2NV^*_{LV} \tag{8}$$

where, V^*_{HV} and V^*_{LV} are nominal voltages. In this case, ΔI_{LV} is equal to zero. It can also be observed from equation (7) that ΔI_{LV} is increased when V_{HV} or V_{LV} vary from their nominal values.

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This results in higher requirement for LV side passive filters to suppress the harmonics from propagating into LV terminal DC networks.

III. The Proposed Modulation Technique

In order to solve the issues discussed in the previous section, a phase shift based modulation scheme is introduced in [27]. However, this method may present DC offset to transformer and deviation to inductor current DC values when applied to the ABAC converter. Therefore, an improved Phase-Shift-Modulation (PSM) is proposed here as shown in Figure 3. The duty cycle of the switches is fixed at 50% irrespective of the converter voltages and power. As can be seen from Figure 3 and considering G_7 as an example, the sum of the active period in one switching cycle is π. The active time of G_7 is split into two parts in period θ_7- θ_{15}. The first part is shifted to the start of this switching period while the second part is shifted to the end of this switching period. Therefore, signals G_7 and G_9 are complementary. It is important to highlight that since the switches T_7 (driven by signal G_7) and T_9 (driven by signal G_9) are always complementarily switched, therefore the LV currents i_{L2} and i_{L3} are always interleaved. The same behaviour can be observed on switches T_5 and T_{11}. Therefore, I_{LV} is ripple-free at any operating points. However, the inductor currents have now an increased period of $2T_s$ in the proposed PSM, as the shape of the inductor currents is defined by the gating signals G_5-G_{11}. In addition, the clamp circuits determine the transformer secondary port voltages v_{ac2} and v_{ac3}. In particular, G_5, G_7 and G_9, G_{11} are used to generate v_{ac2} and v_{ac3}, respectively. According to the driving signals, the transformer secondary voltage v_{ac2} can be generated as $v_{ac2} = v_{c1}G_5 - v_{c2}G_7$, while the phase shift value φ is related to the phase shift between G_1 and G_5. From Figure 3, it can be noted that, in half switching cycle, the pulse duration in both voltages v_{ac1} and v_{ac3} (v_{ac2}) present the same value of πD_d, where D_d can vary from 0 to 1. On the other hand, the outer phase shift between transformer primary and secondary voltages, φ, can vary from 0 to 2π. With this modulation scheme, D_d and φ can be independently controlled in order to optimise the operation of the converter.

There are many ways to generate the gating signals for LV side switches. The proposed PSM requires the generation of variable phases for LV side bridges between two adjacent switching periods. The proposed gating signal generation is shown in Figure 4 where counters for each EPWM module are independently driven. Counters are compared with a fixed value equal to 50% of the counter maximum C_{max} to generate on/off signals G_1-G_{12}. EPWM4-EPWM7 are responsible for generating the driving signals for the secondary switches T_5-T_{12}, respectively. Since each leg is complementarily switched, only the gates of the upper switches in each half bridge are shown in Figure 4. The red dashed lines in Figure 4 represent the boundary, where phase updates are taken place. Phase updating values for each EPWM counters are listed in TABLE I where $\delta = \pi(1-D_d)$ is the zero voltage state on v_{ac2}/v_{ac3}. It can be noted that EPWM4A (G_5) and EPWM7A (G_{11}) always have a phase difference of π, as the same for EPWM5A (G_7) and EPWM6A (G_9). Therefore, 180 degree phase shifts between i_{L1} and i_{L4} also i_{L2} and i_{L3} are guaranteed and comprehensive LV terminal current ripple cancellation can be achieved.

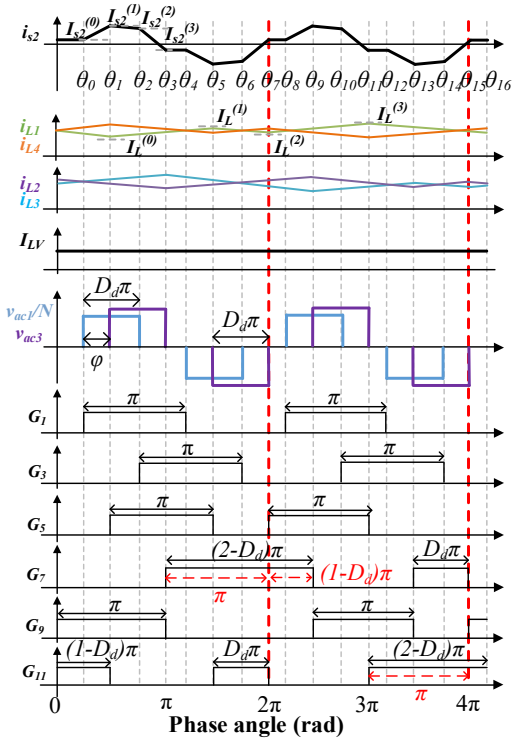

Figure 3: Typical waveforms for operation $0<\varphi/\pi<\text{Min}\{1-D_d, D_d\}$ (mode IV) using the proposed PSM scheme where G_1-G_{12} drive T_1-T_{12} with $G_4=G_1$, $G_2=G_3=not(G_1)$, $G_6=not(G_5)$, $G_8=not(G_7)$, $G_{10}=not(G_9)$ and $G_{12}=not(G_{11})$. Operating modes I - IV are discussed below in *"A. Operation analysis"* and summarised in Table II.

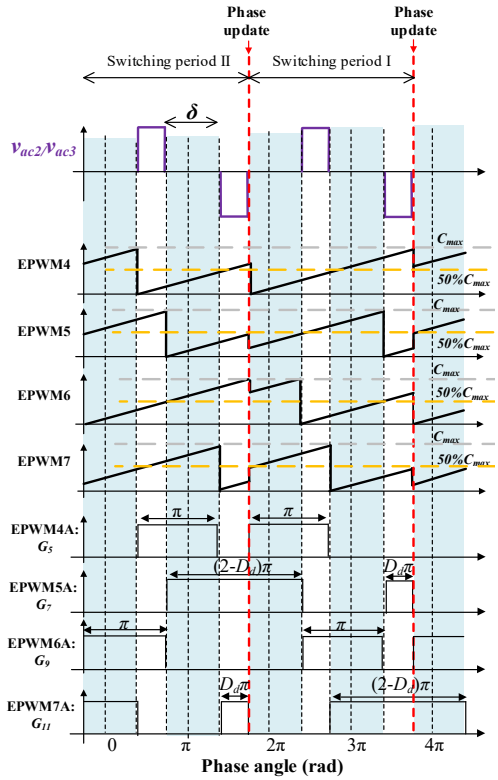

Figure 4: Generation of the switching signals by only phase shifting the carriers.

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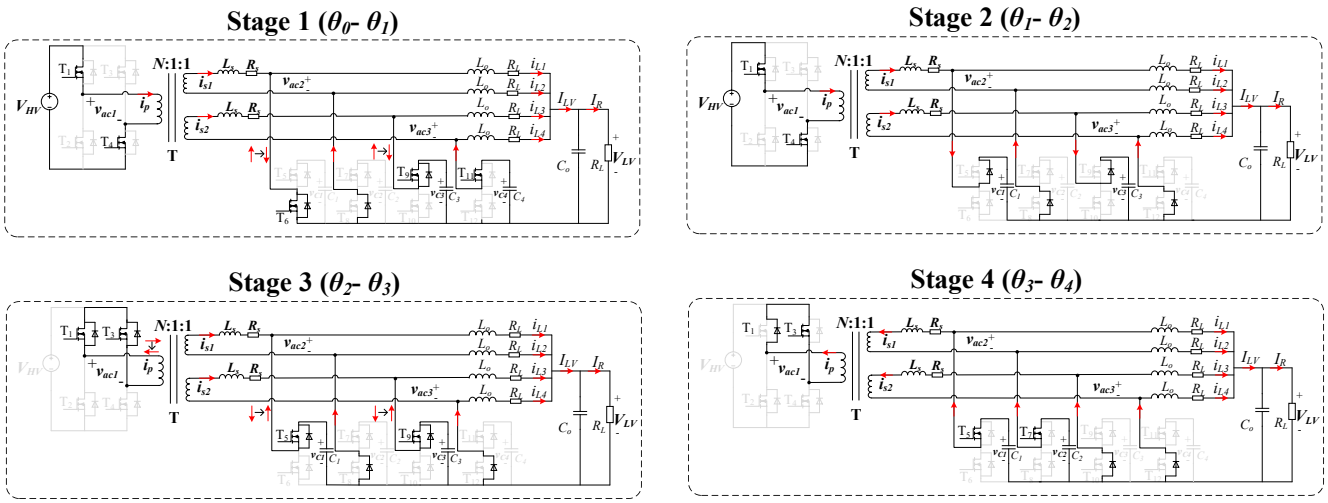

Figure 5: Equivalent circuits in Mode IV

TABLE II:SUMMARY OF MODES IN BUCK OPERATION

Modes	Constraints	$P(D_d, D_\varphi)$	$i_{s2}(\theta_0)$
I	$D_d < \frac{\varphi}{\pi} < 1-D_d$	$2D_d^2$	$D_d(1-\frac{1}{2r_V})$
II	$Max\{1-D_d, D_d\} \le \frac{\varphi}{\pi} \le 1$	$2[2D_d+2\frac{\varphi}{\pi}-2D_d\frac{\varphi}{\pi}-(\frac{\varphi}{\pi})^2-1]$	$2-2\frac{\varphi}{\pi}-D_d\left(1+\frac{1}{2r_V}\right)$
III	$1-D_d < \frac{\varphi}{\pi} < D_d$	$2[2D_d-D_d^2+2\frac{\varphi}{\pi}-2(\frac{\varphi}{\pi})^2-1]$	$2-2\frac{\varphi}{\pi}-D_d(1+\frac{1}{2r_V})$
IV	$0 \le \frac{\varphi}{\pi} \le Min\{1-D_d, D_d\}$	$2[2D_d\frac{\varphi}{\pi}-(\frac{\varphi}{\pi})^2]$	$(1-\frac{1}{2r_V})D_d$

Modes	$i_{s2}(\theta_1)$	$i_{s2}(\theta_2)$	$i_{s2}(\theta_3)$
I	$D_d(1+\frac{1}{2r_V})$	$D_d(1+\frac{1}{2r_V})$	$\frac{1}{2}D_d(\frac{1}{r_V}-2)$
II	$\frac{1}{2r_V}(2\frac{\varphi}{\pi}+D_d-2)+D_d$	$D_d(1+\frac{1}{2r_V})$	$D_d(1+\frac{1}{2r_V})$
III	$\frac{1}{2r_V}(D_d+2\varphi/\pi-2)+D_d$	$D_d+(\frac{\varphi}{\pi}-\frac{D_d}{2})\frac{1}{r_V}$	$2\frac{\varphi}{\pi}+\frac{1}{2}D_d\left(\frac{1}{r_V}-2\right)$
IV	$D_d+(\frac{\varphi}{\pi}-\frac{D_d}{2})\frac{1}{r_V}$	$2\frac{\varphi}{\pi}+\frac{1}{2}D_d\left(\frac{1}{r_V}-2\right)$	$\frac{1}{2}D_d\left(\frac{1}{r_V}-2\right)$

TABLE I
COUNTER UPDATING VALUES FOR EACH EPWM MODULES

SWITCHING PERIOD	I	II
EPWM4A	0	δ
EPWM5A	$\delta+\pi$	π
EPWM6A	δ	0
EPWM7A	π	$\delta+\pi$

The main difference between proposed PSM and PS-PWM can be summarised as follow. In the proposed PSM scheme, the duty cycle over one switching period for the LV side clamp switches is fixed at 50% and the clamp circuits operate similarly to an interleaved boost converter. Thus, at steady state, $V_c = 2V_{LV}$ can always be obtained. The asymmetrical duty cycle of T_7 and T_{11} is complementary to the duty cycle of T_9 and T_5. As a result, inductor currents i_{L1}-i_{L4} present complementary AC components and complete ripple cancellation. On the other hand, using the classical PS-PWM method, the duty cycle of the LV side switches are used to control the clamp voltages accordingly to the variation of the HV terminal voltage V_{HV}. This result in different power transfer capability and LV terminal current quality when the two modulation techniques are compared, as shown in the following subsections.

A. Operation analysis

Due to the two degrees of freedom available, four operating modes are possible as shown in Table II. As an example, operating mode IV is taken into consideration during the analysis, accordingly to the waveforms shown in Figure 3 (a). Since the transformer current i_{s2} is symmetrical, only half of the switching cycle, from θ_0- θ_4 in Figure 3(a), is analysed. A typical operation stage analysis in Mode IV with equivalent circuits is shown in Figure 5.

The analysis considers switches with no parasitic capacitances and dead times, and stages are described as follows:

Stage 1 (θ_0- θ_1): At θ_0, T_1 is switched on while T_2 is switched off. Current is commuted from the body diode of T_2 to T_1. With

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the increase of i_{s2}, natural commutation happens from the body diode of T_6 to T_6 and also from T_9 to its body diode. During this period, the transformer secondary current $i_{s2}(\theta)$ can be calculated as:

$$i_{s2}(\theta) = i_{s2}(\theta_0) + \frac{V_{HV}}{2\pi N f_s L_s}(\theta - \theta_0) \tag{9}$$

Stage 2 (θ_1- θ_2): At θ_1, T_5/T_{12} is switched on while T_6/T_{11} is switched off. Current is commuted from T_6 to the body diode of T_5 and from T_{11} to the body diode of T_{12}, hence T_5 and T_{12} are soft switched. During this period, the transformer secondary current $i_{s2}(\theta)$ can be calculated as:

$$i_{s2}(\theta) = i_{s2}(\theta_1) + \frac{\frac{V_{HV}}{N} - V_c}{2\pi f_s L_s}(\theta - \theta_1) \tag{10}$$

where V_c is the clamp capacitors voltage in steady state.

Stage 3 (θ_2- θ_3): At θ_2, T_3 is switched on while T_4 is switched off. Current is commuted from T_4 to the body diode of T_3, hence T_3 is soft switched. With the decreasing of i_{s2}, natural commutation happens from T_3/T_5/T_9 body diode to T_3/T_5/T_9. During this period, the transformer secondary current $i_{s2}(\theta)$ can be calculated as:

$$i_{s2}(\theta) = i_{s2}(\theta_2) - \frac{V_c}{2\pi f_s L_s}(\theta - \theta_2) \tag{11}$$

Stage 4 (θ_3- θ_4): At θ_3, T_7/T_{10} is switched on while T_8/T_9 is switched off. Current is commuted from the body diode of T_8 to T_7. Current is also commuted from T_9 to T_{10} body diode, hence T_{10} is soft switched. During this period, the transformer secondary current $i_{s2}(\theta)$ remains unchanged. Therefore:

$$i_{s2}(\theta) = i_{s2}(\theta_3) \tag{12}$$

Due to symmetrical operation:

$$i_{s2}(\theta_0) = -i_{s2}(\theta_4) \tag{13}$$

Then, substituting (9)-(12) into (13), currents $i_{s2}(\theta_0)$-$i_{s2}(\theta_4)$ are derived and summarised in Table II. The power transferred for a dual secondary structure can be calculated as:

$$P(D_d, D_\varphi) = \frac{4}{T_s}\int_{\theta_0}^{\theta_4} i_{s2}(\theta) v_{ac3}(\theta) d\theta \tag{14}$$

where D_φ is defined as φ/π.

Furthermore, by imposing constraints (1) and (2), results in Table II are also applicable to PS-PWM, shown in Figure 2.

The transferred power is expressed in per-unit with the base power P_{base} defined as:

$$P_{base} = \frac{V_{HV} V_C}{4 N f_s L_s} \tag{15}$$

Where conditions $V_c = V_{HV}/N$ and $V_c = 2V_{LV}$ are applied to PS-PWM and PSM, respectively, the base power for the two modulations under analysis are:

$$P_{base(PS-PWM)} = \frac{V_{HV}^2}{4 N^2 f_s L_s} \tag{16}$$

$$P_{base(PSM)} = \frac{V_{HV} V_{LV}}{2 N f_s L_s} \tag{17}$$

Similarly, the LV side currents can be expressed in per-unit, with the base I_{base} defined as:

$$I_{base} = \frac{V_{LV}}{2 f_s L_s} \tag{18}$$

Similar calculations can also be conducted for other modes (I, II and III), and results for buck operation (power transferred from the HV bus to the LV bus) are summarised in Table II. For boost operation, the same approach can be applied. However, detailed analysis is omitted in this paper for brevity.

B. Maximum power transfer analysis

The power contour plot $P(D_d, D_\varphi)$ for the ABAC converter is shown in Figure 6 according to Table II, considering all four modes of buck operation. When $D_d = 1$, $\varphi = \pi/2$, maximum power can be delivered using PSM. On the other hand, when the ABAC converter is modulated with PS-PWM, D_d is related to the voltage ratio r_V as indicated in equations (1) and (2). For such reason the condition $D_d = 1$ is not always achievable for PS-PWM.

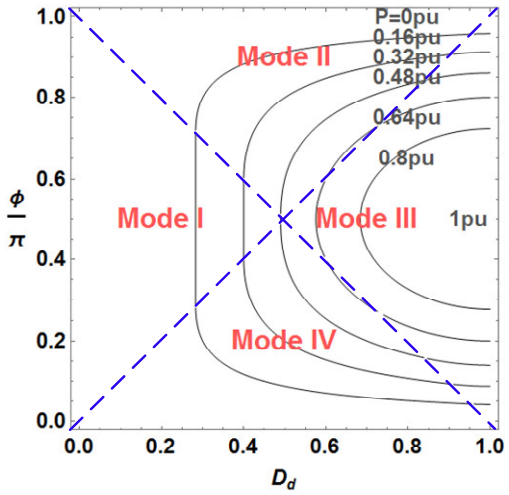

Figure 6: Power contour plot of the ABAC converter.

Referring to Figure 6, the maximum transfer power for both modulations can be expressed as in (19) and (20) by combining equations (1), (2), (16), (17) with the expressions in Table II.

$$P_{\max(PSM)} = P(1, 0.5) P_{base(PSM)} = \frac{V_{LV}^2}{2 f_s L_s r_V} \tag{19}$$

$$P_{\max(PS-PWM)} = P(D_d, 0.5) P_{base(PS-PWM)} = \begin{cases} \dfrac{2V_{LV}^2}{f_s L_s} & ,0 < r_V < 0.25 \\ \dfrac{2V_{LV}^2 (r_V - r_V^2 - 0.125)}{f_s L_s r_V^2} & ,0.25 < r_V < 0.75 \\ \dfrac{2V_{LV}^2 (r_V - 1)^2}{f_s L_s r_V^2} & ,0.75 < r_V < 1 \end{cases} \tag{20}$$

In order to compare power transfer capability of the two modulations under analysis, a maximum power ratio is defined in (21) as the ratio between the maximum power achievable with PS-PWM and PWM considering the same design parameters, respectively.

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$$P_r = \frac{P_{\max(PS\_PWM)}}{P_{\max(PSM)}} = \begin{cases} 4r_V & ,0 \le r_V < 0.25 \\ 4 - \dfrac{1}{2r_V} - 4r_V & ,0.25 \le r_V < 0.75 \\ 4(1-r_V)^2 / r_V & ,0.75 \le r_V < 1 \end{cases} \quad (21)$$

The same equation is plotted in Figure 7 as a function of the voltage ratio r_V. The PSM approach has the ability to deliver more power than PS-PWM when r_V is lower than 0.25 or higher than 0.5.

The ability of providing full power over a wide operating range is a key requirement in aerospace applications. For example, when the More Electric Aircraft concept is considered, the bus voltages may present wide variations with the voltage ratio r_V typically having a range from 0.36 to 1. In fact, the EN2282 standard is usually considered for the LV bus, with voltage variations ranging from 22V to 30V. For the HV DC bus, standard MIL-STD-704 describes a normal operating condition range of 250V to 300V. However, the voltage variation can be even larger, since standards are currently under definition for civil more electric aircraft and converter operation with degraded performances may be required at lower voltage values. Additionally, the converter has to be able to provide the full power for a certain amount of time when a short circuit fault happens on DC buses to allow the circuit breakers to operate [28], [29]. This requirements can also be applied to Solid State Power Controllers (SSPC), as for example the SPDC130D28 from Sensitron Semiconductor [30], which usually use its I^2t curve to trip operations in case of fault. In presence of DC short circuit fault, the DC bus voltage will drop, and it is essential for the ABAC converter to still be able to provide enough current to allow the SSPC to operate properly.

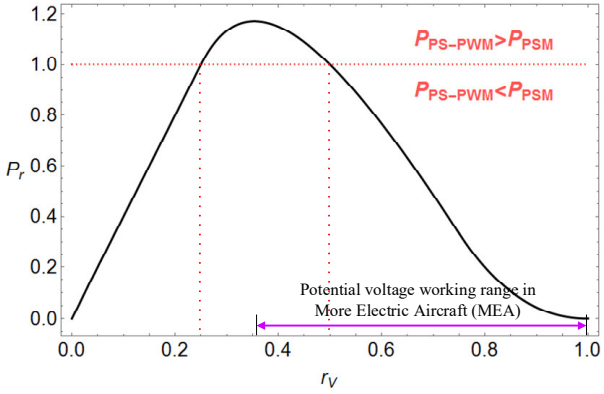

Figure 7: Power ratio P_r plot against the voltage ratio r_V.

C. Current stress minimisation

It can be observed from Figure 6 that there are several combinations of D_d and φ/π able to transfer the same power through the converter. This redundancy allows to obtain higher efficiency and power density if optimised solutions are considered. Amongst all the possible targets for this optimisation, the transformer current peak value represents a viable parameter to minimise in order to achieve higher efficiency and reduce the HF transformer weight and volume. The transformer current peak value is defined as:

$$I_{peak} = Max\{|i_{s2}(\theta_0)|, |i_{s2}(\theta_1)|, |i_{s2}(\theta_2)|, |i_{s2}(\theta_3)|\} \quad (22)$$

Based on equation (22), the transformer current peak value is minimised as follows:

$$Objective: Min\ I_{peak} \qquad Subject\ to: \begin{cases} 0 < \varphi < \pi \\ 0 < D_d < 1 \\ P_{ref} = P(D_d, \varphi/\pi) \end{cases} \quad (23)$$

The obtained results for buck operation are expressed in equations (24) and (25).

The minimised transformer current peak value trajectories are plotted in Figure 8 together with the normalised power contour. In operation modes I and II (illustrated in Figure 6), high current stress on the transformer can be noted. Therefore, operation in these two modes is avoided following the designed trajectories. All the trajectories are confined within operation modes III and IV, characterised by lower transformer current peak value. When HV and LV match ($r_V = 0.5$), the minimum current stress trajectory coincides with the line $D_d = 1$, indicating that the Phase-Shift-Modulated-Single-Phase-Shift (PSM-SPS), also known as "$D_d = 1$ mode" in [25], can achieve minimal current stress. With the variation of r_V from 0.5, the minimum transformer current stress trajectory shows different trends. Figure 8 considers only buck operations ($\varphi > 0$). However when boost operation ($\varphi < 0$) is considered symmetrical trajectories, with respect to the x axis of Figure 8, can be obtained.

$$D_d = \begin{cases} \dfrac{2r_V + 1}{2r_V - 1}\dfrac{\varphi}{\pi}, & \dfrac{\varphi}{\pi} < \dfrac{2r_V - 1}{4r_V} \\ (2r_V - 1)\dfrac{\varphi}{\pi} + \dfrac{3 - 2r_V}{2}, & \dfrac{\varphi}{\pi} > \dfrac{2r_V - 1}{4r_V} \end{cases} \text{, when } r_V > 0.5 \quad (24)$$

$$D_d = \begin{cases} \dfrac{1 + 2r_V}{1 - 2r_V}\dfrac{\varphi}{\pi}, & \dfrac{\varphi}{\pi} < \dfrac{1 - 2r_V}{2} \\ \dfrac{2(1 - 2r_V)}{4r_V}\dfrac{\varphi}{\pi} + \dfrac{6r_V - 1}{4r_V}, & \dfrac{\varphi}{\pi} > \dfrac{1 - 2r_V}{2} \end{cases} \text{, when } r_V < 0.5 \quad (25)$$

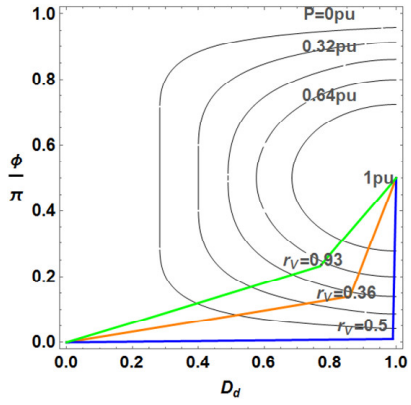

Figure 8: Minimum current stress trajectories with different voltage ratio r_V.

D. Zero Voltage Switching (ZVS) analysis

To simplify the ZVS analysis, the dead time is neglected, as well as the parasitic capacitances of the devices. Therefore, in this approximated analysis, ZVS occurs when the current flows through the body diode of the device when turning it on. Thus, constraints to achieve ZVS for both HV and LV bridges are summarised in Table III where $I_{s2}^{(0)}$-$I_{s2}^{(3)}$ are normalised variables, representing secondary transformer current values at the switching instants as illustrated in Figure 3.

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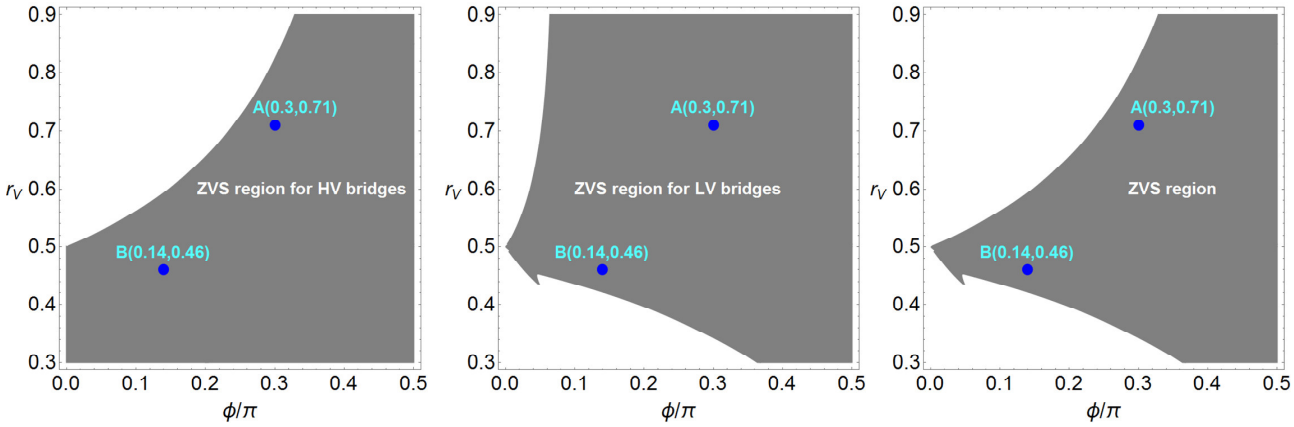

(a) (b) (c)

Figure 9: ZVS regions when operating on the minimum transformer current trajectory with m=3.3 for (a) HV bridges, (b) LV bridges and (c) overall converter.

TABLE III
ZVS CONSTRAINTS FOR BOTH HV AND LV BRIDGES

		Mode III	Mode IV
HV	T_1,T_2	$I_{s2}^{(0)}<0$	
	T_3,T_4	$I_{s2}^{(3)}>0$	$I_{s2}^{(2)}>0$
LV	T_5,T_9	$I_{s2}^{(2)}> I_L^{(0)}$ $I_{s2}^{(1)}> I_L^{(2)}$	$I_{s2}^{(1)}> I_L^{(0)}$ $-I_{s2}^{(3)}> I_L^{(2)}$
	T_7,T_{11}	$I_{s2}^{(1)}> I_L^{(0)}$ $I_{s2}^{(2)}> I_L^{(2)}$	$I_{s2}^{(1)}> I_L^{(2)}$ $-I_{s2}^{(3)}> I_L^{(0)}$
	T_6,T_{10}	$-I_{s2}^{(2)}< I_L^{(1)}$ $-I_{s2}^{(1)}< I_L^{(3)}$	$-I_{s2}^{(1)}<I_L^{(1)}$ $I_{s2}^{(3)}<I_L^{(3)}$
	T_8,T_{12}	$-I_{s2}^{(1)}< I_L^{(1)}$ $-I_{s2}^{(2)}< I_L^{(3)}$	$-I_{s2}^{(1)}< I_L^{(3)}$ $I_{s2}^{(3)}< I_L^{(1)}$

The utilisation of the PSM scheme leads to expressions of the inductor current that are different from the ones proposed in [14]. Therefore, inductor current i_{L1}-i_{L4} values at switching instances are calculated as follows:

$$\begin{cases} I_L^{(0)} = i_{L1}(\theta_1) = i_{L2}(\theta_3) = i_{L3}(\theta_9) = i_{L4}(\theta_{11}) \\ \quad = \dfrac{mP(D_d, \frac{\varphi}{\pi}) + 2r_V(D_d - 2)}{4mr_V} \\ I_L^{(1)} = i_{L1}(\theta_5) = i_{L2}(\theta_{15}) = i_{L3}(\theta_{13}) = i_{L4}(\theta_7) \\ \quad = \dfrac{mP(D_d, \frac{\varphi}{\pi}) + 2r_V D_d}{4mr_V} \\ I_L^{(2)} = i_{L1}(\theta_7) = i_{L2}(\theta_{13}) = i_{L3}(\theta_{15}) = i_{L4}(\theta_5) \\ \quad = \dfrac{mP(D_d, \frac{\varphi}{\pi}) - 2r_V D_d}{4mr_V} \\ I_L^{(3)} = i_{L1}(\theta_{11}) = i_{L2}(\theta_9) = i_{L3}(\theta_3) = i_{L4}(\theta_1) \\ \quad = \dfrac{mP(D_d, \frac{\varphi}{\pi}) + 2r_V(2 - D_d)}{4mr_V} \end{cases} \quad (26)$$

where $I_L^{(0)}$-$I_L^{(3)}$ are normalised variables, representing inductor current values at switching instances as illustrated in Figure 3. Values of currents are all normalised to I_{base} as in (18), and m is defined as the ratio between output inductance and power transferring inductance

$$m = \frac{L_0}{L_s} \quad (27)$$

If the operation of the converter is assumed to follow the minimum transformer current stress trajectories, by substituting equations in Table II, (24), (25) and (26) into the ZVS constraints in Table III, the ZVS region can be derived. It is important to highlight that the ZVS regions depend only on r_V, φ and m. In Figure 9 the ZVS area is plotted as a function of r_V and φ/π, when m=3.3. The HV bridges can achieve ZVS for the whole operating range with r_V values smaller than 0.5 while LV bridges can achieve wider ZVS region for values of r_V higher than 0.5. The overlap between these two ZVS regions correspond to soft-switching of the whole converter when m equals 3.3 (practical values of L_s = 0.5μH, L_o = 1.65μH are considered) and it is shown in Figure 9 (c).

IV. SIMULATION RESULTS

The simulation diagram is shown in Figure 10. A proportional Integral (PI) controller for LV voltage regulation drives the optimised PSM scheme. In fact, even if several different control techniques can be applied to the ABAC converter, the work in this paper focus only on modulation techniques and, for such reason, a simple PI control scheme has been considered. The PI controller design has to take into account the different modes of operation and voltage ratio r_V. For example, a transition between Mode III and Mode IV results in different small signal models for the ABAC converter and, as a consequence, a different sets of PI parameters has to be considered. Similarly when the voltage ratio r_V changes, the small signal model for the ABAC converter also changes and the PI controller needs to be re-tuned. However, the control tuning does not affect the analysis carried out on the proposed modulation and, for such reason, the PI controller parameters have been empirically obtained in each operating point.

The converter parameters are listed in Table IV and correspond to those of the experimental converter discussed in section V, where P_c represents the power transfer capability under all the voltage operating conditions. Simulation results are obtained using Plexim PLECS software.

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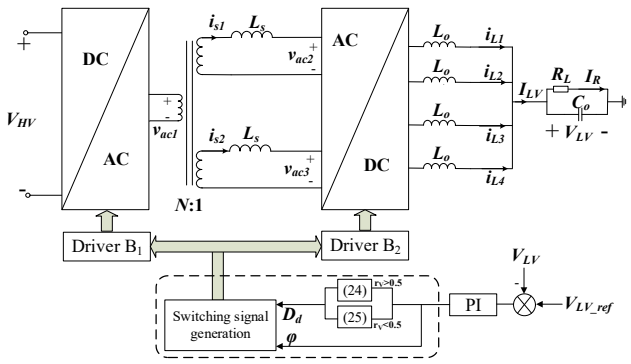

Figure 10: Block diagram of the simulated system.

TABLE IV
ABAC CONVERTER PARAMETERS

Symbol	Description	Value
V_{HV}	HV range	150-300 V
V^*_{HV}	Nominal HV voltage	270V
V_{LV}	LV range	22-30 V
V^*_{LV}	Nominal LV voltage	28V
P^*	Rated power	10 kW
P_c	Power capability	>5 kW
f_s	Switching frequency	100 kHz
N	Transformer turn ratio	5
C_o	Output capacitance	24 uF
C_c	Clamp capacitance	150 uF
L_s	Power transfer inductance	500 nH
L_o	Output inductance	1.65 uH
V_{p-p}	Max peak-to-peak on LV	560mV

Substituting the values from Table IV into equation (7), the contour plot of ΔI_{LV} can be drawn as shown in Figure 11. It can be observed that when V_{HV} = 300V and V_{LV} = 22V, a maximum peak-to-peak ripple of 71.1A on I_{LV} is predicted when using PS-PWM. This is confirmed by the simulation shown in Figure 12 (b). However, when PSM is utilised as illustrated Figure 12 (a), LV current ripple are effectively cancelled, and there is ideally no need for any passives to filter the current I_{LV}. This feature gives the ABAC converters an advantage in applications where batteries or fuel cells are integrated on the LV terminal. It is worth mentioning that due to the the shape of the inductor currents is controlled by the gating signals G_5-G_{11}, different adjacent active state periods of G_5-G_{11} make the inductor current ripple varying between single sampling intervals T_s. Therefore, by using the proposed PSM technique, the inductor currents presents repetitive waveform every two sampling intervals (i.e. every $2T_s$) rather than one. This is the consequence of applying the proposed modulation, which helps to achieve complete ripple cancellation on I_{LV}.

When a MEA application is considered for the ABAC converter, V_{HV} can typically change in a range 150V-300V while V_{LV} can vary from 22V to 30V. Therefore, the range for the voltage ratio r_V is 0.36-1. According to Figure 7, in this practical range, PSM has greater advantage in transferring more power when r_V gets close to 1. For example, considering a case when V_{HV} = 150V, V_{LV} = 28V and the voltage ratio r_V equals to 0.93. Referring to equations (19) and (20), the maximum transfer power for PS-PWM is 160W while it is possible to transfer 8.4kW using the proposed PSM. Simulations are shown in Figure 13. Notably, the duty cycles for both transformer port voltages in case of PS-PWM are very small. This essentially limits the maximum transferred power. However, in case of PSM, the duty can be modified accordingly with the power.

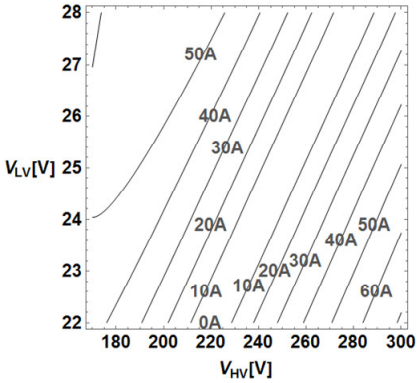

Figure 11: Contour plot of LV current peak-to-peak value ΔI_{LV} according to equation (7) using practical parameters from Table IV.

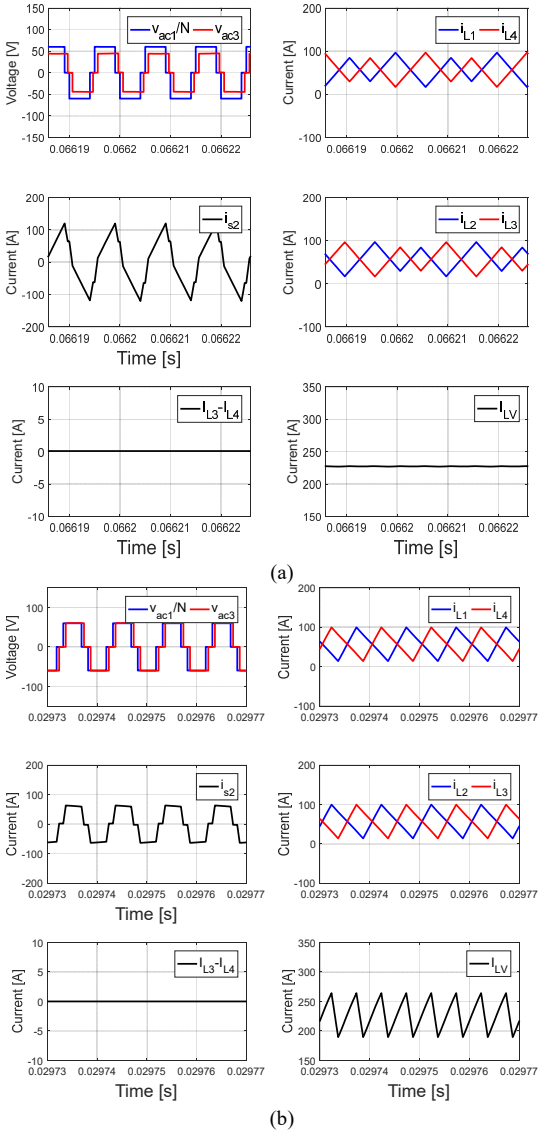

Figure 12: Simulation waveforms for (a) PSM V_{HV}=300V, V_{LV}=22V and P=5kW, and (b) PS-PWM V_{HV}=300V, V_{LV}=22V and P=5kW, emphasising on LV current ripple cancellation.

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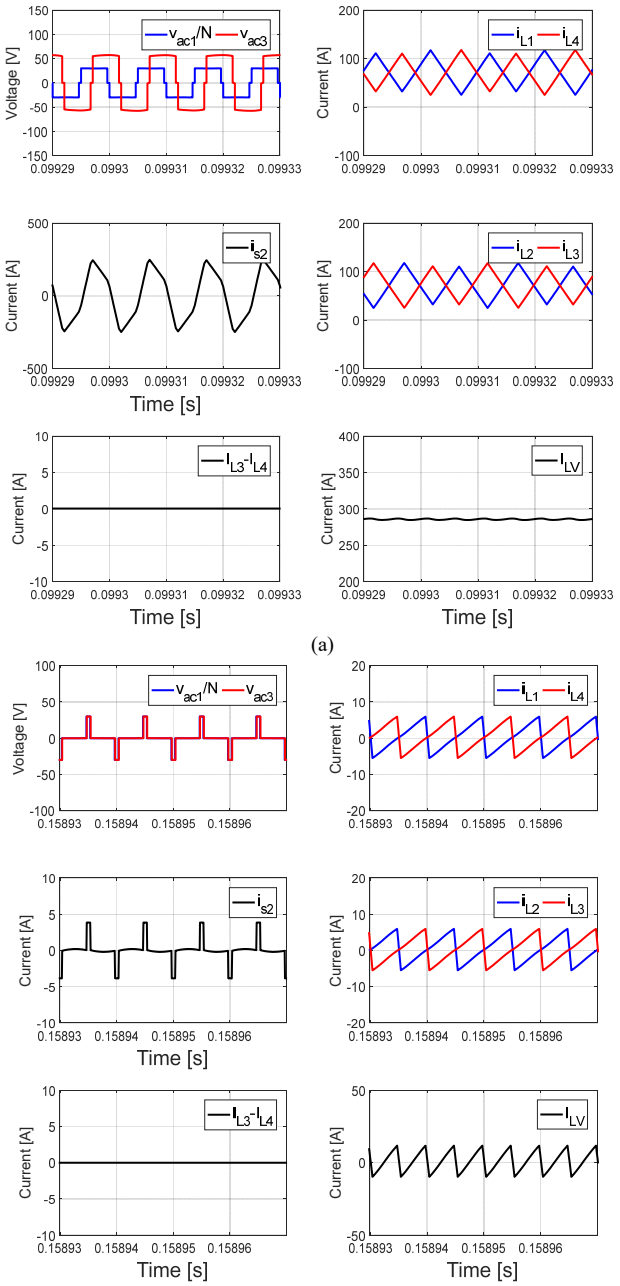

Figure 13: Power transfer capability comparison. (a) PSM V_{HI}=150V, V_{LV}=28V and P=8kW, and (b) PS-PWM V_{HI}=150V, V_{LV}=28V and P=30W.

A transition between Mode IV and Mode III is shown in Figure 8 where the trajectory lines are all linear and continuous across two modes. As mentioned at the beginning of this section, due to the converter model changes between Mode III and Mode IV when power changes, different sets of PI parameters are required to ensure performance. However, the voltage control has been implemented considering, on purpose, a very small control bandwidth. This has been required with the only scope of providing accurate steady state results, with slow dynamic performances and negligible disturbance rejection since the paper focus only on modulation and the control dynamic performances are not considered in this work. In this simulation HV and LV are connected to 300V and 22V voltage sources, respectively. As can be observed in Figure 14, the transition between modes is smooth.

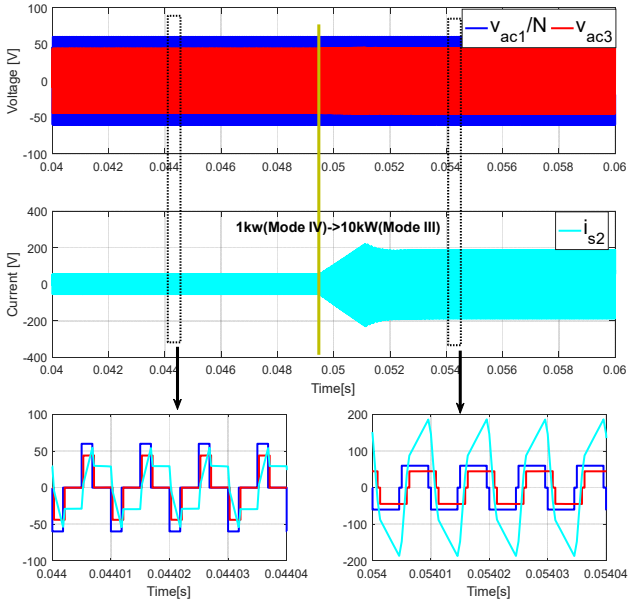

Figure 14: Seamless mode transition from 1kW in Mode IV to 10kW in Mode III under voltage condition: 300V/22V

Finally, losses for all the active devices including HV side and LV side switches are evaluated. The components in Table V are used in both simulation and experiment. Losses are estimated in PLECS based on datasheet parameters.

TABLE V
COMPONENTS INCLUDED IN THE LOSSES ESTIMATION

Component	Description	Main Parameters
HV switches	Wolfspeed C2M0025120D SiC MOSFET	1.2kV/90A $R_{DS(ON)}$ = 25mΩ E_{ON}/E_{OFF} = 1.4J/0.3J
LV switches	Infineon IPT020N10N3 Si MOSFET	100V/300A $R_{DS(ON)}$ = 2mΩ 2 devices in // per switch

Semiconductor losses under four different input/output voltage conditions on the whole converter power range are evaluated. It is worth pointing out that the loss evaluation is only meant to compare different modulation schemes rather than to provide an accurate overall efficiency prediction for this converter. The evaluation comprises both switching and conduction losses. Comparisons between modulations PS-PWM [20], PSM-SPS [25], PS-TRM [27] and PSM are carried out based on the same design parameters. According to p1 and p2 in Figure 15, PS-PWM presents the advantage over other schemes in terms of losses from switching devices. This is expected as in the case of PS-PWM, transformer current is lower in both peak and RMS value than others [22]. The increase in loss compared to PS-PWM is the major shortcoming of PSM. However, under voltage operating points p3 and p4, the conventional PS-PWM approach can hardly transfer any power, and PS-PWM cannot achieve comprehensive LV current ripple cancellation. It is worth pointing out that the power transfer capability of PS-TRM [27] relies on the difference between primary and secondary port voltages. As can be seen from p1 and p4, PS-TRM has larger maximum power transfer capability compared to p2 and p3. Additionally, it can be observed that the optimised PSM generally has less

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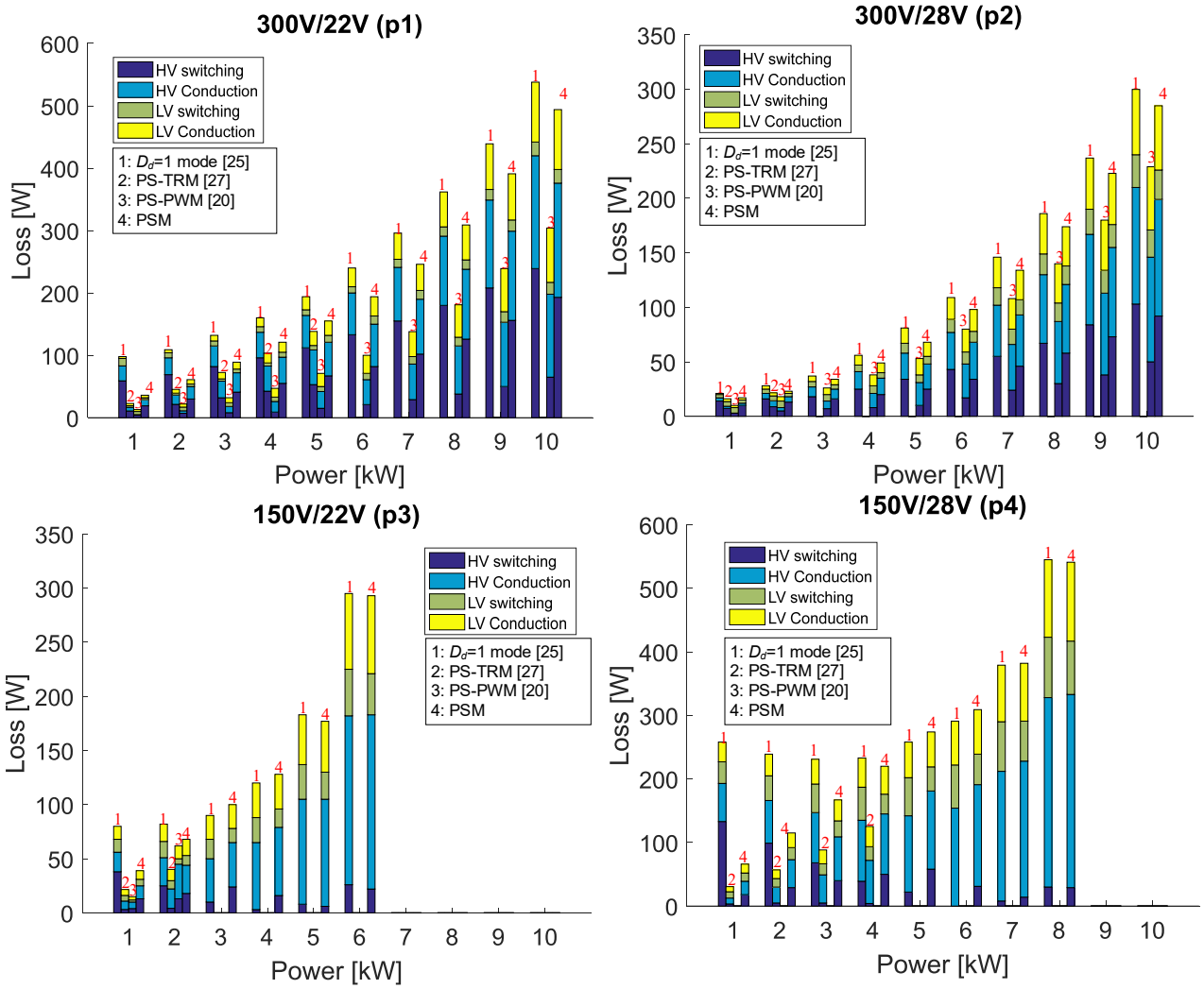

Figure 15: Loss evaluations for semiconductor devices on both HV and LV sides using different modulation methods with same design parameters.

losses than PSM-SPS under light and medium power in p1 and p2. According to the loss evaluation, a hybrid modulation scheme is possible for future investigation, but this paper focuses only on the proposed PSM, emphasising on the comprehensive LV current ripple cancellation and enhanced power transfer capability.

V. Experimental Results

The proposed modulation has been validated on a 100 kHz, 270V-28V prototype, shown in Figure 16. Semiconductors listed in Table V have been also used in this prototype. A TMS320F2837xD evaluation board from Texas Instruments enhanced by a custom interface board has been adopted as the digital control platform. The LV terminal voltage is measured and controlled by a PI controller as discussed in Figure 10. Results are sampled with a LeCroy oscilloscope using 100 MHz bandwidth differential voltage probes and 10 MHz bandwidth current probes. Results have been plotted using Matlab in order to provide clearer waveforms and to facilitate analysis.

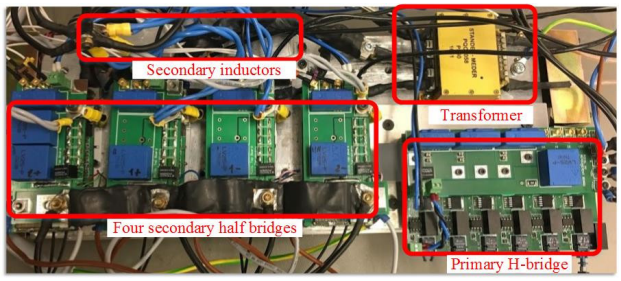

Figure 16: Practical experiment prototype of the ABAC converter.

Experimental results are shown in Figure 17 where the ABAC is modulated with PSM-SPS to deliver a power of 10kW to the LV resistive load, in the nominal voltage condition. The primary, secondary port voltages and secondary, primary transformer currents, together with the LV terminal voltage are shown from top to bottom in Figure 17. The V_{LV} is well regulated with 550mV peak-to-peak ripple.

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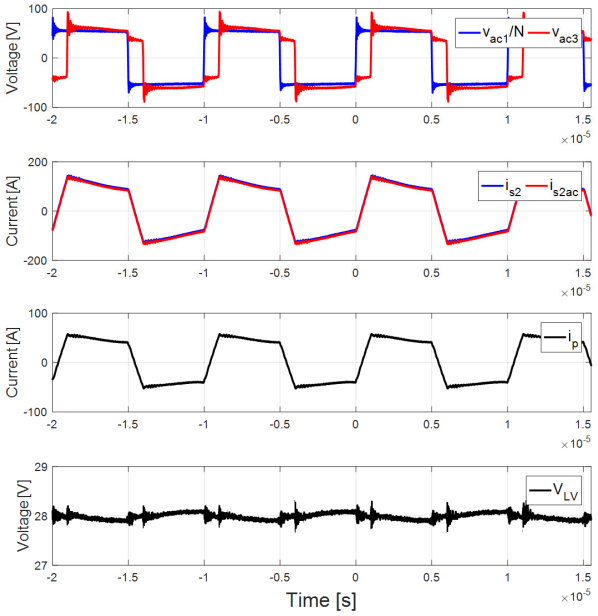

Figure 17: Experimental results using PSM-SPS under P=10kW, V_{HV}=270V and V_{LV}=28V.

Experimental results using optimised PSM are shown in Figure 18 (a) highlighting the balanced output inductor currents and absence of transformer DC bias, compared to the modulation method in [27]. The terminal voltage condition is V_{HV} = 170V, V_{LV} = 28V whilst providing 3kW on a resistive load. The DC components of current i_{L3} and i_{L4} are balanced according to the waveform of I_{L3}-I_{L4}. Also there is no DC bias current on the transformer, as confirmed by the i_{s2ac} waveform. Experiment results highlighting the LV currents interleaving feature of the proposed PSM scheme are shown in Figure 18 (b). In the experiment, the AC components of the LV current is measured as I_{LVac}. It is clear from the figure that effective LV ripple cancellation is achieved between i_{L1}, i_{L4} and i_{L2}, i_{L3}. As a consequence, the V_{LV} peak-to-peak ripple is limited to 540mV. It is worth mentioning that under such operating voltage condition, the conventional approach PS-PWM [20] can hardly transfer any power.

In accordance with the proposed PSM in Figure 3, the inductor currents have a period of $2/f_s$. Therefore, the shapes of i_{L3} and i_{L4} is balanced in two switching cycles. Regarding the transformer current, in the period θ_3- θ_5 and θ_7- θ_9 the capacitor C_1 and C_2 are inserted in the circuit together. However, in the period 0 - θ_1 and θ_{11} - θ_{13} both capacitors are floating. Therefore due to voltage variations on clamp capacitors, the shape of i_{s2} is different in period θ_3 - θ_5 and θ_7 - θ_9 from the shape in the period 0 - θ_1 and θ_{11} - θ_{13}. Notably, the waveform of v_{ac3} has some discrepancies compared to the one obtained in Figure 12 (a) and Figure 13 (a), and it presents additional voltage steps on v_{ac3} when the slope of the transformer current changes. These are caused by parasitic grounding inductance between four clamp circuits in the prototype and this effect can be removed by changing the physical layout of the clamp circuits.

Comparisons of transformer current stress between PSM-SPS (also known as "D_d = 1 mode" in paper [25]) and optimised PSM under different voltage ratio r_V are shown in Figure 19. It can be noted that when using optimised PSM, the transformer current stress is always smaller than PSM-SPS, especially when the load power is decreased and operation voltage varies from the nominal value. However, when operating voltages become close to the nominal value, the optimisation on peak current presents negligible advantages, as already shown in Figure 15.

Experiment results in Figure 20 and Figure 21 show ZVS validations for points A and B in Figure 9. The waveforms are obtained under r_V above 0.5 in Figure 20 (a) and Figure 21 (a) and for r_V close to 0.5 in Figure 20(b) and Figure 21(b). As predicted by the theoretical analysis, currents are always flowing through the anti-paralleled body diode of the MOSFETs before being turned on. Therefore, ZVS can be achieved for all switches in both cases.

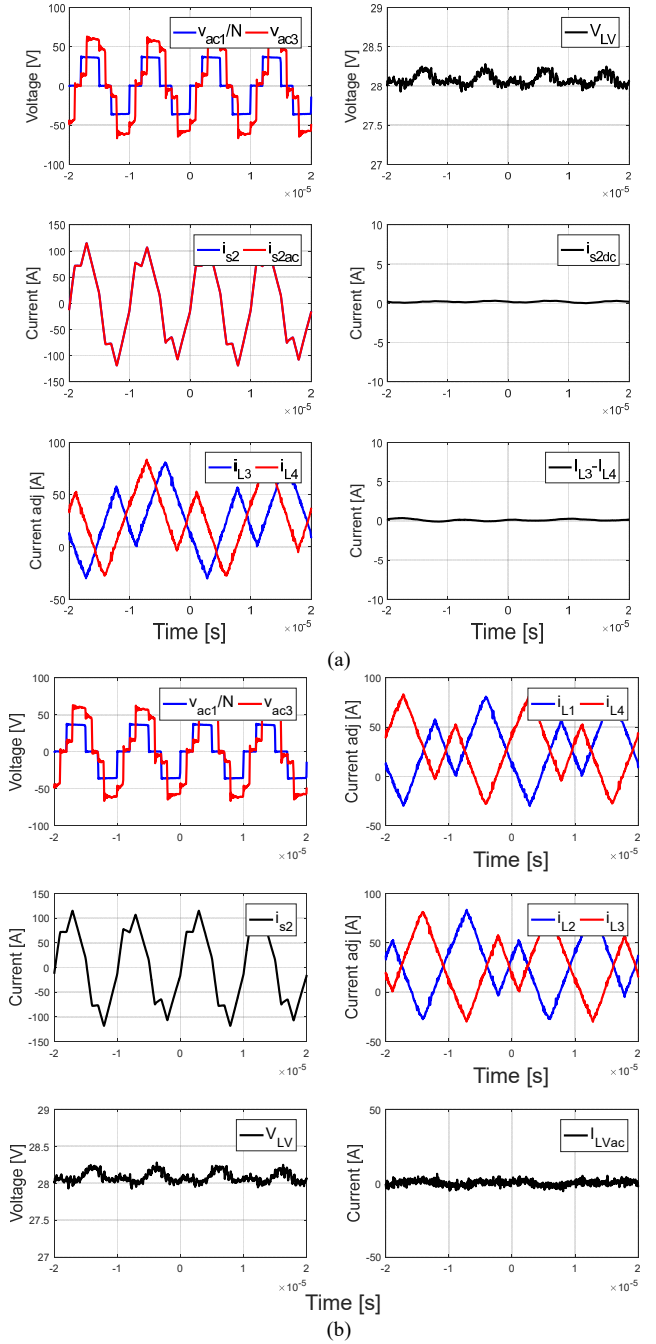

Figure 18: Experimental results with the proposed PSM applied under P=3kW, V_{HV}=170V, V_{LV}=28V, emphasising on (a) balanced power transfer, and (b) comprehensive LV current interleaving.

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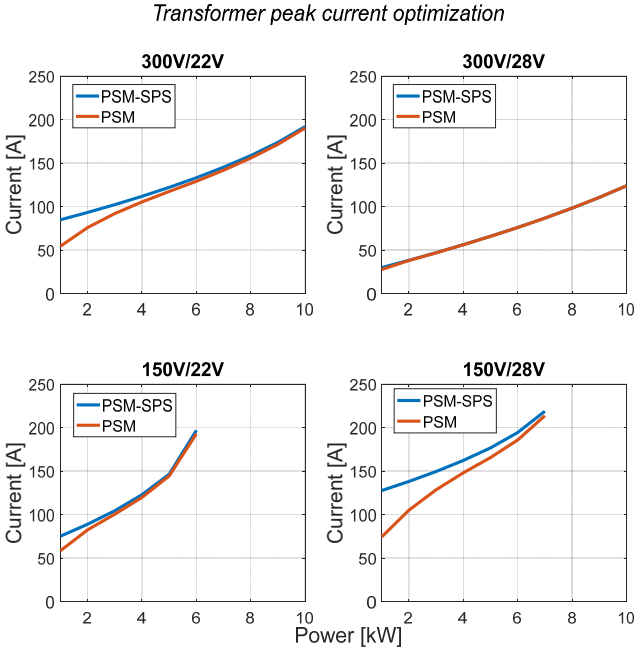

Figure 19: Transformer secondary current peak value comparisons between PSM-SPS and optimised PSM.

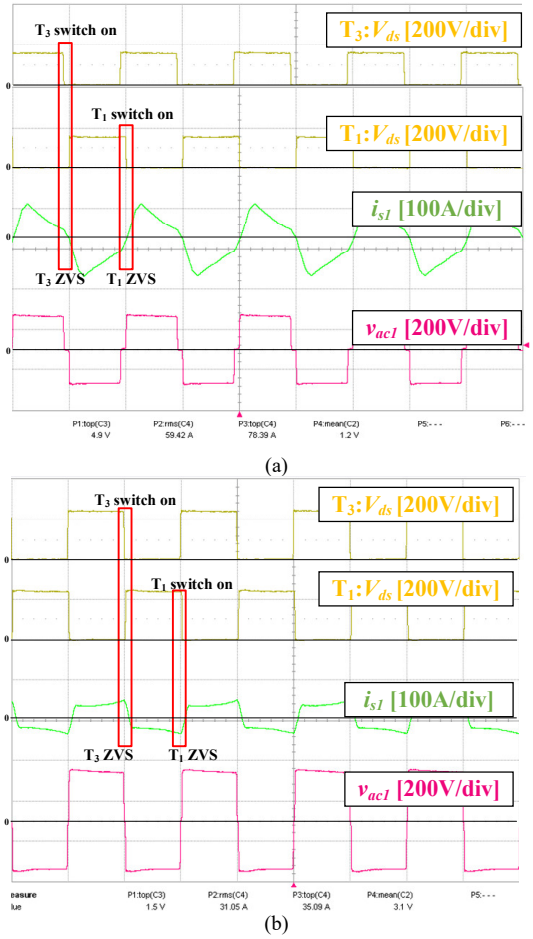

Figure 20: Experimental waveforms for ZVS validation of HV bridge MOSFETs at (a) V_{HV} = 154.47 V, V_{LV} = 22 V (r_V=0.71) with phase shift values D_d=0.91, φ/π=0.3, and (b) V_{HV} = 238 V, V_{LV} = 22 V (r_V=0.46) with phase shift values D_d=0.97, φ/π =0.14. Time base: 5 µs/div.

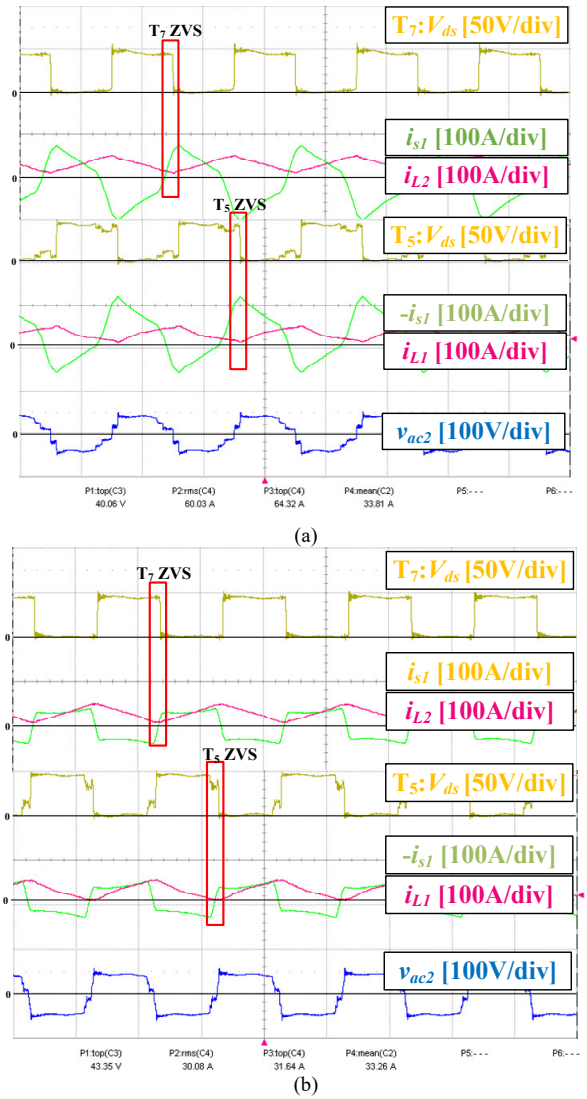

Figure 21: Experimental waveforms for ZVS validation of LV bridge MOSFETs at (a) V_{HV} = 154.47 V, V_{LV} = 22 V (r_V=0.71) with phase shift values D_d=0.91, φ/π=0.3, and (b) V_{HV} = 238 V, V_{LV} = 22 V (r_V=0.46) with phase shift values D_d=0.97, φ/π =0.14. Time base: 5 µs/div.

VI. CONCLUSION

In this paper, the ABAC converter is introduced as a suitable power converter topology to transfer power between 270VDC and 28VDC buses in high power MEA applications where stringent power quality requirements apply. Conventionally, the ABAC converter can be driven with PS-PWM techniques. However, PS-PWM presents increased LV current harmonics and less power transfer capability when HV and LV vary from their nominal values. Therefore, a PSM is proposed and optimised. By using the proposed PSM in this paper, maximum power transfer capability can be greatly improved compared to PS-PWM. It can also achieve comprehensive cancellation on LV current at any voltage operation points, resulting in lower requirements for passive filtering when compared to the PS-PWM.

Simulations and experiments on a 10-KW ABAC converter are conducted to verify the theoretical claims. A comparison between the presented PSM and PS-PWM has been carried out.

The results show the advantage of the proposed method in terms of LV power quality and power transfer ability. In addition, analysis and validation of the ZVS region are also provided. Comparisons between optimised PSM and PSM-SPS is also conducted, confirming the merit of transformer current stress reduction using the proposed method.

REFERENCES

[1] P. Wheeler and S. Bozhko, "The More Electric Aircraft," *IEEE Electrif. Mag.*, vol. 2, no. 4, pp. 6–12, 2014.

[2] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017.

[3] G. Buticchi, L. Costa, and M. Liserre, "Improving System Efficiency for the More Electric Aircraft: A Look at dc\/dc Converters for the Avionic Onboard dc Microgrid," *IEEE Ind. Electron. Mag.*, vol. 11, no. 3, pp. 26–36, Sep. 2017.

[4] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, 1992.

[5] C. Mi, H. Bai, C. Wang, and S. Gargies, "Operation, design and control of dual H-bridge-based isolated bidirectional DC-DC converter," *IET Power Electron.*, vol. 1, no. 4, pp. 507–517, 2008.

[6] J. Riedel, D. G. Holmes, B. P. McGrath, and C. Teixeira, "Active Suppression of Selected DC Bus Harmonics for Dual Active Bridge DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8857–8867, Nov. 2017.

[7] Xiaodong Li and A. K. S. Bhat, "Analysis and Design of High-Frequency Isolated Dual-Bridge Series Resonant DC/DC Converter," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 850–862, Apr. 2010.

[8] C. Liu, H. Liu, G. Cai, S. Cui, H. Liu, and H. Yao, "Novel Hybrid LLC Resonant and DAB Linear DC–DC Converter: Average Model and Experimental Verification," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 6970–6978, Sep. 2017.

[9] J. Wu, Y. Li, X. Sun, and F. Liu, "A New Dual-Bridge Series Resonant DC-DC Converter with Dual-Tank," *IEEE Trans. Power Electron.*, pp. 1–1, 2017.

[10] H. Wu, K. Sun, Y. Li, and Y. Xing, "Fixed-Frequency PWM-Controlled Bidirectional Current-Fed Soft-Switching Series-Resonant Converter for Energy Storage Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6190–6201, Aug. 2017.

[11] S. Bal, D. B. Yelaverthi, A. K. Rathore, and D. Srinivasan, "Improved Modulation Strategy using Dual Phase Shift Modulation for Active Commutated Current-fed Dual Active Bridge," *IEEE Trans. Power Electron.*, pp. 1–1, 2017.

[12] F. Z. Peng, H. Li, G.-J. Su, and J. S. Lawler, "A New ZVS Bidirectional DC–DC Converter for Fuel Cell and Battery Application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004.

[13] G. Spiazzi and S. Buso, "Analysis of the Interleaved Isolated Boost Converter With Coupled Inductors," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7. pp. 4481–4491, 2015.

[14] D. Sha, Y. Xu, J. Zhang, and Y. Yan, "Current-Fed Hybrid Dual Active Bridge DC–DC Converter for a Fuel Cell Power Conditioning System With Reduced Input Current Ripple," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6628–6638, Aug. 2017.

[15] L. Tarisciotti, A. Costabeber, C. Linglin, A. Walker, and M. Galea, "Evaluation of isolated DC/DC converter topologies for future HVDC aerospace microgrids," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 2238–2245.

[16] D. Sha, F. You, and X. Wang, "A High Efficiency Current Fed Semi Dual Active Bridge DC-DC Converter for Low Input Voltage Applications," *IEEE Trans. Ind. Electron.*, pp. 1–1, 2015.

[17] G. Ortiz, L. Fassler, J. W. Kolar, and O. Apeldoorn, "Flux Balancing of Isolation Transformers and Application of 'The Magnetic Ear' for Closed-Loop Volt–Second Compensation," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4078–4090, Aug. 2014.

[18] B. Zhao, Q. Song, W. Liu, and Y. Zhao, "Transient DC Bias and Current Impact Effects of High-Frequency-Isolated Bidirectional DC–DC Converter in Practice," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3203–3216, Apr. 2016.

[19] D. Urciuoli, R. A. Wood, and C. W. Tipton, "Trade Study and Design of a TRL-4, 100 °C, 28- to 600-V Bidirectional DC." 01-Jan-2011.

[20] H. Xiao and S. Xie, "A ZVS Bidirectional DC–DC Converter With Phase-Shift Plus PWM Control Scheme," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 813–823, Mar. 2008.

[21] D. Sha, X. Wang, and D. Chen, "High Efficiency Current-Fed Dual Active Bridge DC–DC Converter with ZVS Achievement Throughout Full Range of Load Using Optimized Switching Patterns," *IEEE Trans. Power Electron.*, pp. 1–1, 2017.

[22] Z. Guo, K. Sun, T.-F. Wu, and canbing Li, "An Improved Modulation Scheme of Current-fed Bidirectional DC-DC Converters for Loss Reduction," *IEEE Trans. Power Electron.*, pp. 1–1, 2017.

[23] G. Xu, D. Sha, J. Zhang, and X. Liao, "Unified Boundary Trapezoidal Modulation Control Utilizing Fixed Duty Cycle Compensation and Magnetizing Current Design for Dual Active Bridge DC–DC Converter," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2243–2252, Mar. 2017.

[24] Y. Wang, S. W. H. de Haan, and J. A. Ferreira, "Optimal operating ranges of three modulation methods in dual active bridge converters," in *2009 IEEE 6th International Power Electronics and Motion Control Conference*, 2009, pp. 1397–1401.

[25] Y. Shi, R. Li, Y. Xue, and H. Li, "Optimized Operation of Current-Fed Dual Active Bridge DC-DC Converter for PV Applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6986–6995, Nov. 2015.

[26] X. Nan and C. R. Sullivan, "An Equivalent Complex Permeability Model for Litz-Wire Windings," *IEEE Trans. Ind. Appl.*, vol. 45, no. 2, pp. 854–860, 2009.

[27] L. Chen, L. Tarisciotti, A. Costabeber, P. Zanchetta, and P. Wheeler, "Advanced modulation for the Active-Bridge-Active-Clamp (ABAC) converter," in *2017 IEEE Southern Power Electronics Conference (SPEC)*, 2017, pp. 1–6.

[28] J. Hayes, K. George, P. Killeen, B. McPherson, K. J. Olejniczak, and T. R. McNutt, "Bidirectional, SiC module-based solid-state circuit breakers for 270 Vdc MEA/AEA systems," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, pp. 70–77.

[29] D. A. Molligoda, P. Chatterjee, C. J. Gajanayake, A. K. Gupta, and K. J. Tseng, "Review of design and challenges of DC SSPC in more electric aircraft," in *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, 2016, pp. 1–5.

[30] *Sensitron Semiconductor, "28V DC Solid State Power Controller Module ," SPDC150D28 datasheet [Revised C].*

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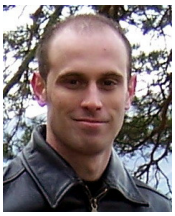

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