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2018 ITRW Packaging and Integration Roadmap

Unlocking the full potential of wide-bandgap devices

by Mark Johnson,
Peter R. Wilson,
Lee Empringham,
and Liliana De Lillo

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The International Technology Roadmap for Wide-Bandgap Power Semiconductors (ITRW) has four distinct technical working groups, each providing its own perspective on the technology and industrial drivers for the adoption of wide-bandgap (WBG) power semiconductors in power electronics. This article summarizes the progress toward an initial roadmap for the packaging and integration working group of the ITRW.

Background

New approaches to packaging and integration will be needed to unlock the full potential of wide-bandgap devices. Compared to silicon power device technology, the significantly increased switching speeds of the wide-bandgap devices allow for much higher switching frequencies, leading, e.g., to smaller passive component requirements, more power-dense converters, and a reduced bill of materials (BoM). However, such desirable features can only be achieved if circuit parasitics and the associated electromagnetic interference (EMI) can be reduced to unprecedentedly low levels. This demands radically new approaches to integration, moving from assemblies of discrete components, each designed and packaged separately, to fully integrated assemblies comprising power devices, gate drives, filters, sensing, and control functions.

The progression to integrated functional blocks will occur over differing timescales according to the power level and application. Many low-power (fewer than a few hundred watts) dc-dc converters are already fabricated as single-package, integrated

assemblies. The norm for higher power levels (greater than a few kilowatts) typically combines surface-mount components on a multilayer printed circuit board (PCB) with larger discrete passive components and power semiconductor modules. The desire for higher switching speeds will drive the move to smaller commutation cells, favoring increased use of smaller, surface-mount components, embedded component technologies, and three-dimensional (3-D) stacked structures.

Consequently, it is likely that higher-power converters will be realized as several lower-power modular blocks, combined in parallel or in a series, so that the benefits of higher-frequency switching can be maintained. The upper power limit for such techniques is likely to increase once a modular approach to the design and manufacture of these converters becomes established across the industry.

Focus and Scope

The primary technology focus of the packaging and integration working group is high-speed switching, identifying the materials, design, and manufacturing approaches that will support the thermal, electromagnetic, and through-life management of power electronic converters at power levels from hundreds of watts to hundreds of kilowatts and beyond. A secondary focus is on technologies that enable the operation at higher temperatures and other harsh environments. The roadmap targets technological developments within three distinct terms: short (within five years), medium (within five to 15 years), and long term (commercial realization at 15 years and more).

Top-Level Drivers

The top-level drivers for power electronics that apply to packaging and integration include:

- reduced costs [BoM, manufacturing, operation and maintenance (O&M), recycling]
- increased efficiency (reduced losses through life)
- increased power density (reduced volume, reduced mass)
- ease of use (plug and go, modular solutions, higher voltage, higher current, load/source integration, simple maintenance)
- environmental tolerance (higher temperature, extreme temperature range, vibration and shock, radiation that is hard)
- reliability and robustness (longer application lifetimes, longer time between maintenance, fewer early failures, ability to survive fault events).

Technical Drivers

The overarching challenge for the packaging and integration working group is to develop cost-effective solutions that can unlock the full potential of WBG semiconductors. Specific technology drivers for packaging and the modules that contribute to the realization of the top-level drivers include:

- higher levels of structural and functional integration
- improved electrical and magnetic performance
- greater reliability and robustness
- extended operating range (voltage, current, temperature, and frequency)
- improved thermal performance.

Table 1 summarizes the primary influences of the packaging and modules technology drivers on the top-level

Table 1. A summary of the primary influences of the packaging and modules technology drivers on the top-level drivers and their target metrics.

		Packaging and Integration Technology Drivers				
Power Electronics High-Level Drivers	High-Level Targets	Higher Levels of Structural and Functional Integration	Improved Electrical and Magnetic Performance	Improved Reliability and Robustness	Extended Operating Range (V, I, T, f)	Improved Thermal Performance
Cost	Reduced BoM low-cost manufacturing; easier recycling; reduced O&M cost; reduced recycling cost	+	0–	+	+	+0–
Efficiency	Lower through-life energy losses	0	+	0	0–	+
Power Density	Smaller and lighter	+	+0–	0–	+	+
Ease of Use	Plug and go; simplified thermal management; modular and reconfigurable; minimized EMI; load/source integration	+	+	+	+	+
Environmental Tolerance	Higher temperature; extreme vibration and shock	+0	0	+	+	+0

V: voltage; I: current; T: temperature; f: frequency.

FIG 1 The roadmap for supporting technology in packaging and integration for WBG power electronics. SFI: structural and functional integration; EMP: electrical and magnetic performance; RR: reliability and robustness; EOR: extended operating range; TP: thermal performance; DBC: direct bonded copper; AMB: active metal brazed; IMS: insulated metal substrate; AlSiC: aluminum-silicon carbide.

drivers and their target metrics. For example, a top-level driver “cost” is influenced positively (+) by “higher levels of structural and functional integration” (reduced BoM and low-cost assembly), “improved reliability and robustness” (lower O&M costs and reduced recycling), and “higher temperature operation” (reduced BoM). Conversely, the need for “improved electromagnetic management” and “improved thermal management” may be cost neutral (0) or add (–) to the BoM, assembly costs, and so on.

Relationship to Other Roadmaps: IEEE Electronic Packaging Society Heterogeneous Integration Roadmap

The Electronic Packaging Society (EPS) Heterogeneous Integration Roadmap (HIR) covers a wide range of electronic applications, including integrated power electronics (IPE), as part of the system-in-package (SiP) solutions. IPE looks specifically at approaches that are mapping technologies for integrating power around the periphery or directly embedding power within a component, which is a single package among other components within an SiP module, e.g., a radio-frequency communications component, a graphics-processor component, or a photonic information processor. The HIR does not focus on discrete power electronics or stand-alone power conversion modules, whether outside or inside the SiP module.

To maximize the efficiency and effectiveness of both roadmaps, the ITRW will work in cooperation with the HIR team by sharing knowledge and the experience of power electronic packaging and integration. This will be facilitated by cross-representation within relevant groups of the ITRW and HIR. For more details regarding HIR, see <https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html>.

Plan and Expected Outcome

What will the impact be of such a roadmap, what is included and excluded, and would there be a draft template? The roadmap for this working group has been divided into two main sections: 1) supporting technologies and 2) packages. The supporting technologies include interconnects and vias, die attach and mount-down, substrates, encapsulation, baseplate and thermal management, housing and termination, metallization, passive components and sensors, simulation and virtual prototyping, and testing and qualification. The package types have been divided into three broad classes: 1) discrete or single functional switches, including through-hole, surface mount, and chip direct packages; 2) modules, including conventional monoplanar, hermetic power hybrid, press-pack, and conventional multiplanar; and 3) integrated power modules, including substrate-assembled and additive-embedded variants. The draft roadmaps for the supporting technolo-

This article summarizes the progress toward an initial roadmap for the packaging and integration working group of the ITRW.

gies and the various package types are shown in Figures 1 and 2, respectively.

Each technology bar shows the period of mass-market exploitation with chevrons, indicating a degree of uncertainty; one chevron indicates some uncertainty around the timing of mass-market adoption or phaseout, while two chevrons indicate considerable uncertainty around the timing of mass-market adoption or phaseout. The relevance of each technology bar to the packaging and integration

technology drivers are shown using color-coded bars (see Figure 3). Each bar has a color-coded key indicating the strength of the impact on each driver, with five separate columns labeled as follows:

- 1) *SFI*: higher levels of structural and functional integration
- 2) *EMP*: improved electrical and magnetic performance
- 3) *RR*: improved reliability and robustness (voltage, current, temperature, and frequency)
- 4) *EOR*: extended operating range
- 5) *TP*: improved thermal performance.

Packaging for WBG Power Electronics

Case Study 1: Integrated Switching Cells for Modular WBG Conversion

The fast-switching speeds and low specific conduction losses of WBG semiconductors allow for the realization of high-frequency, high-power density switching converters with dramatically reduced passive component requirements compared to silicon technology. However, careful attention must be paid to switching cell design to mitigate the effects of circuit parasitics and fast voltage transitions, which would otherwise limit the attainable switching speed and lead to increased levels of EMI. A modular, power-cell solution is proposed in [1], which allows for the creation of any two-level topology converter. The cell structure enables fast switching of WBG semiconductor devices while allowing high-power converters to be fabricated using multiple smaller commutation cells. Using a single-ceramic substrate to act as the thermal path, close integration of semiconductor dies, decoupling capacitors, gate drives, and output filters allows for a dramatic increase in power density without compromising converter performance (Figure 4).

Case Study 2: High-Voltage Packages for Silicon Carbide MOSFETs

High-voltage silicon carbide (SiC) devices offer an attractive combination of fast switching and low losses. This gives application users unprecedented levels of flexibility in choosing the topology and control strategy for medium- and high-voltage power conversion. However, the realization of power modules that are optimized for

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FIG 2 The roadmap for a range of package types applicable to WBG power electronics. Si: silicon; GaN: gallium nitride; EM: electromagnetic; DBC: direct-bonded copper; LTCC: low-temperature cofired ceramic; IPM: integrated power module.

the high-electric fields while maintaining compact commutation loops and effective thermal management presents significant challenges including: 1) the mitigation of high-electric fields in the substrates, interconnects, and leadout connections; 2) the suppression of switching voltage overshoot and common-mode interference; and 3) the high-performance thermal management. The assembled module described in [2] incorporates stacked substrates with vias to mitigate internal electric fields and allows for the realization of vertical-commutation loops (Figure 5). Embedded decoupling capacitors and an inter-

layer screen help to suppress voltage overshoot and heat-sink-coupled common-mode interference. Finally, the application of a direct-substrate liquid impingement cooler permits exceptional thermal performance within a small physical envelope.

Case Study 3: SiC Power Electronics for Traction Applications

Because of numerous emerging challenges that are different from those in the automotive industry, a sustained effort is required to realize the aggressive targets of heavy equipment electrification, e.g., heavy-duty and off-road vehicles. Heavy equipment manufacturers are increasingly investing in a new generation of power electronics technology to fulfill high-performance and reliability targets under harsh environments while reducing fuel consumption and maintaining cost competitiveness. In a recent work led by the University of Arkansas [3], a holistic

FIG 3 The relevance to technology-driver color coding.

FIG 4 (a) A modular three-phase inverter based on half-bridge switching cells incorporating gate drives, sensors, low-level controls, and input/output filters [1]. (b) The output V and I waveforms with a resistive load, demonstrating low levels of switching noise and ripple.

FIG 5 (a) A cross section through the module and cooler, showing stacked substrates, interconnected posts, and termination pins. (b) The physical realization of the prototype 10-kV SiC MOSFET module [2].

power electronics design approach is proposed to achieve 25 kW/L at 98% peak efficiency for a compact 250-kW three-level T-type traction inverter. This traction inverter is designed using the best-in-class SiC power modules, novel gate drivers, and, most importantly, a multiobjective optimization approach. This will trade the volumetric power density (kW/L) against the SiC device types (650, 900, and 1,200 V), the dc-bus voltage, the switching frequencies, the size of the passives, and the subsequent filtering requirements.

Taking a modular approach to developing these power electronics modules leads to the use of power modules or building blocks. The power electronics building block (PEBB) developed by the University of Arkansas features a switching power device with associated gate drivers, dc-link capacitors, and an interconnection bus bar, as shown in Figure 6. A hybrid switch, which includes a silicon (Si) IGBT and MOSFET in parallel, forms the switching power device in the PEBB. A low-inductive multilayer laminated bus bar was designed to have symmetrical current commutation loops. A major contribution is that this was achieved while using no three-level T-type power module. A loop inductance of 29 nH was achieved, which is lower than

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the existing state-of-the-art three-level designs in the existing literature. The fabricated prototype PEBB achieves a specific power density of 27.7 kW/kg and a volumetric power density of 308.61 W/in³. Single-phase operation of the PEBB has been demonstrated at the switching frequency of 28 kHz. This hybrid switch concept can provide benefits of high-switching speed and low-switching loss from the SiC MOSFET while also providing high-current handling capability from the large IGBT. The overall cost of this WBG Si-hybrid approach is economic comparing to all SiC solutions while

it is offering advanced switching characteristics over Si IGBTs.

Summary

This article, which discusses the packaging and integration roadmap of WBG power electronics, was written by the packaging and integration working group of the ITRW to stimulate discourse in the stakeholder group. The membership of the packaging and integration working group will be reviewed to ensure that all relevant stakeholder groups are represented by global leaders in their respective fields.

The working group is continuously reviewing the proposed taxonomy, paying attention to the top-level

FIG 6 A 100-kW three-level T-type single-phase PEBB [3].

technology drivers as well as and the package types and supporting technologies to confirm that the adopted taxonomy is appropriate and complete. A key task for the working group will be to identify the research, development, and industrialization activities needed to support the roadmap priorities on a short (0–5 years), medium (5–15 years), and long-term (15–30 years) horizon.

The broad categories defined by the working group are:

- curiosity-inspired research ten or more years out from mass-market exploitation
- industry-led development five to ten years out from mass-market exploitation
- industrialization initiatives zero to five years out from mass-market exploitation.

The realization of roadmap priorities will generally require all three stages in succession.

A key challenge for the practical realization of WBG devices in power electronics applications will be effective packaging that addresses the challenges of high-speed operations and thermal management for extreme and hazardous environments. As can be seen in the state-of-the-art examples presented in this article, solid progress has been made, but there is much work to be done in packaging for WBG devices over the longer term.

About the Authors

Mark Johnson (mark.johnson@nottingham.ac.uk) received his B.A. and Ph.D. degrees from the University of Cambridge, United Kingdom, in 1986 and 1990, respectively. He is the director of the EPSRC Centre for Power Electronics and professor of advanced power conversion, Faculty of Engineering, in the Department of Electrical and Electronic Engineering at the University of Nottingham, England. His research interests include the packaging, integration, thermal management, and reliability of power electronic assemblies. He is a Member of the IEEE.

Peter R. Wilson (p.r.wilson@bath.ac.uk) received his B.Eng. degree (honors) from Heriot-Watt University, Edinburgh, United Kingdom; his M.B.A. degree from Edinburgh Business School, United Kingdom; and his Ph.D. degree from the University of Southampton, United Kingdom. He has worked for Ferranti, Scotland; Analogy Inc.; the University of Southampton as a research fellow, lecturer, senior lecturer, and reader between 2002 and 2015; and joined the University of Bath, United Kingdom, in 2015 as a full professor. He has published more than 100 papers, three books, and a patent in power electronics and electronic systems engineering. His research interests include the modeling and simulation of power electronics, particularly for aerospace applications, modeling magnetic components, integrated circuit design for silicon photonic systems, electronic design tools and design automation, artificial neural networks, and autonomous systems. He is the executive vice

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president of standards in the IEEE Power Electronics Society and a Senior Member of the IEEE.

Lee Empringham (lee.empringham@nottingham.ac.uk) received his B.Eng. degree (honors) in electrical and electronic engineering from the University of Nottingham, United Kingdom, in 1996 and received his Ph.D. degree in 2000. While pursuing

his Ph.D. degree, he joined the Power Electronics, Machines, and Control Group within the School of Electrical and Electronic Engineering at the University of Nottingham to work on matrix converter commutation techniques. He is currently employed as a research fellow to support different ongoing matrix converter projects. In 2010, he was appointed as the principal research fellow within the group and a full professor in 2017. His research interests include direct ac–ac power conversion, variable speed ac motor drives using different circuit topologies and more-electric aircraft applications. More recently, his research interests have focused on power electronics integration and high power density power conversion techniques.

Liliana De Lillo (Liliana.De_lillo@nottingham.ac.uk) received her M.Eng. degree in electronic engineering from Politecnico di Bari, Italy, in 2001. She received her Ph.D. degree in electrical engineering from the University of Nottingham, United Kingdom, in 2006 after having joined the Power Electronics, Machines, and Control (PEMC) Group and following her participation in a European student exchange project. In 2007, she started working as a research fellow within the PEMC Group, further developing her interest in more-electric aircraft applications and fault-tolerant power converters for aircraft applications. In 2012, she was appointed as a senior research fellow within the same group and continued to work on direct ac–ac converters, especially employing wide-bandgap semiconductor devices, fault tolerant systems, and the design and implementation of compact power converters with a main focus on the challenges of power electronics integration. She is a Member of the IEEE.

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