The optimisation of a 15 kV 4H-silicon carbide integrated gate commutated thyristor

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***Abstract*—A 15kV SiC thyristor is analysed, considering for the first time the design properties that will ensure the safe, stable operation of the device as an integrated gate commutated thyristor (IGCT), while also minimizing its on-state losses. Key to the optimization is ensuring that, during the turn-off phase, minority carrier charge is commutated via the base to the gate, rather than flowing into the cathode, thus reducing large switching losses, and an unstable transition period. This is made possible in the design presented via the introduction of a highly doped base strip (HDBS), which provides a low resistance channel between the centre of the cathode and the gate. This innovation allows the cathode to be extended, such that it makes up 90% of the top surface, thus minimising on-state losses.**

Keywords—Silicon carbide, thyristor, IGCT, optimization, simulation.

I. Introduction

In recent years, the need to develop high-voltage and high-power switching devices has grown rapidly. It is believed that semiconductor devices made of wide bandgap materials such as Silicon Carbide (SiC) will replace conventional silicon (Si) power devices in high voltage power systems due to their high critical electrical field and thermal conductivity [1].

Today, SiC Schottky diodes and MOSFETs have been produced commercially up to 1.7 kV [2], yet there is potential for SiC to be scaled to voltages beyond 10 kV. However, achieving a high blocking voltage requires thick drift regions (>100 µm), and on-state resistance reduction must therefore be achieved via conductivity modulation [3], therefore making devices such as IGBTs and thyristors most relevant. These ultra-high voltage SiC bipolar devices could be used to simplify the topology of electric power circuitry such as MMCs, wherein one SiC device can replace several series connected Si IGBTs or thyristors [4]. As current driven devices without a MOS interface, SiC thyristors have high safe operating temperatures and no oxide reliability problems [5]. Therefore, a study of SiC thyristor devices is necessary to enable ultra-high-power applications.

Traditional Si gate turn-off thyristors (GTOs), which can be turned on and off using a gate current signal, were the mainstay of high voltage, high power systems from their introduction in the 1960's. The introduction of Integrated Gate Commutated Thyristors (IGCTs) around the turn of the century [6] can be seen as an evolution of the GTO. The problem with traditional GTOs was that during the turn off transition, current was commutated via the cathode, while at the same time the anode-cathode voltage was rising, which led to large losses and an unstable transition region. This could only be overcome through circuit design, typically snubbers to reroute the current during switching.

The key principle that led to the redesign of the IGCT was to reroute the current internally, ensuring commutation via the gate during the turn-off phase, thus separating the expanding space charge region and the current flow. This was achieved largely via changes to the circuitry, including low inductance gate design, and greater integration, in order to increase the dI_G/dt from GTO levels of ~50A/µs to kA/µs levels. However, in designing an IGCT, the design of the base and cathode regions require careful optimisation to ensure that current commutation occurs exclusively via the gate, avoiding dangerous current filaments in the central cathode region that can lead to device failure.

These principals will apply equally to a future SiC IGCT, though it is a subject that is yet to receive consideration, devices having been limited thus far to generic thyristor structures. Given the wide availability of N+ SiC substrates, there has been some initial interest in P-GTOs [7], whereby a p-type drift region sits above a N-type anode. However, the turn-off time of a SiC P-GTO is much longer than the equivalent N-GTO due to the low hole mobility in the top PNP base region. The absence of a P-substrate can however be resolved as it has been for n-

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IGBTs [8], by using an epitaxially grown anode region, and later removing the N+ substrate via grinding/polishing.

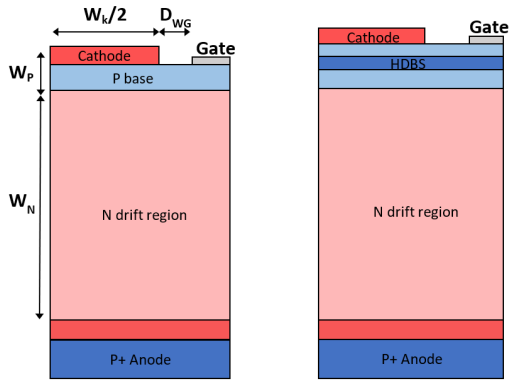

Figure 1: Section of IGCT (left: conventional IGCT; right: IGCT with HDBS)

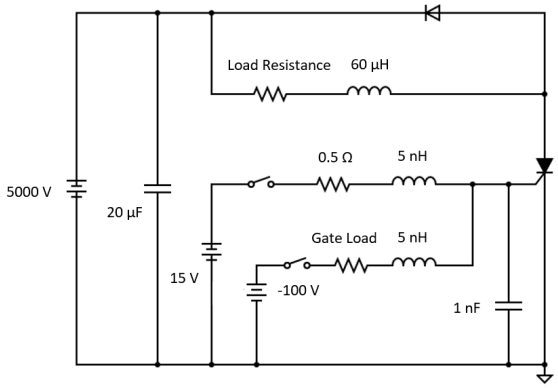

Figure 2: The IGCT PSPICE Switching Circuit

This work will introduce the design principles of optimizing a SiC IGCT. A 15 kV design will be introduced, made possible via a newly proposed highly doped base strip (HDBS). The advantages and limitations of this design will be explored using TCAD Sentaurus.

II. Methodology

The basic 2D structure of two IGCT designs is shown in figure 1. In both designs, a 2 µm thick, 5×10^{17} cm^{-3} N-field stop layer is on top of a 15 µm thick, 1×10^{19} cm^{-3} P-type injector/substrate. Atop the field stop layer, a 160 µm, 2×10^{14} cm^{-3} drift region is designed to support 16 kV. While the base layers vary between designs, the cathode region in both is an n-type layer 2µm thick, with 1×10^{19} cm^{-3} doping, while the horizontal distance between cathode edge and gate edge (D_{wg}) in both designs is fixed at 2 µm and the gate width is 5 µm.

The base region of the conventional design comprises a single p-type layer, 2 µm thick with doping of 1×10^{17} cm^{-3} that is contacted by the gate metal. In the second design, the base consists of three layers, in which a novel highly doped base strip (HDBS), a layer that is 1 µm thick and 2×10^{17} cm^{-3} doped, is sandwiched between two lightly p-type doped regions of 1×10^{15} cm^{-3}, the upper layer above the HDBS being 1 µm thick, the lower layer below being 2 µm thick.

The impact of the P base design has been implemented using Sentaurus TCAD. The simulation physics model includes carrier recombination, mobility and incomplete ionization with respect to 4H-SiC. The carrier lifetime is 2 µs, which is often achieved on commercially available epitaxial layer structures.

The cells are further simulated in a PSPICE test circuit, shown in figure 2, which is used to assess the switching characteristics of the devices.

III. Fundamental Trade Offs

A. On-state Performance

Common trade-offs affect the on-state of the device, regardless of whether it switches as a GTO or IGCT. This includes the optimal base width and p-base doping in Figure 3 and the cathode width in Figure 4. In these designs, except where these values are varied, the conventional design has a gate width of 5 µm, a half cathode width ($W_k/2$) of 5 µm and a base that is 2 µm in length with p-type doping of 1×10^{17} cm^{-3}. A gate current of 10 A is utilised to facilitate the turn on process and to maintain the device in the on-state.

These figures reaffirm that to minimise on state conduction losses, a shorter base length, wider cathode, and lower p-base doping is necessary. However, in Figure 4, it is clear that the benefits of further widening $W_k/2$ beyond 50 µm (more than 90% of the device surface) are minimal. As such, achieving IGCT switching across a W_k=100 µm cathode, is the target of the optimisation work to follow.

B. Switching Performance

As a low frequency high power device, the mitigation of on-state loss needs to be prioritised. However, the turn-off performance is not only important in energy saving but also ensuring its operation as an IGCT, rather than a GTO, which is crucial for the reliability of whole power system.

In Figure 5, the switching performance of the conventional design is assessed for devices with different cathode widths. Devices with a narrower cathode width are shown to take less time to switch off, placing the requirements for efficient switching in conflict with minimising on-state losses.

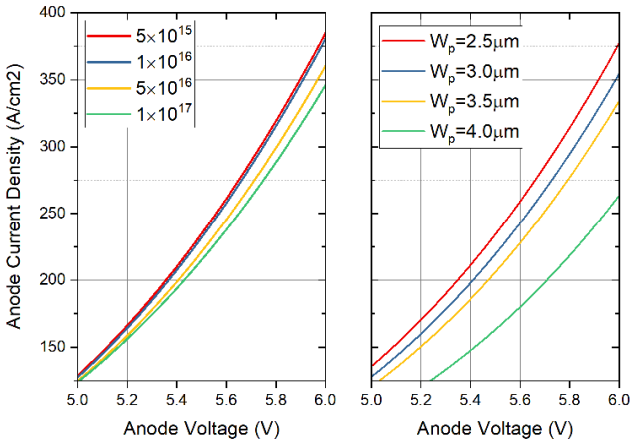

Figure 3: On-state of a conventional IGCT design with (left) different P base doping levels, and (right) different P base lengths.

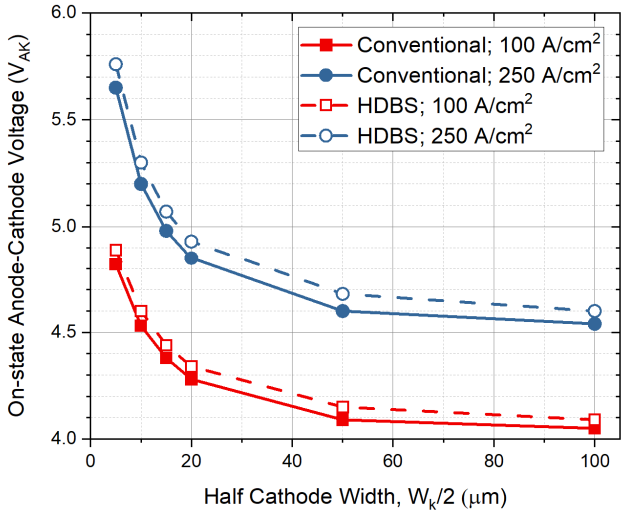

Figure 4: Forward voltage drop of the conventional IGCT design and the HDBS design at 100 and 250 A/cm^2 for different $W_k/2$, and a fixed gate width of 5 µm.

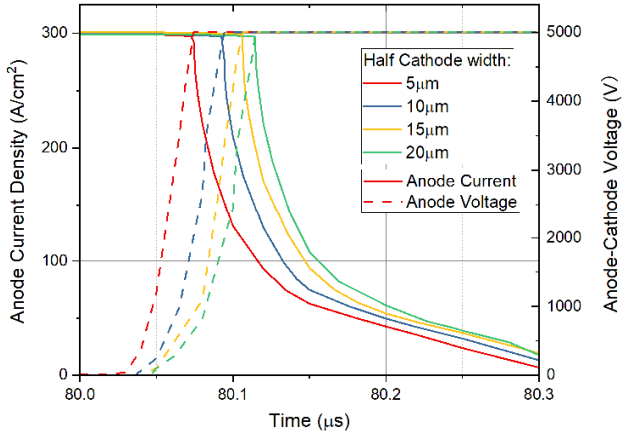

Figure 5: Turn off performance of a conventional IGCT design with cathode widths (W_k) varying from 5 to 20 µm, for a constant gate width of 5 µm, p-base doping of 1×10^{17} cm^{-3}, base length of 2 µm, and a gate reverse bias of 100V.

IV. Ensuring IGCT Operation

In this section, the device operation is explained in detail, including the two conditions required to ensure safe IGCT operation, rather than unstable GTO operation.

A. Condition 1: Commutation via the gate ($t_g \leq t_s$)

Shown in Figure 6 is the ideal IGCT switch-off process, which can be divided into 4 stages. The first interval is a storage time t_s, defined as the time taken from the initial increase in the gate voltage to the time that the anode voltage begins to rise. Concurrently, t_g is defined as the time taken for the initial gate current reaches its negative maximum. The first condition that must be satisfied for stable IGCT turn off behaviour, rather than that of a GTO, is that $t_g \leq t_s$, so ensuring that the gate, rather than the cathode is commutating the current as the voltage rises. In Figure 6, $t_g = t_s$.

In the second period, the anode voltage V_{AK} rises to the DC supply voltage in time t_v. Then, in the third period, the anode current drops rapidly in time t_f. However, a final, more gradual charge extraction period results in a slow decay of the current to zero, lasting time t_i.

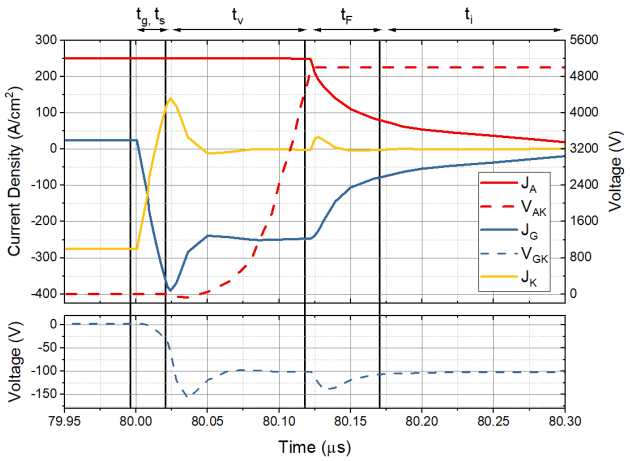

Figure 6: IV curve of IGCT during switching off (J_g: gate current density; I_k: cathode current density; J_a: anode current density; V_a: anode voltage; V_g: gate voltage). The on state current density J_{on} is 250Acm^{-2}, the turning off V_g is -100V and the V_{dc} is 5kV.

To derive the IGCT transition mathematically, first, the total charge removed during time period t_s is:

$$Q_R = \frac{1}{2} I_g . t_s = \frac{1}{2} a . {t_s}^2 \ (1)$$

Where a is the slope of gate current which depends on the applied gate voltage and the external circuitry.

The total stored charge in the P base region can be derive by:

$$Q_{P,base} = qW_P \frac{W_k}{2} Z n_a \ (2)$$

Where W_k is the cathode width and W_P is the length of the P base as shown in figure 1.

The average carrier concentration n_a in the P base under $I_{A,on}$ current flow is given by:

$$n_a = \frac{\tau_{HL}}{q(W_P + W_N)} \left(\frac{2 I_{A,on}}{W_K Z} \right) (3)$$

Where W_N is the length of N drift region and Z is the depth perpendicular to the cross section. τ_{HL} is high level carrier concentration.

Combining equation 2 and 3,

$$Q_{P,base} = \left(\frac{W_P}{W_p + W_N} \right) \tau_{HL} I_{A,on} (4)$$

During turn-off, due to the conservation of charge, $Q_{P,base} = Q_R$, and therefore the storage time t_s can be calculated by:

$$t_s = \sqrt[2]{2 \left(\frac{W_P}{W_p + W_N} \right) \tau_{HL} \left(\frac{I_{A,on}}{a} \right)} \ (5)$$

Meanwhile, the time for gate current to reach the value of anode current is given by:

$$t_g = \frac{I_{A,on}}{a} \ (6)$$

Notable form this derivation is that the cathode width W_k does not feature equations 5 or 6. Rather it is the base

design, in W_P, and the anode current that dictates whether the $t_g \leq t_s$ condition is satisfied or not.

B. *Condition 2: Depleting the entire cathode*

While W_K has little influence on the first condition, it has two major impacts on the device. As the cathode is widened, so the ratio of cathode width to gate width increases. Hence the capacitance associated with the cathode increases proportionally, reducing the anode voltage rise time (dv/dt) and lengthening t_v. This effect can be seen in figure 5 wherein the rise time is fast while the cathode proportion is 50% of the top surface, to the worst case whereby the cathode proportion is 80%

Cathode width also impacts the second IGCT condition. After the storage time t_s, the junction between the cathode and base and between the base and drift region are both reverse biased. As a result, and in the ideal IGCT case, a depletion region will extend across the entire cathode, blocking the path for minority charge (hole) extraction. Instead the charge is collected uniformly in the base and commutated along the p-region to the gate.

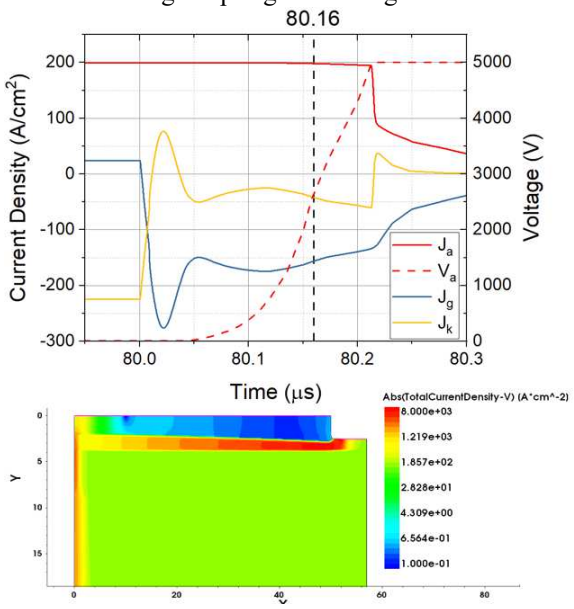

Figure 7: The IV plot of an unsuccessful IGCT turning-off (top) and the respective current density distribution in cathode-base-drift region of the device at a given time point (bottom).

In an unsuccessful IGCT, such as the one seen in Figure 7, the first condition ($t_g \leq t_s$) may be met, but if the cathode is too wide for the given switching conditions, then a failure will result. This occurs because a significant potential voltage difference exists along the p-base region between the cathode centre and the gate, which is the product of the current transport and the low doped p-base resistance. In this case the cathode-base junction no longer remains reverse biased, allowing current to once again flow through the centre of the cathode during the V_{AK} rise period, the device reverting to GTO turn-off, and possible failure.

Therefore, the second condition for IGCT turn-off is that, for the given switching conditions, the cathode must be narrow enough to maintain a depletion region in the centre of the cathode.

The failure of the conventional design can be seen in figure 7 and in figure 8, as the device with the targeted 50 µm cathode width fails to turn off as an IGCT under 200A/cm^2 conducting current and 5kV source voltage. Rather, it turns off as a GTO, because the depletion region (white line) in the cathode has not extended to the centre of the device.

V. IGCT Operation Utilising a Highly Doped Base Strip (HDBS)

One way to optimise a IGCT, to ensure condition 2 is met for the widest possible cathode widths, is to reduce the p-base resistance. This is the purpose of introducing the HDBS into the IGCT design.

In the HDBS design, the doping density in the upper and lower P base layers is reduced from 1×10^{17} cm^{-3} to 1×10^{15} cm^{-3}, though a highly doped strip (2×10^{17} cm^{-3}) remains in the middle of base. The thickness of HDBS is half that of the original P base length, thus ensuring that the total p-type dose in the HDBS P base is similar to (1.5% higher than) the conventional design.

The HDBS results in a number of advantages over the conventional design. First, the HDBS can be imagined as a highway in the middle of the base region for current to pass through. Its higher doping reduces the resistance between gate and cathode electrodes. This provides one of two advantages. If the same cathode width is maintained, the maximum reverse gate current can be increased, leading to a higher current turn-off capability. Alternatively, the HDBS facilitates IGCT action over wider depletion regions for the same gate current, ensuring the cathode remains reverse biased at its centre. This can be seen in the HDBS structure in Figure 8, in which the device with the targeted 50 µm cathode width turns off as an IGCT, the depletion region covering the whole cathode region.

The impact of widening the cathode to 50 µm, more than 90% of the total top surface, is seen in Figure 4, allowing the forward voltage to be reduced to a value close to its minimum. However, from Figure 5, the switching times also approach their maximum, and so the true benefits of widening the cathode depend on the switching speed utilised.

In a like-for-like comparison, in which the cathode widths are the same, the HDBS marginally increases the forward voltage drop compared to the conventional design. From figure 4, there is a 1.8% increase in anode-cathode voltage drop at any equivalent cathode width. However, if the conventional design cannot switch off the widest cathode widths safely, then this is irrelevant.

Switching losses are modestly reduced using the HDBS in the same like-for like comparison. Considering an IGCT with a 20 µm cathode width to be turned off under 5000 V anode voltage and 167 A/cm^2 load current and -100 V gate voltage, the switching power loss of conventional IGCT is 72.5 mJ while IGCT with HDBS only consumes 70.5 mJ, which is 2.8% improvement.

Finally, the lower doped region above the HDBS can reach a higher electric field (figure 9), which enhances the reverse blocking capability between the cathode and gate compared to the conventional design, from 150 V to 270 V in these designs. This in turn greatly increases the

reliability of the IGCT in an ultra-high power system. At the same time, higher turn-off gate voltage can be applied to achieve shorter switching times.

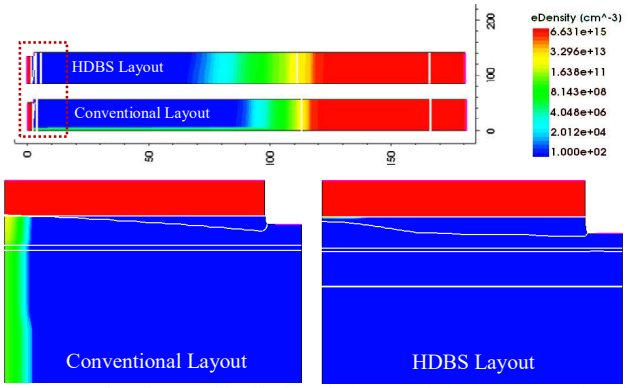

Figure 8: The electron distribution during t_V of the conventional and HDBS design thyristors (White line: depletion region edge). In both designs $W_k/2$=50 µm.

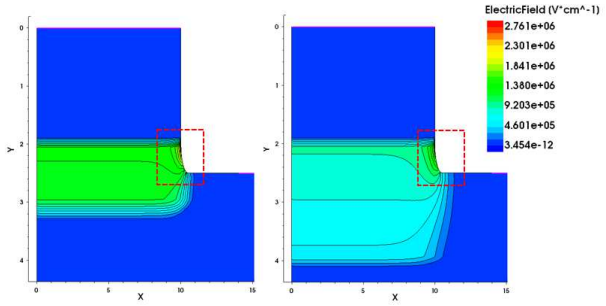

Figure 9: Electric filed distribution @Vgk=-140V (left: conventional IGCT; right: IGCT with HDBS

VI. Conclusion

In summary, the optimisation of an IGCT, produced in SiC for a 15kV design, has been explored for the first time. The conditions that will ensure the safe turn off of the device as an IGCT rather than a GTO have been defined. These are first that the gate current must rise to its maximum value, ensuring current via the gate rather than the cathode, before the anode voltage begins to rise. The second condition is that the cathode-base p-n junction must remain reverse biased across its entire length during the voltage rise time period, thus limiting the width of the cathode for the given conditions. A highly doped base strip (HDBS) is introduced to help satisfy this second condition. Providing a highly doped, low resistance path for hole transport, this allows the cathode to be extended such that it makes up 90% of the top surface, so in turn minimising on-state losses. The HDBS has secondary benefits, including the ability to increase the maximum gate voltage, which reduces switching losses and improves switching.

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