Matrix Converter Open Circuit Fault Behavior Analysis and Diagnosis with a Model Predictive Control Strategy

Jiawei Zhang, Hanbing Dan, Lee Empringham, Liliana De Lillo, and Patrick Wheeler

***Abstract*—A novel fast and reliable open circuit fault diagnosis strategy for a Matrix Converter with a Finite Control Set Model Predictive Control strategy is proposed in this paper. Current sensors are located ahead of the clamp circuit to measure the output currents in order to improve the speed of fault diagnosis. In addition, the current recirculating path during a single open circuit switch fault condition is given in detail with the aim of contributing more expert knowledge to the fault diagnosis. The proposed fault diagnosis method is applicable over the whole range of modulation index.**

***Index Terms*—Current Recirculation, Clamp Circuit, Direct Matrix Converter, Fault Diagnosis, Finite Control Set Model Predictive Control.**

I. Introduction

DIRECT Matrix Converters (DMCs) can realize AC to AC power conversion with minimal requirements for passive components [1] as shown in Fig. 1. The topology comprises of a bidirectional switch matrix which connects the output lines directly to the input lines. The MC topology possesses advantages such as compact power circuit topology, the possibility of higher power density [2], controllable input power factor [3], [4], and removal of the need for bulky DC-Link component [5]. Without the DC-Link component the MC topology can be used as a substitute for the traditional back-to-back PWM converter topology in volume and weight critical applications such as aerospace. However, the removal of the DC-Link component also means that any power pulsations at the MC output side will also be present at the input side. Therefore, the MC topology is more suited to constant power loads than pulsed loads [1]. The MC topology is very suitable for applications such as induction machines and permanent-magnet synchronous machines drives.

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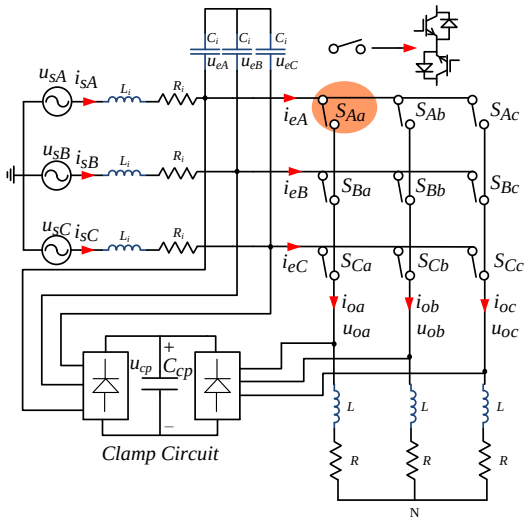

Fig. 1: Direct matrix converter topology

An industry survey claims that the failure of the power devices counts for 38% of the total faults in variable speed AC motor drives [6]. Since the MC topology is composed of semiconductor switches the reliability of the devices is a big concern. Prognosis assesses the current health of a component, and predicts the health of the component at some point in the future [7]. Prognosis is a very challenging task because it needs a very good reliability model of the components. Condition monitoring is when the system measures the condition of a component in real-time, an appropriate action will be taken if the parameters drift away from the healthy condition. Condition monitoring techniques require sensing and signal processing as well as the knowledge of semiconductor device failure mechanisms, which will increase the hardware complexity and cost. Diagnosis is to identify the root cause of a fault, given that a fault has occurred. Diagnosis techniques are still a more cost-effective way compared with prognosis and condition monitoring because it requires less or even no hardware complexity.

A fault may occur during the matrix converter (MC) system lifetime. A semiconductor device can either fail as a short circuit or an open circuit fault. Most of the short circuit fault detection and diagnosis methods are hardware circuit based rather than software based [7]. This is because the time interval between the fault initiation and failure is too small to implement a software based detection method [8]. When an open circuit fault occurs, the MC may not suffer catastrophic failure immediately. However, if the open circuit fault cannot be detected, diagnosed, and isolated in time, accumulated over-voltage stress on the power devices will cause further damage on the MC system and can lead to catastrophic failure. This paper will focus on the open circuit switch faults in the MC system.

The fault detection and diagnosis methods for power converters proposed in the literature can be divided into two categories: the signal processing-based methods [9] and the analytical model-based methods [10]–[18]. In [9], a Fast Furrier Transformation (FFT) is used to analyze the spectral components in the output current, but this method cannot locate the fault to the exact bidirectional switch because the spectral components of each faulty device in one output phase are similar. Considering the analytical model-based fault diagnosis methods, in [10], the matrix converter output voltage is captured by three additional voltage sensors and used for fault detection purpose, which can locate the fault to a particular output phase. The work presented in [11] improves the output error voltage method by implementing nine modulated error voltages to locate the fault to one switch.

In [12], a MC fault diagnosis method is proposed which relies on the reduction of the MC output currents with specific conditions satisfied such as the input-output voltage space vectors and power switches duty-cycle limitation under the Optimized Alesina-Venturini (OAV) modulation method. However, the integration of output currents will slow down the fault detection process. In [13], a fault detection method based on the clamp circuit capacitor current measurement is proposed. An additional current sensor is used in this method and the fault detection process is slowed down by the integration of the clamp circuit current. In [15] a fault diagnosis method which relocates the three output current sensors ahead of the clamp circuit to directly measure the matrix converter output currents within three different zero vectors is proposed. However, the zero vector duty-cycles are extremely small and hard to capture with high modulation ratios. In [16], a fault diagnosis method relying on the load currents decreasing to zero is proposed under Finite Control Set Model Predictive Control (FCS-MPC). However, the speed of the proposed fault diagnosis method is slowed down by waiting for the load current to drop to zero.

This paper presents a novel, fast and reliable online fault diagnosis method which can locate an open-circuited fault with significant improvements of speed and modulation index range. The output current sensors are located ahead of the clamp circuit to measure the DMC output currents. In addition, the expert knowledge of the DMC open circuit current recirculating path is implemented in the fault diagnosis method to avoid false diagnosis [19]. The proposed methodology is validated with experimental results.

II. DMC System with FCS-MPC strategy

The DMC topology is shown in Fig. 1. The DMC system is composed of an input filter, a switch matrix of nine bidirectional switches and a clamp circuit. The input filter attenuates the switching frequency harmonics of the input currents of the DMC. The switch matrix connects the three phase input source directly to the three phase output load. The clamp circuit, which consists of 12 fast-recovery diodes and a capacitor, connects in parallel with the DMC to avoid over-voltage damage on the bidirectional switches.

A. Clamp Circuit

Since there is no free-wheeling device in the DMCs, so a clamp circuit must be added to protect the DMCs from over-voltage when an open-circuit fault occurs, which could destroy the power semiconductor devices. A typical clamp circuit is shown in Fig. 2. The clamp circuit is connected between the three phase input supply and the load terminals of the converter. This clamp circuit consists of two fast-recovery diode rectifier bridges, a clamp capacitor and a dissipation resistor. During an open circuit switch fault, the reactive energy stored in the load inductance is transferred to the clamp capacitor and then is dissipated in the resistor.

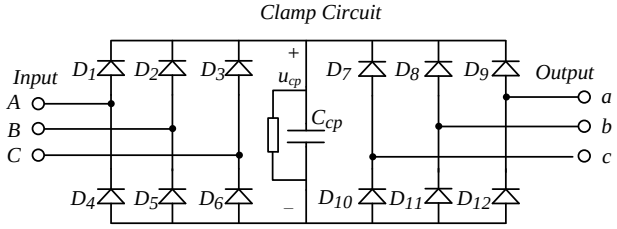

Fig. 2: Clamp Circuit for the DMC

If an open circuit fault occurs, the faulty phase current will first recirculate in the clamp circuit. The current recirculating path is decided by three factors. The three factors are the direction and amplitude of faulty phase current, the input source voltages and the switching states, respectively. If the faulty output phase is clamped to the positive bus of the clamp circuit, the faulty current will flow through the diodes which connect to the most negative voltage as shown in Fig. 3.

Similarly, if the faulty output phase is clamped to the negative bus of the clamp circuit, the faulty current will flow through the diodes which connect to the most positive voltage. In addition, The currents recirculating in the DMC output, the clamp circuit and the load current satisfy the Kirchhoff Current Law (KCL) as expressed in (1). Where $i_{out}(n)$, $i_{clamp}(n)$ and $i_{load}(n)$ are the three phase DMC output currents, the clamp circuit output side currents and the load currents, respectively.

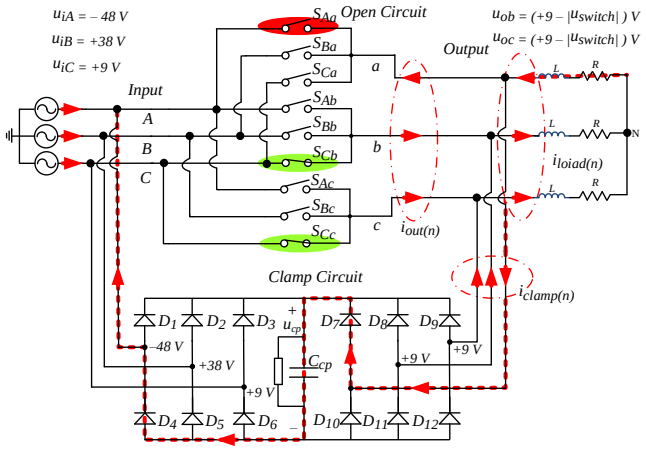

Fig. 3: The faulty output phase current recirculating behavior in the clamp circuit of the DMC

$$\sum_{i=1}^{3} i_{load}(n) = \sum_{i=1}^{3}(i_{out}(n) + i_{clamp}(n)) = 0$$
$$\sum_{i=1}^{3} i_{out}(n) = -\sum_{i=1}^{3} i_{clamp}(n) \tag{1}$$

B. FCS-MPC strategy

FCS-MPC strategy enables the controlled variables to achieve the corresponding reference at the end of each sampling period by predicting the controlled variables two steps ahead in one sampling period. The first prediction step compensates one period delay of the DSP-FPGA control platform. The second prediction step predicts the expecting value of the controlled variables in the next sampling period. The load current can be predicted by using forward Euler approximation, and the prediction of the source current and input voltage are acquired using a discrete input filter model as shown in (2). Where constants F_1 and F_2 depend on the load parameters and the sampling time T_s. D_1, D_2, D_3, D_4, E_1, E_2, E_3 and E_4 depend on the input filter parameters and the sampling time T_s [16], [20], [21].

$$\begin{aligned} i_o^{k+1} &= F_1 u_o^k + F_2 i_o^k \\ i_s^{k+1} &= D_1 u_s^k + D_2 u_e^k + D_3 i_s^k + D_4 i_e^k \\ u_e^{k+1} &= E_1 u_s^k + E_2 u_e^k + E_3 i_s^k + E_4 i_e^k \end{aligned} \tag{2}$$

FCS-MPC strategy uses cost functions to select the suitable switching state in the next sampling period. Cost functions can be defined differently depending on what the control aim is. This paper defines the cost functions g_1, g_2 and g based on the input and output current quality as shown in (3). The next sampling period switching state N with minimum cost $g[N]$ is chosen as shown in (4). Where $\Delta i_{s\alpha}$, $\Delta i_{s\beta}$, $\Delta i_{o\alpha}$ and $\Delta i_{o\beta}$ are the errors between the reference value and the predicted value of the input-source and output-load currents in $\alpha - \beta$ coordinate. λ is the weighting factor.

$$\begin{aligned} g_1 &= \Delta i_{s\alpha}{}^2 + \Delta i_{s\beta}{}^2 \\ g_2 &= \Delta i_{o\alpha}{}^2 + \Delta i_{o\beta}{}^2 \\ g &= \lambda g_1 + g_2 \end{aligned} \tag{3}$$

$$g[N] = min\{g^{k+2}[i]\} \tag{4}$$

III. DMC Current Recirculating Analysis Under Single Switch Open Circuit Fault Condition

It is of significant importance to know how current will recirculate in the clamp circuit during an open circuit fault condition. The currents recirculating expert knowledge is essential to improve the speed and precision of the output-current-based fault diagnosis methods, because the faulty output phase current will affect the currents of the healthy output phases by current recirculating and causes false-diagnosis in the fault diagnosis process eventually. When a bidirectional switch occurs an open circuit fault, the load current of the faulty output phase will recirculate through the clamp circuit. Then the recirculating current in the clamp circuit will either flow back to other phases of the load, or flow into the input source, DMC and then back to the load. The specific current recirculating path is decided by three factors. These three factors are the load current direction, the switching state, and the input voltages. There are two types of current recirculating paths that the faulty output phase load current can flow through. The type 1 current recirculating path means that the faulty output phase load current will flow through the clamp circuit, then flow into the input source, the DMC and finally flow back to other phases of the load. In type 1 path, there are still currents flowing through the DMC output side. The type 2 current recirculating path means that the faulty output phase load current is the biggest absolute value among the three output load currents, and will flow through the clamp circuit and then flow back to other phases of the load directly.

The key difference between type 1 path and type 2 path is the current difference of the healthy phases of the DMC output. Both of the currents of the healthy phases of the DMC output will not be zero in type 1 path. However, at least one current of the healthy phases of the DMC output will be zero in type 2 path.

A. *Type* 1 *Current Recirculating Path*

Type 1 current recirculating path includes the faulty phase of the load, the clamp circuit, the input source, the DMC and other phases of the load. Moreover, both of the currents of the healthy phases of the DMC output will not be zero in type 1 path. For instance, the bidirectional switch S_{Aa} occurs an open circuit fault at the time point t_k. The three phase input voltages at t_k are $u_{iA} = -48V$, $u_{iB} = +38V$ and $u_{iC} = +9V$, respectively. The faulty output phase current i_{oa} is flowing out from the load, and the healthy output phases currents i_{ob} and i_{oc} are flowing into the load. The bidirectional switches which are conducting at t_k are S_{Aa}, S_{Cb} and S_{Cc}, respectively. Under these conditions, the faulty output phase current i_{oa} will first flow into the clamp capacitor C_{cp} through diode D_7. Then the current will continue to flow through the diode D_4 because of the input voltages as well as the nature of the diode bridge. Next, the current will continue to flow through the input voltage sources U_{sA}, U_{sC} and through the DMC due to the switching state condition. Finally, the current will flow back into the load phases b and c and create a complete current recirculating path for the faulty output phase current i_{oa}. The type 1 current recirculating path under these specific conditions is shown in Fig. 4.

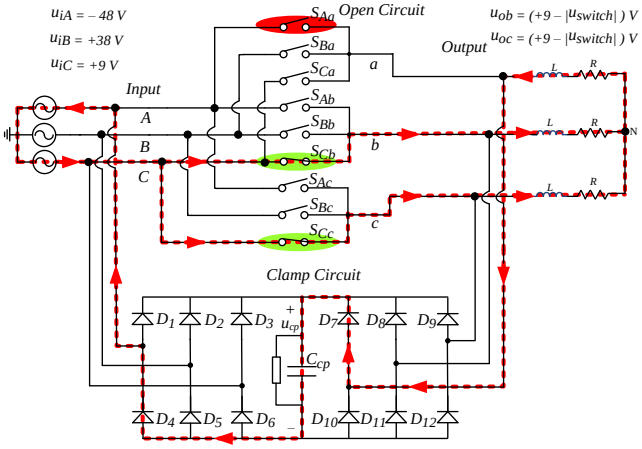

Fig. 4: Type 1 current recirculating path

B. *Type* 2 *Current Recirculating Path*

Type 2 current recirculating path includes the faulty phase of the load, the clamp circuit, and other phases of the load. In addition, the faulty output phase load current is the biggest absolute value among the three output load currents in type 2 path. Last but not least, at least one current of the healthy phases of the DMC output will be zero in type 2 path. For instance, the bidirectional switch S_{Aa} occurs an open circuit fault at the time point t_l. The three phase input voltages at t_l are $u_{iA} = -20V$, $u_{iB} = +48V$ and $u_{iC} = -28V$, respectively. The faulty output phase current i_{oa} is flowing out from the load, and the healthy output phases currents i_{ob} and i_{oc} are flowing into the load. The bidirectional switches which are conducting at t_k are S_{Aa}, S_{Cb} and S_{Bc}, respectively. Under these conditions, the faulty output phase current i_{oa} will first flow into the clamp capacitor C_{cp} through diode D_7. Then the current will be divided into two paths. One path will flow through diode D_6 and the other will flow through diode D_{11} because of the input voltages as well as the nature of the diode bridge. Next, the current flowing from the diode D_{11} will flow into load phase b, and the current flowing from the diode D_6 will continue to flow through the input sources and the DMC and back to load phase c eventually. Since the load current i_{ob} is supplied by the faulty phase current i_{oa}, so there will be no current in the DMC output phase b. The type 2 current recirculating path under these specific conditions is shown in Fig. 5.

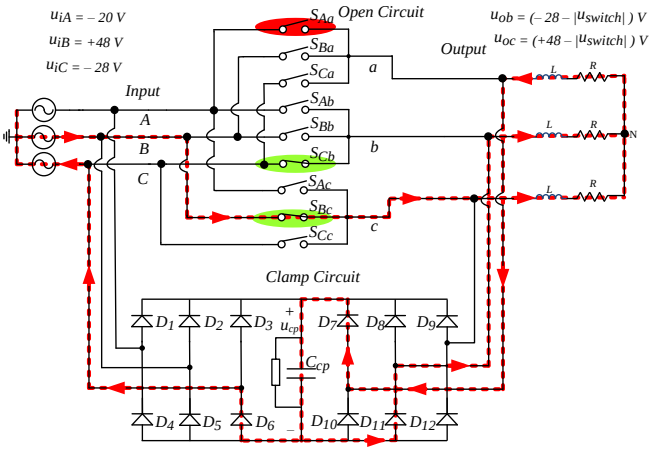

Fig. 5: Type 2 current recirculating path

C. *Comparison between Type* 1 *and Type* 2 *current recirculating paths*

The comparison between type 1 and type 2 current recirculating paths are presented in TABLE I. In conclusion, type 2 path will cause at least one healthy output phase current of the DMC to reduce to zero due to the influence by the faulty phase current, the input source voltages and the switching states at the same time. A type 2 path can occur if

two conditions are satisfied at the same time:
• the actual faulty output phase current is the biggest absolute value;
• at least one of the healthy output phase voltage is the most negative when the faulty phase current direction is flowing into the clamp circuit, or at least one of the healthy output phase voltage is the most positive when the faulty phase current direction is flowing out from the clamp circuit.

TABLE I: Comparison between type 1 and type 2 paths

	Type 1 path	*Type 2 path*
Is the faulty phase current the biggest absolute value?	No	Yes
Does the faulty phase DMC output current reduce to zero?	Yes	Yes
Does the healthy phase DMC output current reduce to zero?	No	Yes

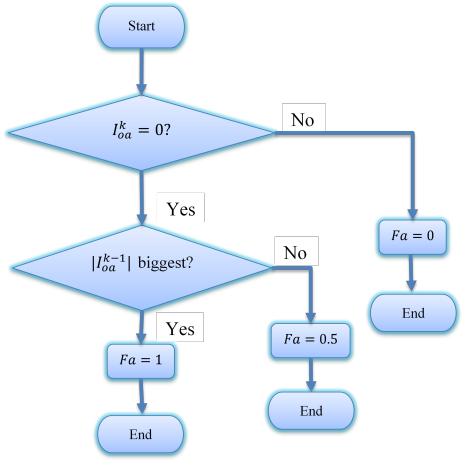

Fig. 6: Flow chart of the fault detection for phase a

D. False Diagnosis

In terms of the fault diagnosis method proposed in [15] that the output current sensors are located ahead of the clamp circuit to measure the DMC output current, a false-diagnosis will occur if there is a type 2 current recirculating path. Because the current sensor located in a healthy output phase of the DMC will detect a zero current, and a faulty flag will be generated indicating an open circuit fault occurring in the healthy output phase. Therefore, the current recirculating expert knowledge presented in this paper will avoid the false-diagnosis occurs in [15].

IV. Fault Diagnosis Method

In order to avoid any false-diagnosis during the whole fault detection process, the clamp circuit current recirculating expert knowledge is required to be implemented into the fault detection algorithm. The faulty output phase current may recirculate through the clamp circuit and provide current supply for a healthy phase load current. This type of current recirculation will cause the output current sensor to detect a zero current. Therefore, a false-diagnosis can be avoided by implementing the clamp circuit current recirculating expert knowledge. The output phase a current I_{oa} of the direct matrix converter will be detected in every sampling period as shown in Fig. 6. Fault diagnosis algorithm for I_{ob} and I_{oc} is exactly the same as for I_{oa}.

First, the output currents i_{oa}^{k}, i_{ob}^{k} and i_{oc}^{k} in the sampling period T_s^k will be checked whether or not are zero. If the current is not zero, the fault detection algorithm will make a decision that there is no open circuit fault in the corresponding output phase and set the corresponding flag to 0. If the current is zero, then the fault detection algorithm will check which of the output currents i_{oa}^{k-1}, i_{ob}^{k-1} and i_{oc}^{k-1} in the sampling period T_s^{k-1} is the biggest absolute value comparing the other two. If the output current has the biggest absolute value, the fault diagnosis algorithm will make a decision that there must be the corresponding output phase occurring an open circuit fault and set the corresponding flag to 1. If the output current does not have the biggest absolute value, the fault detection algorithm will make a decision that there might be the corresponding output phase occurring an open circuit fault and set the corresponding flag to 0.5.

Once the fault detection algorithm for each output phase is finished, the switching state information of the present sampling period T_s^k will be used by the fault diagnosis algorithm to identify the specific bidirectional switch in the faulty phase as shown in (5). Since this section focuses on single bidirectional switch open-circuited fault, the switch which has the highest possibility of fault will be identified as a faulty switch.

$$\begin{bmatrix} F_{Aa} & F_{Ba} & F_{Ca} \\ F_{Ab} & F_{Bb} & F_{Cb} \\ F_{Ac} & F_{Bc} & F_{Cc} \end{bmatrix} = \begin{bmatrix} F_a & 0 & 0 \\ 0 & F_b & 0 \\ 0 & 0 & F_c \end{bmatrix} \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \tag{5}$$

Ideally, the proposed fault diagnosis method can locate the fault within one sampling period. The speed of the fault diagnosis method would not be affected by an output current filter due to the output current sensor location. The only limitation in this fault diagnosis method is that it cannot detect a fault when the output current is at natural zero-crossing point.

TABLE II: The experimental parameters of bench rig

Variables	*Description*	*Value*
V_s	*Amplitude AC Phase Voltage*	$50[V]$
L_f	*Input Filter Inductor*	$273[\mu H]$
C_f	*Input Filter Capacitor*	$72[\mu F]$
R_f	*Input Filter Resistor*	$0.08[\Omega]$
R_{load}	*Load Resistor*	$12[\Omega]$
L_{load}	*Load Inductor*	$17[mH]$
T_{sample}	*Sampling Time*	$100[\mu s]$
I_{out}	*Output Current Amplitude*	$2.5[A]$
f_{out}	*Output Current Frequency*	$60[Hz]$

V. Experimental Results

In the experimental implementation, the FCS-MPC strategy [16], [20] is used to control the DMC. The advantage of using FCS-MPC strategy is that there is only one fixed switching state applied in each sampling period, which will simplify the switching states capturing process in the DSP-FPGA control platform. The output current sensors are located ahead of the clamp circuit to measure the DMC output currents directly as shown in Fig. 7. The experimental parameters are presented in TABLE II. The experimental bench rig is shown in Fig. 8.

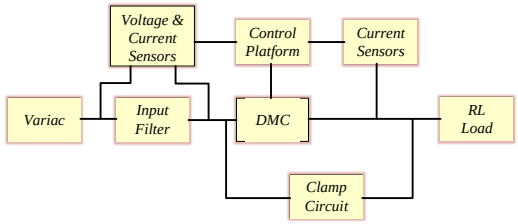

Fig. 7: Experimental rig set up diagram

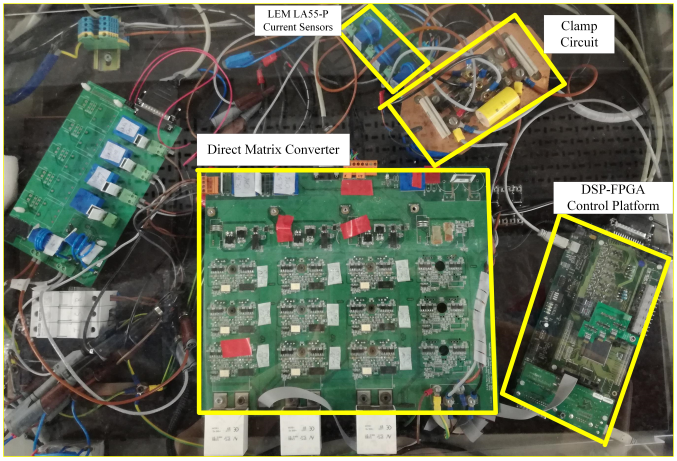

Fig. 8: Experimental bench rig

In the experiment, the experimental results of input phase voltage U_{sA}, output line-to-line voltage U_{oca}, and output current i_{oa} under normal condition are shown in Fig. 9. Then the bidirectional switch S_{Aa} is triggered to be open circuit for $1ms$ and then set back to normal operation immediately for safety purpose. This is because if the open circuit switch fault can not be detected, diagnosed, and isolated in time, accumulated over-voltage stress on the power switches will cause further damage on the MC system and can lead to catastrophic failure eventually.

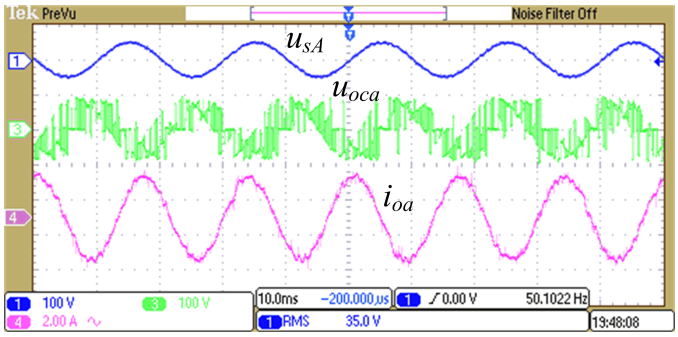

Fig. 9: Input phase voltage U_{sA}, output line-to-line voltage U_{oca}, and output current i_{oa} under normal condition

A. *Type* 1 *Path Results*

The DMC output three phase currents i_{oa}, i_{ob}, and i_{oc} under the bidirectional switch S_{Aa} open circuit fault condition is shown in Fig. 10. The magnified waveforms of the switching states, the DMC output currents, and the input voltages during the open circuit fault period are presented in Fig. 11. The bidirectional switch S_{Aa} occurs an open circuit fault at $0.3ms$. The type 1 current recirculating path presented in Fig. 4 occurs at $0.4ms$ as shown in Fig. 11. The three phase input voltages at t_k are $u_{iA} = -48.0V$, $u_{iB} = +38.5V$ and $u_{iC} = +9.5V$, respectively. The faulty output phase current i_{oa} is flowing out from the load, and the healthy output phases currents i_{ob} and i_{oc} are flowing into the load. The bidirectional switches which are conducting at t_k are S_{Aa}, S_{Cb} and S_{Cc}, respectively. From the experimental results it can be seen that there is current flowing in the DMC healthy output phases b and c.

B. *Type* 2 *Path Results*

The DMC output three phase currents i_{oa}, i_{ob}, and i_{oc} under the bidirectional switch S_{Aa} open circuit fault condition are shown in Fig. 12. The magnified waveforms of the switching states, the DMC output currents, and the input voltages during the open circuit fault period are presented in Fig. 13. The bidirectional switch S_{Aa} occurs an open circuit fault at $0.3ms$. The type 2 current recirculating path presented in Fig. 5 occurs at $0.4ms$ as shown in Fig. 13. The three phase input voltages at t_l are $u_{iA} = -22.4V$, $u_{iB} = +48.4V$ and $u_{iC} = -26.0V$,

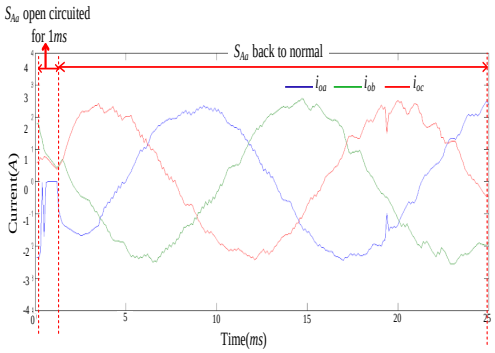

Fig. 10: The DMC output currents under type 1 faulty phase current recirculating path occasion

respectively. The faulty output phase current i_{oa} is flowing out from the load, and the healthy output phases currents i_{ob} and i_{oc} are flowing into the load. The bidirectional switches which are conducting at t_k are S_{Aa}, S_{Cb} and S_{Bc}, respectively. From the experimental results it can be seen that there is no current flowing in the DMC healthy output phase b.

C. Fault Diagnosis Results

The results during the open-circuited period are magnified and shown in Fig. 14 and Fig. 15. It can be seen that the DMC output current i_{oa} drops to zero immediately when switch S_{Aa} is triggered to be open-circuited and keeps zero during the whole open-circuited period. So the open-circuited flag F_{Aa} is set to 1 by the proposed fault diagnosis system. According to literature [19], if the absolute value of the open-circuited faulty output phase current is the biggest among the three output phase currents, The healthy output phases currents could be influenced by the faulty phase current to decrease to zero. This expert knowledge is contributed to the proposed fault diagnosis system to avoid false-diagnosis. Since the absolute value of the current i_{oa} is the biggest among the three currents, so the current i_{ob} dropped to zero for two sampling periods. In these two sampling periods, the open-circuited flag F_{Bc} is set to 0.5 respectively by the proposed fault diagnosis system by using the present switching state information, which are obtained directly from the FPGA card. Since this paper focuses on single-switch open-circuited fault occasion, so only the switch S_{Aa} with the highest faulty possibility is detected as open-circuited. The switch S_{Bc} is considered as healthy switch due to lower faulty possibility. Therefore, a false diagnosis can be avoided.

One drawback of the proposed method is that it will diagnose an open-circuited fault during the natural zero crossing. Therefore, at least two sampling periods are needed to guarantee the currents are not experiencing natural zero crossing. The

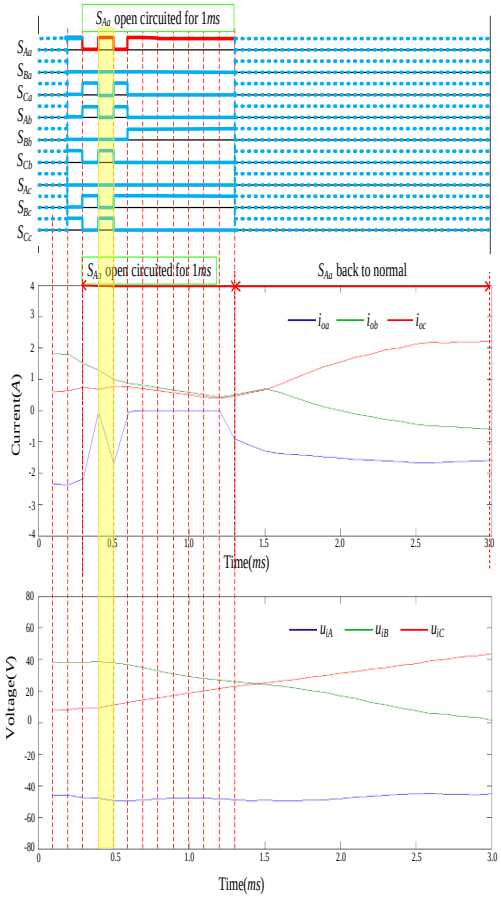

Fig. 11: Magnified waveforms of the switching states, the output currents, and the input voltages of the DMC under type 1 faulty phase current recirculating path occasion

number of sampling periods needed also depends on the output frequency and amplitude. The lower the output frequency and the lower the amplitude, the more numbers of sampling periods are needed to avoid natural zero crossing.

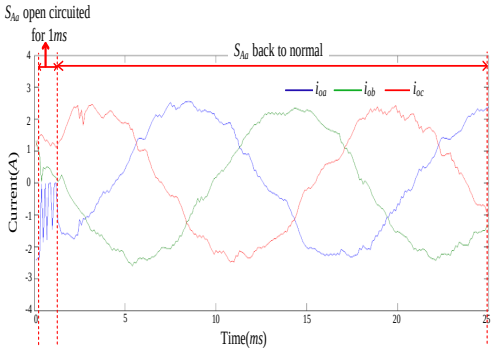

Fig. 12: The DMC output currents under type 2 faulty phase current recirculating path occasion

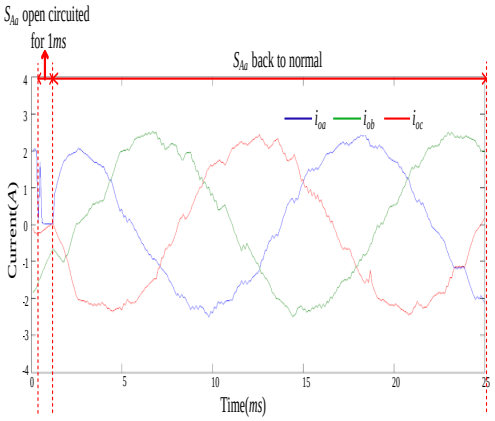

Fig. 14: output currents under open circuit fault condition

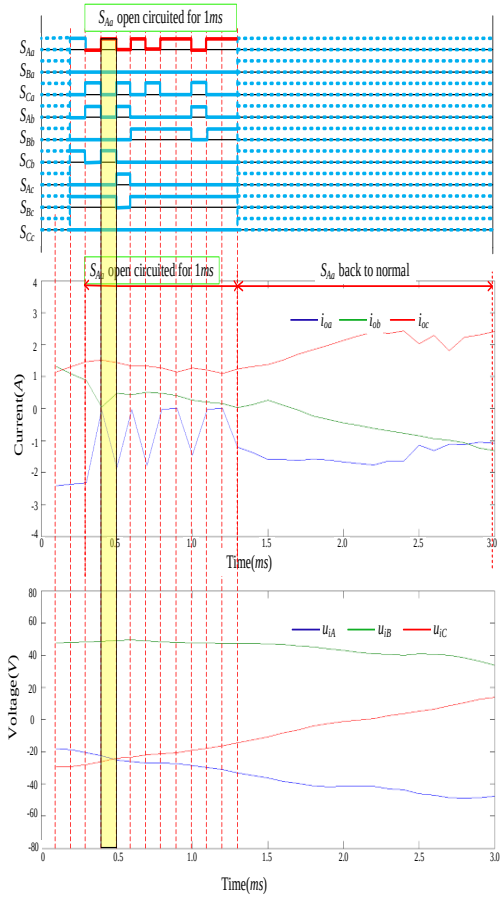

Fig. 13: Magnified waveforms of the switching states, the output currents, and the input voltages of the DMC under type 2 faulty phase current recirculating path occasion

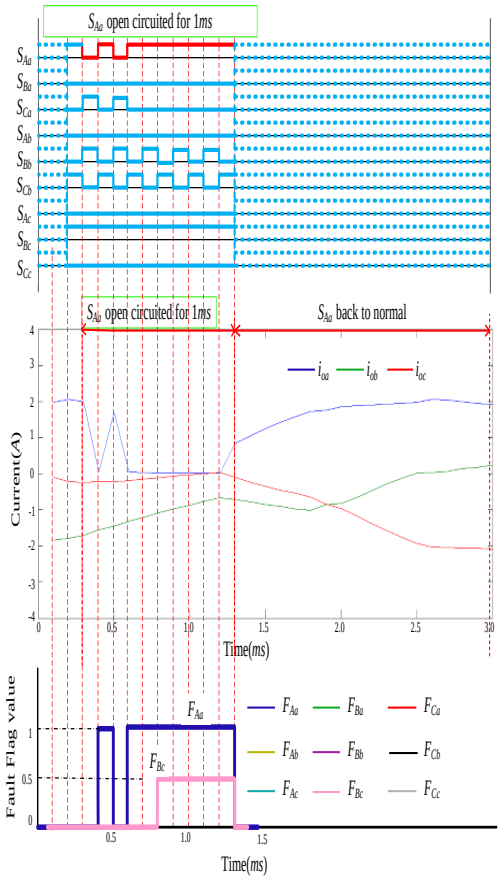

Fig. 15: Magnified output currents under open circuit fault condition

VI. Conclusion

This paper has proposed a novel online open-circuited fault detection and diagnosis method for DMC with FCS-MPC strategy. The proposed method has been validated experimentally. The three output current sensors are located ahead of the clamp circuit to measure the matrix converter output current directly. In addition, the faulty phase current recirculating expert knowledge is investigated in this paper to avoid false-diagnosis. The faulty phase current recirculating path is decided by three factors. These three factors are the direction and amplitude of faulty phase current, the input source voltages and the switching states, respectively. The current recirculating path could cause at least one healthy output phase current of the DMC to reduce to zero due to the impact by the faulty phase current, the input source voltages and the switching states. Ideally the proposed method can locate an open-circuited switch fault in one sampling period, which significantly improves the speed and the precision of the fault detection and diagnosis progress comparing with the method in [16]. In addition, the proposed fault diagnosis method is applicable within the whole range of modulation index comparing with the presented method in [15], which can only be applied during low modulation index occasion. The proposed fast and reliable fault diagnosis method can guarantee the correct use of fault tolerant strategy.

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