P-gate GaN HEMT gate-driver design for joint optimization of switching performance, freewheeling conduction and short-circuit robustness

Han Wu, Asad Fayyaz, Alberto Castellazzi
Power Electronics, Machines and Control Group
University of Nottingham
Nottingham, UK

asad.fayyaz@nottingham.ac.uk; alberto.castellazzi@nottingham.ac.uk

Abstract—This paper proposes the design and prototype development and testing of a gate-driver which enables to jointly optimize the performance in application of gate-injection type high electron mobility transistors, taking into account a number of diverse operational conditions, including nominal and abnormal events. The results show that it is possible to optimize the gate-driver parameters in such a way as to ensure optimum switching and free-wheeling performance, while ensuring enhanced short-circuit robustness.

Keywords—GaN HEMTs; GaN GITs; gate-drivers; wide-band-gap semiconductors.

I. INTRODUCTION

GaN transistors are finding rapidly growing interest in power conversion applications, where fully GaN normally-off solutions are oftentimes the preferred choice. In this work, the focus is in particular on devices in the 650 V rating class, of ample interest for automotive and renewable energies applications. Among the few commercially available packaged device options, p-gate type gate injection transistors (GIT) have been demonstrated in previous works to offer excellent performance in application, to show very good promise for high robustness and longer term reliability, while requiring some specific gate-driver design features for best operation [1-4]. Recently, a hybrid-drain (HD) GIT device has been introduced, which significantly advances well known issues related to current collapse in GaN HEMT technology [5]. The specific device under analysis in this work is the PGA26E19BA transistor, with a nominal DC current rating of 13 A [6].

Fig. 1 reports data-sheet information for the gate-source p-n junction type characteristics, together with the device output characteristics. As can be seen, although a threshold-voltage is specified for the transistor, it is actually not fully voltage-driven; in other words, the gate and drain current, I_D , are not independent one of the other. Moreover, as visible in Fig. 1 a), the gate bias current increases with temperature for a given gate-source bias voltage. The investigations of [7] have also shown that for a given drain current value, the on-state resistance does not vary significantly increasing the gate bias current value from a few mA to several tens of mA.

Fig. 1: GaN GIT gate-source *p-n* junction characteristics, a), and output-characteristics at 25 °C, b) (data-sheet information, PGA26E19BA).

Based on these preliminary considerations, this work proposes the development of a bespoke original gate-driver design, which addresses all the main needs for device performance optimization in real operational conditions.

II. GATE DRIVER DESIGN

The device-manufacturer recommended design for the terminal stage of the gate driver is shown in Fig. 2: this design optimizes the switching transitions in terms of application of a fast gate voltage and current peak at turn-on and turn-off, controlled by the values of $R1$ and C , followed by a region of current limitation, according to the on-state characteristics discussed above, controlled by the value of $R2$, which also controls the discharge rate of C during the off-state along with $R1$. The corresponding gate-source voltage, V_{GS} , drive waveform is illustrated in Fig. 3 a). In particular, with this design, due to the relatively high value of $R2$ needed to limit the gate current, the off-state voltage remains negative throughout the off-state period. This solution is not satisfactory in guaranteeing optimum device switching performance in real applications. Indeed, in a real switching converter, the most typical situation is that a half-bridge connection of a high-side and low-side transistors (HST, LST) is switched on and off alternately, with a *dead-time* between commutations to avoid current shoot-through phenomena, as schematically illustrated in Fig. 3 b). During the dead-times, the load current freewheels in one of the two switches, which

Fig. 2: Recommended gate-driver power stage design.

is then biased in the third quadrant of its output characteristics: device performance in this region of operation is strongly dependent upon the applied V_{GS} : higher losses are associated with more negative V_{GS} values. Experimental results in support of that are presented in Fig. 4 a). Moreover, switching tests reveal that when the device is turned-on again, the transition is much faster and efficient if the off-state V_{GS} value is closer to zero, as clearly visible in the results of Fig. 4 b). in which the curve labelled GaN-HEMT corresponds to a turn-on transition from a negative V_{GS} value; the curve labelled GaN-HEMT-Z corresponds to a turn-on transition from a zero V_{GS} value.

Thus, to improve both free-wheeling and switching performance, the gate-driver design was enhanced with the addition of the diode-resistor network, shown in Fig. 5 a), which effectively by-passes $R2$ during the off-state: the discharge rate of C is now controlled by $R1$ and $R3$ and can be made much faster, while enabling more freedom for the value of $R2$, that is, of the nominal on-state drive current. Simulation

a)

b)

Fig. 3: a); V_{GS} waveform corresponding to the recommended gate-driver design, a); illustration of typical half-bridge switching sequence, including dead-times, b).

a)

b)

Fig. 4: Measured 1st and 3rd quadrant output characteristics of the GaN GIT for various V_{GS} values, a); measured drain-source voltage and drain current waveforms at turn-on, for two different values of off-state V_{GS} , b)

results illustrating the faster discharge to zero of C are shown in Fig. 5 b). The value of C can also be used to the same aim to some extent, but reducing it too much causes a too low on-state V_{GS} value. The solution implemented here allows much more freedom in shaping the driving waveform according to the needs.

Fig. 5: Gate-driver design improvement, a), to achieve rapid return to zero of V_{GS} during turn-off, b), for improved free-wheeling and turn-on switching performance: the $D1$ - $R3$ network bypasses $R2$, enabling a faster discharge of C , controlled by the values of $R1$ and $R3$.

Finally, recent investigations have shown that GaN GITs have the potential to offer excellent short-circuit robustness, provided that the large gate and drain charge injection taking place during the turn-on transient are duly limited, for example by reducing the V_{GS} peak at turn-on [8]. To this aim, the gate-driver design was further enhanced here with the addition of a clamp circuit for the gate terminal, as shown in Fig. 6 a). This solution effectively reduces the short-circuit drain and, correspondingly, gate current peak, without compromise on nominal operation: Fig. 6 b) and c) show simulation results for I_D and V_{GS} during two consecutive pulses of operation, the first corresponding to nominal current switching on resistive load and the second corresponding to a short-circuit condition; the results of b) refer to the case when no V_{GS} clamp circuit is inserted, the results in c) correspond to

the use of the clamp circuit; it is visible from these results that the clamp is very effective in reducing the short-circuit current, while nominal operation remains unaffected.

Fig. 6: Gate-driver design improvement to achieve V_{GS} positive peak clamping, a). Illustration of nominal (first pulse, resistive load) I_D and V_{GS} waveforms and their change during short-circuit (second pulse, current limited by device characteristics), a): b): $R5$ and $R6$ set the clamp voltage value, whereas $C2$ limits the voltage increase when the clamp is active and $D2$ is conducting; corresponding reduction of short-circuit peak current (from about 105 A to less than 80 A) for enhanced device robustness, c).

a)

b)

c)

d)

Fig. 7: Gate-driver prototype, a) and b); representative switching waveform showing the ability to control turn-on and turn-off peak amplitudes and rapid return to zero during the turn-off phase.

The clamp network can also serve as a fast short-circuit monitor by careful selection of R6 and C2.

III. PROOF-OF-CONCEPT DEMONSTRATION

A prototype of the gate-driver designed as per above description was implemented. Fig. 7 a) shows the top and bottom side of the gate-driver PCB circuit, which was nearly entirely built with surface mount devices. Fig. 7 b) shows a typical experimental transient profile for V_{GS} and it should be noted that the amplitude of the plateau can be easily adjusted by controlling the value of the bias voltage of the push-pulls driver stage, V_{dc} in Fig. 6 a), taking into account the decrease with temperature due to the above mentioned increase in the gate bias current. Figs. 7 c) and d) show V_{GS} and I_D during a short-circuit event, with and without the clamp circuit, respectively.

IV. CONCLUSION

This paper has presented the design and prototype demonstration of a gate driver dedicated to optimize the operational performance of gate-injection high electron mobility GaN transistors in real applications. The design enables independent setting of the parameters required to achieve best switching performance, both on and off, reverse current conduction for free-wheeling of inductive load currents, and withstand of abnormal overload short-circuit events to deliver the typical required robustness of drive applications, as required by a number of strategic application domains, such as automotive.

REFERENCES

- [1] Y. Uemoto et al., *Gate injection transistor (GIT) - a normally-off AlGaIn/GaN power transistor using conductivity modulation*, IEEE Trans. Electron Devices, 54 (12) (2014) 3393–3399.
- [2] E. Gurpinar, A. Castellazzi, *Tradeoff Study of Heat Sink and Output Filter Volume in a GaN HEMT Based Single-Phase Inverter*, IEEE Transactions on Power Electronics (Volume: 33, Issue: 6, June 2018), 5226 – 5239.
- [3] T. Oeder, A. Castellazzi, M. Pfost, Experimental study of the short-circuit performance for a 600V normally-off p-gate GaN HEMT, in Proc. ISPSD 2017, Sapporo, Japan, 28 May-1 June 2017.
- [4] T. Oeder, A. Castellazzi, M. Pfost, Electrical and thermal failure modes of 600 V p-gate GaN HEMTs, Microelectronics Reliability Vol. 76–77, September 2017, 321-326.
- [5] K. Tanaka et al., *Reliability of hybrid-drain-embedded gate injection transistor*, 2017 IEEE International Reliability Physics Symposium (IRPS), 2-6 April 2017, Monterey, CA, USA.
- [6] https://industrial.panasonic.com/content/data/SC/ds/ds8/c2/FLY000075_EN.pdf
- [7] Y. C. Fong, K. W. E. Cheng, *Experimental Study on the Electrical Characteristic of a GaN Hybrid Drain-embedded Gate Injection Transistor (HD-GIT)*, 7th International Conference Power Electronics Systems and Applications - Smart Mobility, Power Transfer & Security (PESA), 2017, 12-14 Dec. 2017, Hong Kong, China.
- [8] A. Castellazzi, T. Oeder, A. Fayyaz, S. Zhu, M. Pfost, *Single pulse short-circuit robustness and repetitive stress aging of GaN GITs*, 2018 IEEE International Reliability Physics Symposium, March 11-15, 2018, Burlingame, California, USA.