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A Comprehensive Analysis and Hardware Implementation of Control Strategies for High Output Voltage DC-DC Boost Power Converter

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Abstract

Classical DC-DC converters used in high voltage direct current (HVDC) power transmission systems, lack in terms of efficiency, reduced transfer gain and increased cost with sensor (voltage/current) numbers. Besides, the internal self-parasitic behavior of the power components reduces the output voltage and efficiency of classical HV converters. This paper deals with extra high-voltage (EHV) dc-dc boost converter by the application of voltage-lift technique to overcome the aforementioned deficiencies. The control strategy is based on classical proportional-integral (P-I) and fuzzy logic closed-loop controller to get high and stable output voltage. Complete hardware prototype of EHV is implemented and experimental tasks are carried out with digital signal processor (DSP) TMS320F2812. The control algorithms P-I, fuzzy logic and the pulse-width modulation (PWM) signals for *N*-channel MOSFET device are performed by the DSP. The experimental results provided show good conformity with developed hypothetical predictions. Additionally, the presented study confirms that the fuzzy logic controller provides better performance than classical P-I controller under different perturbation conditions.

Keywords: DC-DC boost converter, proportional-integral (P-I) controller, fuzzy controller, voltage-lift technology, HVDC power converter.

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1. Introduction

Traditional DC-DC boost converters widely utilized for high voltage direct current (HVDC) power transmission systems, transportation, electric vehicles (EVs) and hybrid electric vehicles (HEVs) applications [1-4]. But, the issues are persisting by the experimental study [3]. The EVs that are supplied by 42V batteries or storage devices require around 300V during start-up. Hence, the transient is increased for the DC-DC converter. Numerous topologies are proposed to meet the HV requirements, but almost all of them suffer deficiencies [1], [4-6]. A transformer-less DC-DC boost resonant converter topology with four switches in full-wave structure was investigated [7]. However, the switching frequency is limited up to 10 kHz in order to decrease the switching losses, but efficiency is limited [7]. Further, the converter topology that operates in cascaded structure of six MOSFETs was proposed to over HV requirements. But, which require a complex control algorithm to yield high voltage output [8]. Alternatively, the transformer based topologies to obtain HV gain with increased number of switches also was developed [9-10]. In this case, the transformer causes bulky structure and increased high-cost of the overall topology. Furthermore, the literature survey on HV DC-DC converters concludes that above topologies are drastically suffered by the reduction in gain and reduced output voltage. Approach by increased switch numbers make the control strategy much more complex that further causes lesser efficiency and increased costs [11-15].

To overcome these stated deficiencies, DC-DC converter with integrated voltage-lift techniques is recommended. The voltage-lift technique provides a staircase increment on output voltage by geometrical progressions [16-18]. Extra HV (EHV) DC-DC boost power converter which is obtained from the modified version of the classical buck. Power circuit is constituted with voltage-lift technique by including some additional passive (inductor/capacitor) components. Owing to its simple control algorithm and higher gain on output voltage [16-18].The performance of the proposed EHV power converter adds the advantages as below [11-12], [18]:

- Increased output voltage-gain (k) ratio
- Simpler in control algorithm with wide range of operation
- Reduced ripple level at the output voltage and current
- Increased power density with efficiency
- Closed-loop controller requires only one sensor (voltage feedback) for investigated controlling aspects P-I and fuzzy logic

The hardware prototype of EHV DC-DC boost converter is implemented with a digital signal processor (DSP) TMS320F2812 platform. The main contribution of this study focused on simple development of the control strategy based on P-I and fuzzy logic controllers for its comparative performances under different line/load regulation conditions. The TMS320F2812 processor performs the closed-loop control algorithm of P-I and fuzzy logic, and PWM generation for *N*-channel MOSFET. The experimental results presented closely match with the analytical predictions.

This research manuscript is articulated here in below. Section 2 describes the circuit configuration of EHV boost power converter. Analytical developments during operational mode are elaborated in section 3. The characteristic of the converter configuration along with power loss calculation are given by section 4. Further, theoretical background and practical implementation are discussed in same section 4. Proposed control scheme based on P-I and Fuzzy Logic algorithm are illustrated in detail by section 5. Hardware prototype implementation using DSP processor and complete set of experimental results are presented in the section 6. Real time results are presented with different perturbation conditions along with theoretical background in the same section. Finally, the conclusions of this article are given by section 7.

2. EHV Boost Power Circuit Configuration

Fig. 1(a) shows the extra high voltage (EHV) DC-DC boost converter circuit. The load voltage (V_O), load current (i_O), the supply voltage (V_I), supply current of the power circuit (i_I) are depicted in the same Fig. 1(a). It consists of an *N*-channel MOSFET as static switch *S*, and diodes ($D, D_1, \ldots, D_{13}$). The voltage-lift circuit is obtained by inclusion of additional capacitors ($C, C_0, C_1, \ldots, C_4$) and inductors ($L, L_0, \ldots, L_3$) to the existing circuit. The voltage-lift gain is actually obtained by the capacitors (C_2, C_3, C_4), where the capacitor voltage V_C is built-up by four

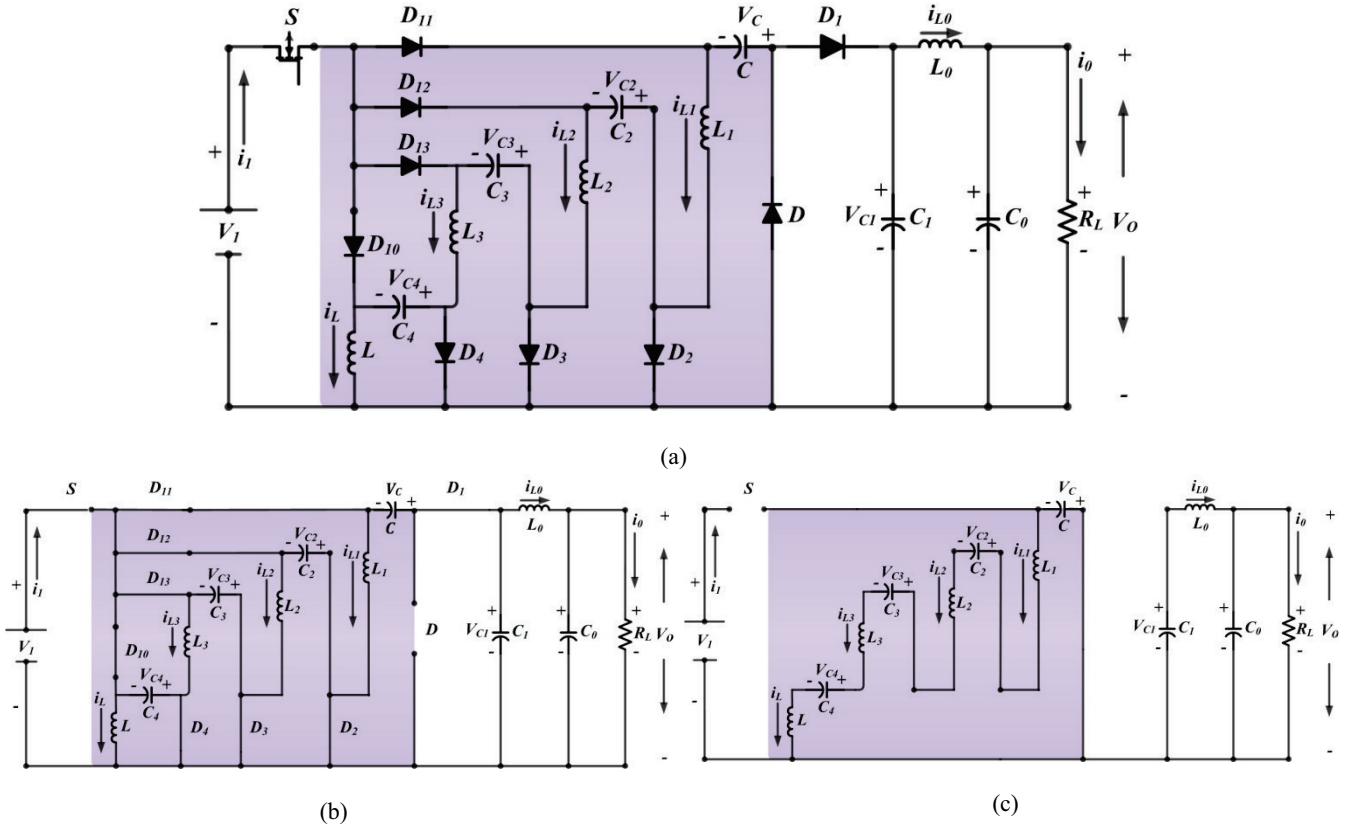

Fig. 1. (a) Topology of extra high voltage (EHV) dc-dc boost power converter circuit; (b) Equivalent power converter circuit when switch turned ON; (c) Equivalent power converter circuit when switch turned OFF.

times (transfer gain ratio) of the battery input voltage V_1 (V_{CO}=V_{C1}). In continuous conduction mode, it is assumed that all components are ideal, capacitors are large enough.

3. Analytical Prediction of Operating Modes

The first interval when the switch S is turned ON, corresponding equivalent circuit is shown in Fig. 1(b) with voltages and currents direction. The instantaneous input current (i_1-source current) gets equal to sum of all capacitor and inductor currents, except i_{CO} and i_{C1}. The load current (i_O-load) flows depending to the sum of the battery supply voltage V_1 and the capacitor voltage V_C.

Now, the capacitors C_2, C_3, and C_4 are charged by the input voltage and all inductor currents which lead to first prediction of investigation are increased at this interval.

The corresponding equivalent circuit when switch S is turned OFF is shown in Fig. 1(c) along with voltages and currents direction. The instantaneous input current (i_1-source current) equals to zero at this interval. The voltage-lift part that is located on the left-hand side of capacitor C (L_1, L_2, L_3 and L), and inductor store the energy, while C_2, C_3 and C_4 capacitor discharge the stored energy. Corresponding directions that are leading to charge the capacitor C are shown in the Fig. 1(c). The current i_{L0} flows through the load over the inductor and decreases the current with all the inductors which leads to second prediction of investigation. In steady–state, the average inductor voltage is zero, leading to:

$$V_{CO} = V_O \tag{1}$$

The circuit voltages will be the same when switch S is turned ON:

$$V_{C2} = V_{C3} = V_{C4} = V_1 \tag{2}$$

that also yields:

$$V_O = V_{C1} = V_C + V_1 \tag{3}$$

It should be noted that the inductor current I_L is increased when the switch S is turned ON and is decreased during switch *S is* turned OFF. The voltage components V_1 as well $-V_{L\text{-}OFF}$, which predicts that the voltages across the inductor *L* are expressed as follows:

$$kTV_1 = (1\text{-}k)\ TV_{L\text{-}OFF} \quad (4)$$

$$V_{L\text{-}OFF} = [k/(1\text{-}k)]\ V_1 \quad (5)$$

The voltages across inductors (L_1, L_2, L_3) are determined as the following:

$$V_{L1\text{-}OFF} = [k/(1\text{-}k)]\ V_1 \quad (6)$$

$$V_{L2\text{-}OFF} = [k/(1\text{-}k)]\ V_1 \quad (7)$$

$$V_{L3\text{-}OFF} = [k/(1\text{-}k)]\ V_1 \quad (8)$$

Fig. 1(c) provides the analytical prediction of the capacitor voltage V_C and output voltage V_O as:

$$V_C = V_{C\text{-}OFF} = V_{L\text{-}OFF} + V_{L1\text{-}OFF} + V_{L2\text{-}OFF} + V_{L3\text{-}OFF} + V_{C2} + V_{C3} + V_{C4} \quad (9)$$

$$V_C = 4k/(1\text{-}k)\ V_1 + 3V_1 \quad (10)$$

Again from Eq. 3,

$$V_O = V_C + V_1 \quad (11)$$

$$V_O = [4/(1\text{-}k)]\ V_1 \quad (12)$$

then, gain transfer ratio of output current and voltage are given by:

Table 1. Comparative performances emphasis the proposed with classical dc-dc boost power converter.

Converter Type	Output Voltage (V_0) (Volts)	Output Current (i_0) (Amps)
Classical Converter	$V_0 = [k/(1\text{-}k)]\ V_1$	$i_0 = [(1\text{-}k)/k]\ i_1$
Proposed Converter	$V_0 = [4/(1\text{-}k)]\ V_1$	$i_0 = [(1\text{-}k)/4]\ i_1$

Table 2. Simulation parameters taken for investigation.

Parameter		Value
Input Voltage	(V_1)	10 V
Inductance	(L)	100µH
Capacitance	(C)	5µF
Load Resistance	(R)	44 ohms
Duty Ratio	(k)	2/3
Switching	(F_{SW})	50 KHz
Digital Processor	DSP	TMS 320F2812
N-channel MOSFET	(IRFPC60)	V_{DSS}= 600V, $R_{DS(ON)}$= 0.40Ω, I_D=16A

$$i_O = [(1\text{-}k)/4]\ i_1, \quad (13)$$

$$M_O = 4/(1\text{-}k). \quad (14)$$

Finally, the average voltages and currents are predicted and summarized as:

Table 3. Investigated output performance indices of hardware prototype testing.

Duty Ratio (k)	Output Voltage (V_O) volt	Output Current (i_0) amp	Output Power (P_O) watt	Input Voltage (V_1) volt	Input Current (i_1) amp	Input Power (P_1) watt	% Efficiency (η)	% Ripple
0.1	44.24444	1.004901	44.46129	10	4.466227	44.66227	99.55	0.486
0.2	49.8	1.131164	56.33195	10	5.655818	56.55818	99.6	0.478
0.3	56.94286	1.293501	73.65566	10	7.391436	73.91436	99.65	0.472
0.4	66.46667	1.509952	100.3614	10	10.06634	100.6634	99.7	0.466
0.5	79.8	1.812982	144.6759	10	14.50385	145.0385	99.75	0.441
0.6	99.8	2.267527	226.2992	10	22.67527	226.7527	99.8	0.432
2/3	**119.8**	**2.722**	**326.094**	**10**	**32.664**	**326.64**	**99.83**	**0.431**
0.7	133.1333	3.025103	402.7421	10	40.33471	403.3471	99.85	0.431
0.8	199.8	4.540255	907.1429	10	90.80509	908.0509	99.9	0.431
0.9	399.8	9.085709	3632.466	10	363.4284	3634.284	99.95	0.431

$$V_C = [(3+k)/(1-k)]\ V_1 \quad (15)$$

$$V_{C1} = V_O, \quad (16)$$

$$V_{C2} = V_{C3} = V_{C4} = V_1 \quad (17)$$

$$i_{LO} = i_O \quad (18)$$

$$i_L = [k/(1-k)]\ i_O \quad (19)$$

$$i_{L1} = i_{L2} = i_{L3} = i_L + i_{LO} = [1/(1-k)]i_O \quad (20)$$

4. Characteristics and Power Loss Analysis

Table 1 summarizes the comparison between the EHV DC-DC boost converter and classical converter with respect to voltage-lift transfer

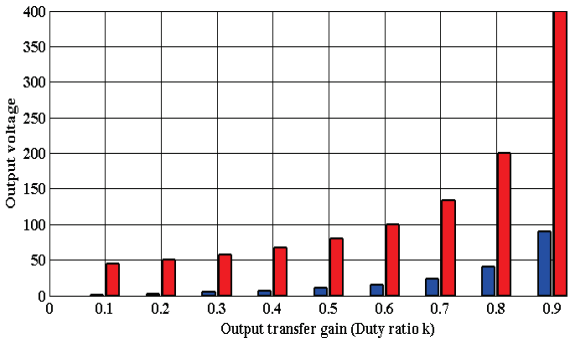

Fig. 2. Comparative performances emphasis the variation of duty ratio k versus output voltage V_O for the proposed power conversion (red bar) with classical power conversion (blue bar) unit (steady-state rated condition).

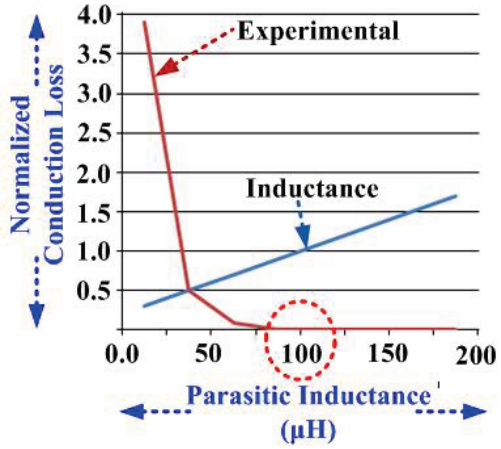

Fig. 3. Plot showing conduction loss versus inductance variation.

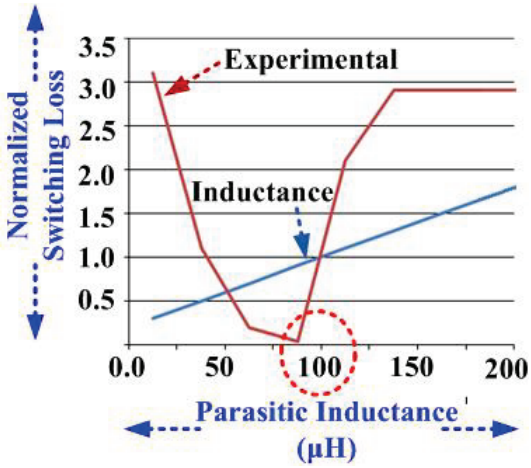

Fig. 4. Plot showing switching loss versus inductance variation.

Accordingly, Fig. 2 proves the effectiveness of proposed power conversion. As seen, the proposed DC-DC converter (red bar) output voltage varies from 44.44V to 400V, while for classical one (blue bar) varies from 1.11V to 90V when subjected to output transfer gain (duty ratio) k = 0.1 to 0.9 variation.

A complete set of performance outputs obtained from open-loop experimental tests by considering the parameters taken from Table 2 are summarized in Table 3. All operating conditions (duty cycle variation k= 0.1~0.9) the converter performed with efficiency of 99% in experimental test with reduced ripple content of 0.43% at the outputs is observed. Thus, the test parameters output voltage (V_O), output current (i_O) and efficiency (η) from the Table 2 confirms that obtained results are very closely matched with the theoretical background. To be noted, that the converter produced high efficiency due to the inclusion of additional passive (L, C) components actually reduced several parasitic effects (L, R, C, and MOSFET switching, conduction etc.) [21], which is proved by Eq. 12. Further literatures, the inductance parasitic effects are neglected in DC-DC converters investigations. To attain high efficiency the RC time constant of converter is always compared to the switching frequency. Hence by considering the small parasitic inductance, the results could differ and the current is expressed as [19]:

$$i(t) = \frac{V_O}{R} e^{-\frac{t}{RC}} + i_O \quad (21)$$

where, V_O is the initial voltage difference between the source voltage and the voltage across the capacitor. The input current is given by:

$$i(t) = i_O e^{-\frac{R}{2L}t} \cos\left(\sqrt{\frac{1}{LC} + \left(\frac{R}{2L}\right)^2}\, t\right) + i_O + \frac{V_O - \frac{Ri_O}{2}}{\sqrt{\frac{L}{C} - \left(\frac{R}{2}\right)^2}} e^{-\frac{R}{2L}t} \sin\left(\sqrt{\frac{1}{LC} + \left(\frac{R}{2L}\right)^2}\, t\right) \quad (22)$$

or expressed as,

$$i(t) = i_O + f(i_{int}, V_O) e^{-\frac{R}{2L}t} \text{ x } \sin\left(\sqrt{\frac{1}{LC} + \left(\frac{R}{2L}\right)^2}\, t + \varphi(i_{int}, V_O)\right) \quad (23)$$

Where i_O, i_{int}, and V_O, are the load current, initial current, and initial voltage difference between the source voltage and capacitor, respectively. The conduction loss of the circuit is directly proportional to the square of the rms value. Hence the conduction loss of the MOSFET is calculated as:

$$P_{COND.} = I_{ON}^2 R_{DS,ON} \quad (24)$$

Where, I_{ON} is the drain current, $R_{DS,ON}$ is the drain-source resistance of the MOSFET, in ON state. Therefore, by multiplying Eq. 24 by the duty ratio (k) leads to average value of the conduction loss. The switching losses of the MOSFET are calculated by the non-zero product of drain current (I_D) and drain to source voltage (V_{DSS}). If the MOSFET is assumed as ideal switch, the rise and fall time of the current and voltage, switching loss is zero. Then, the switching losses are determined by:

$$P_{SW} = \frac{T_{SW,ON} V_{OFF} I_{ON} F_{SW}}{2} + \frac{T_{SW,OFF} V_{OFF} I_{ON} F_{SW}}{2} \quad (25)$$

Where, V_{OFF} is the drain source voltage, $T_{SW,ON}$, $T_{SW,OFF}$ is the time to turn ON and turn OFF state, and F_{SW} is the switching frequency of the MOSFET. From Table 2 and considering Eq. 24 and Eq.25, with duty ratio $k=2/3$ (i.e.$T_{SW,ON} = 2/3 * 1/50KHz, T_{SW,OFF} = 1/3 * 1/50KHz$) used for calculating the losses.

Fig. 3 and Fig. 4 illustrate the variation of conduction loss and switching loss, respectively, when parasitic L changes. It could be observed that the conduction losses are reduced dramatically at 100µH and correspondingly the switching loss is minimal at resonant point 100µH with inductance profile variation. Therefore this concludes that the increasing parasitic effects of power converters can be overcome by inclusion of additional passive components (L and C i.e. voltage lift technique) within the power circuit without any additional external compensation network/circuitry [11-17], [19].

Finally, the performances obtained such as the higher output voltage and higher efficiency, reduced % ripple, which verifies that the proposed DC-DC converter (hardware prototype) has a better power density factor as per the standard [20-22]. This which in turn proves the exact viability for parasitic compensation and suits the high voltage industrial needs.

5. Control Strategies based on P-I and Fuzzy Logic

A standard closed-loop P-I controller scheme for the proposed EHV DC-DC boost converter is shown in Fig. 5. It notably consists of one stage voltage sensor feedback

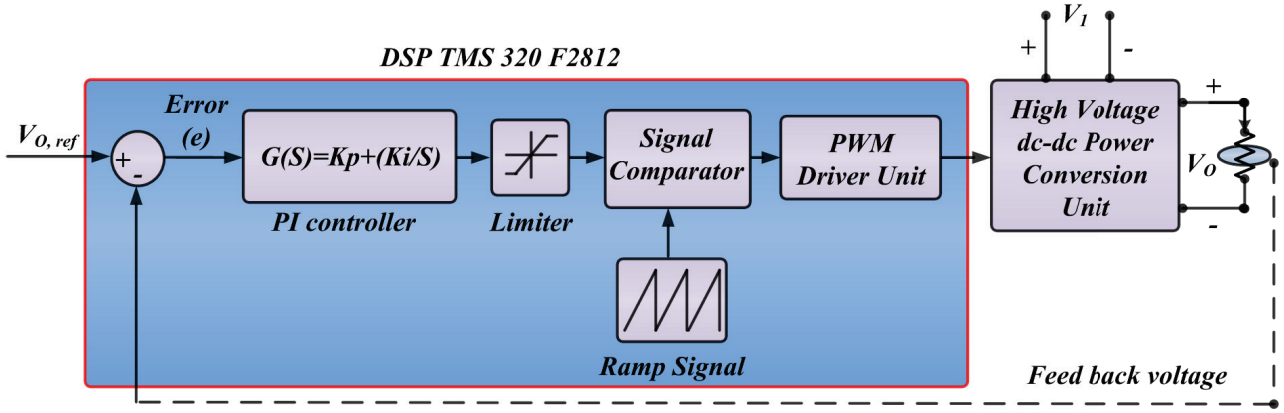

Fig. 5. Simplified closed loop control strategy under line/load regulation using proportional-integral (P-I) control scheme.

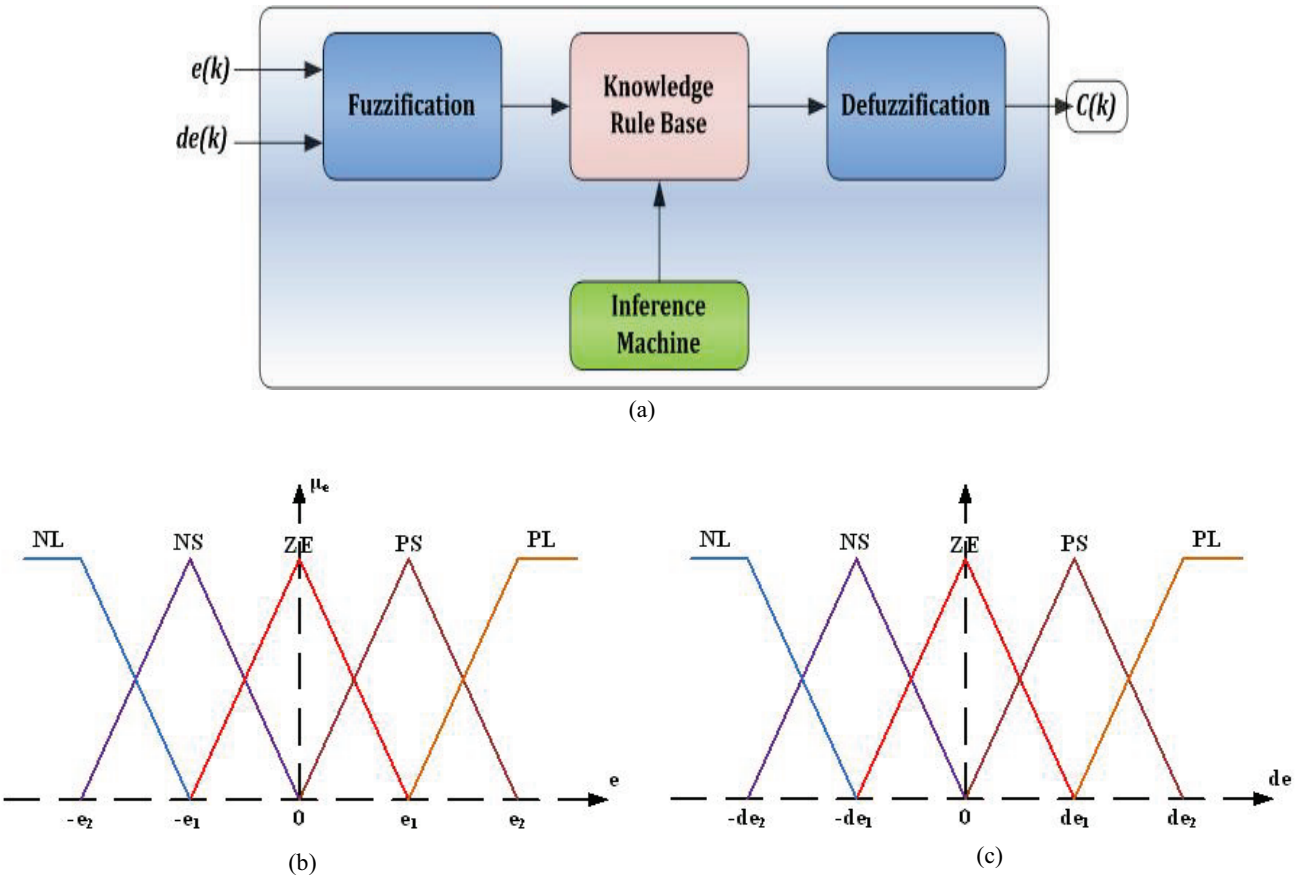

Fig. 6. (a) Fuzzy logic rule based system generalized structure. Membership function of the fuzzy logic controller, (b) membership function of error (e), (c) membership function of change-in-error (de).

obtained from the dc load voltage. It is then compared with the set reference voltage $V_{O,ref}$ to obtain the error between reference DC bus voltage and feedback signal. Further, the error signal is applied to the P-I controller to compensate the available error. The manipulated signal thus obtained from the P-I controller defines the set duty ratio k and is compared with high frequency ramp-signal to generate the controlled pulse-width modulated (PWM) signal to the static switch *S*. The parameters (P-proportional gain, I-integral gain) are fine-tuned to get the set reference dc voltage under different perturbation conditions [11-12], [23-29].

The block diagram of generalized rule based fuzzy logic controller (FLC) is shown in Fig. 6(a), where *e(k)* and *de(k)* denote the input error and the rate of change in the input variables, respectively. The FLC block is composed of fuzzification interface, fuzzy rules, and inference and de-fuzzification mechanism. The FLC has two inputs which are error signal, *e(k)*, and change in error signal, *de(k)*. The output, *c(k)*, on the other hand represents the control component to generate the switching signal for n-channel MOSFET switch.

In the first stage, the crisp variables, *e(k)* and *de(k)*, are converted into fuzzy variables such as *E(k)* and *dE(k)* using the triangular membership functions given by Fig.

Table 4. Matrix formulation (5x5) for fuzzy logic rules.

e(k) / *de(k)*	NL	NS	ZE	PS	PL
NL	NL	NL	NL	NS	ZE
NS	NL	NL	NS	ZE	PS
ZE	NL	NS	ZE	PS	PL
PS	NS	ZE	PS	PL	PL
PL	ZE	PS	PL	PL	PL

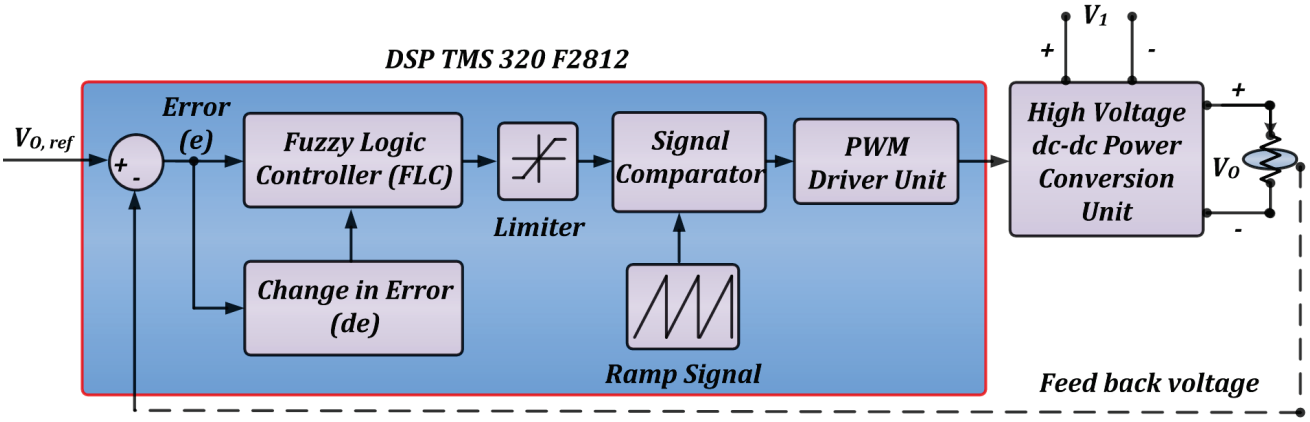

Fig. 7. Simplified closed loop control strategy under line/load regulation using fuzzy logic control scheme.

6(b) and Fig. 6(c). Then, each universe of discourse is divided into five fuzzy sets: Namely, NL (negative large), NS (negative small), ZE (zero), PS (positive small) and PL (positive large). Each fuzzy variable is a member of the subsets with a degree of membership varying between 0 (non-member) and 1 (full-member) [30-32]. In the second stage of the FLC, the fuzzy variables, *E(k)* and *dE(k)*, are processed by an inference engine that executes a set of control rules contained in a 5×5 rule bases as given by Table 4. These rules are designed based on the dynamic behavior of the error signal resulting in the symmetrical matrix. This is a general rule-based design with a 2-D phase plane. Each rule is expressed via the following form

Rule: If x is A and y is B then z is C.

Different inference algorithms can be used to space the fuzzy set values for the output fuzzy variable, *c(k)*. In this work, the max-min inference algorithm is used, in which the membership degree is equal to the maximum of the product of *E* and *dE* membership degree. The output variable from the inference engine is converted into a crisp value in the de-fuzzification stage. Various de-fuzzification algorithms have been proposed in the literature. In this work, the centroid de-fuzzification algorithm is used, in which the crisp value is calculated as the centre of gravity of the membership function. The definition of the spread of each partition, or conversely the width and symmetry of the membership functions, is generally a compromise between dynamic and steady state accuracy. Equally, spaced partitions and consequently symmetrical triangles are reasonable choices [30-32]. Complete control scheme based on fuzzy logic controller algorithm for the EHV DC-DC boost converter is illustrated by Fig. 7.

6. Hardware Implementation and Experimental Results

Hardware prototype model of EHV DC-DC boost power converter is implemented as shown by Fig. 8 and based on parameter given by Table 2 with a digital signal processor (DSP) TMS320F2812 [26-28]. The control strategies based on P-I and fuzzy logic controller algorithm are framed in DSP that also generates the controlled PWM signal for *N*-channel MOSFET. The inductance and

Fig. 8. Hardware prototype module of EHV dc-dc boost power converter with DSP TMS320F2812 processor.

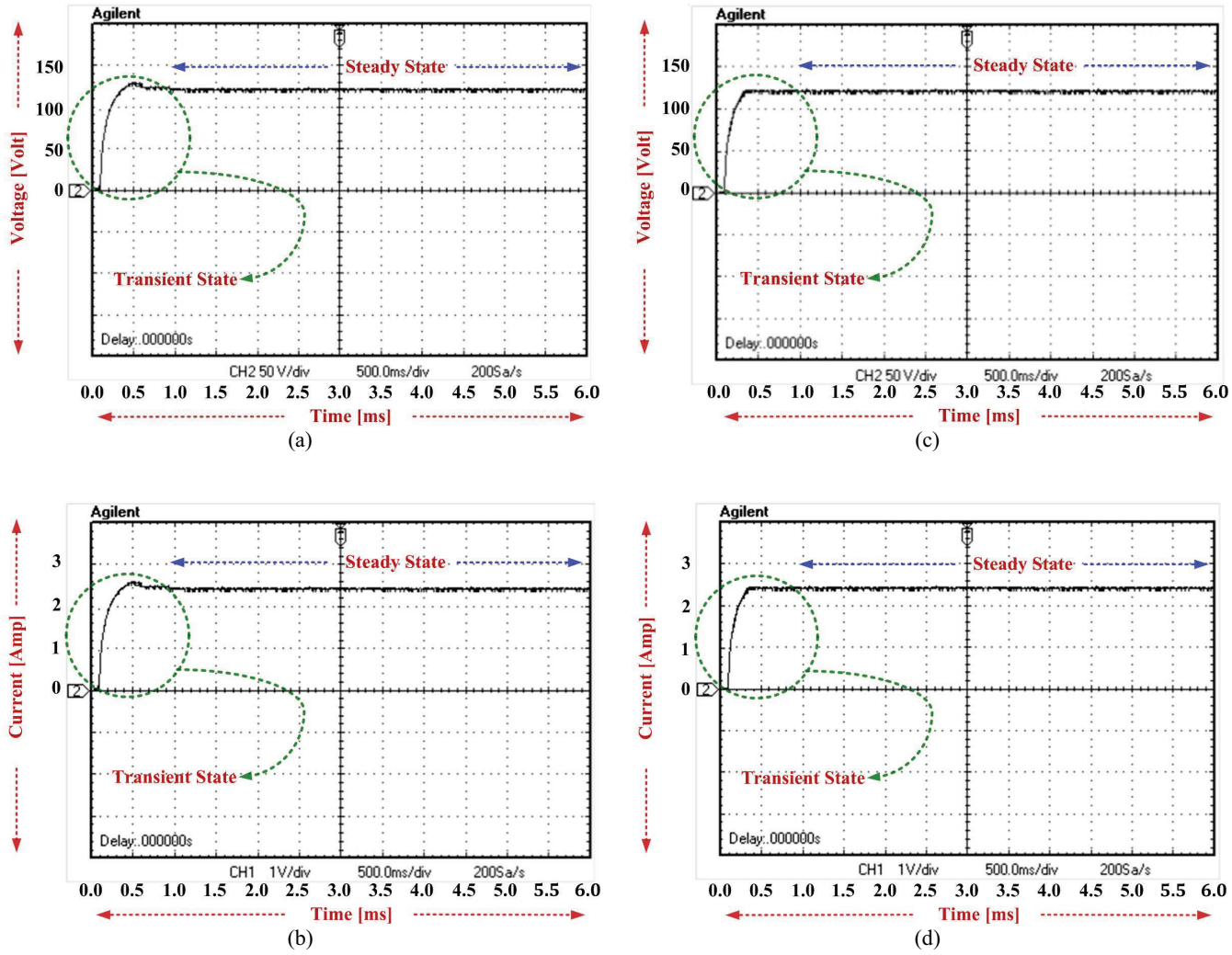

Fig. 9. P-I and fuzzy controlled output performances of EHV power converter in transient and steady-state conditions. P-I: (a) output voltage, (b) output current. Fuzzy: (c) output voltage, (d) output current. [50v/div, 2A/div].

capacitance values of the power circuit are determined according to the criteria of 5% output ripple requirement as per IEEE standards [11-12], [27-29].

Fig. 9(a) and Fig. 9(b) shows the P-I controller based experimental results of output voltage and current at the rated conditions (set reference output voltage 120V, load resistance 44Ω and duty ratio k = 2/3). It is observed that the output voltage is slightly lower than the set reference and settles at 119.8V with 1.0833% peak overshoot, with 200mv steady state and 1 sec settling time, closely matches the prediction given by Eq. 12 at k = 2/3. Correspondingly, the output current is observed as 2.722A with 1.0833% peak overshoot and 1 sec settling time that closely matches the prediction given by Eq. 13.

Fig. 9(c) and Fig. 9(d) show the fuzzy logic controller based experimental results of output voltage and current at the rated conditions. It is observed that the output voltage is slightly lower than the set reference that settles at

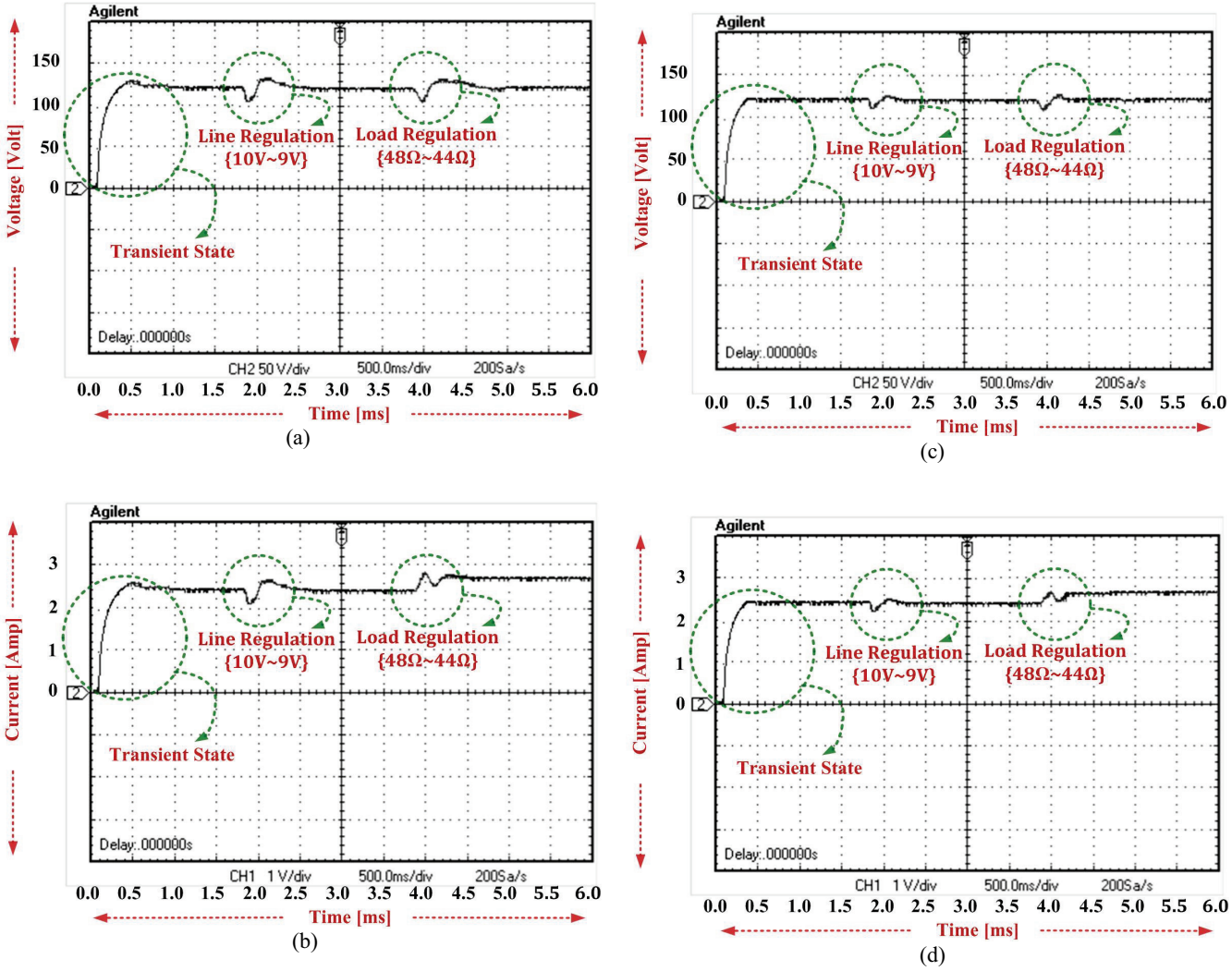

Fig. 10. P-I and fuzzy controlled output performances of EHV power converter in transient, line/load regulation & steady-state conditions. P-I: (a) output voltage, (b) output current. Fuzzy: (c) output voltage, (d) output current. [50v/div, 2A/div].

119.925V with 1.016% peak overshoot and 0.4 sec settling time, which closely meets the prediction given by Eq. 12 at k = 2/3. Correspondingly, the output current 2.7255A observed with 1.016% peak overshoot and 0.4 sec settling time, closely matches the prediction given by Eq. 13.

Fig. 10(a) and Fig. 10(b) show the P-I controller based experimental results of output voltage and current obtained under line and load perturbation condition. It is noticed that the output voltage and current are stabilized at 1 sec with a peak overshoot 1.125% when the battery voltage represents a step variation from 10V to 9V. Even though the load resistance varies from 48Ω to 44Ω, the output voltage retains the same value of 119.8V and current value of 2.722A which was observed with 1.125% peak overshoot and 1.2 sec settling time. The output voltage and current results closely match the prediction given by Eq. 12 and Eq. 13.

Fig. 10(c) and Fig. 10(d) show the fuzzy logic controller based experimental results of output voltage and current obtained under line and load perturbation condition. It is noticed that the output voltage and current are stabilized at 0.28 sec with a peak overshoot 1.0416% when the battery voltage represents a step variation from 10V to 9V. Even though the load resistance varies from 48Ω to 44Ω, the output voltage retains the same value of 119.925V and current value of 2.7255A which was observed with 1.0666% peak overshoot and 0.25 sec settling time. The output voltage and current results closely match the prediction given by Eq. 12 and Eq. 13.

The experimental test results and information provided by Table 5 confirms that the control strategy based on fuzzy logic controller provides minimal peak overshoot with faster settling time and steady error accuracy in comparison to classical P-I controller. It is practically appreciable that the verified generated outputs of hardware prototype have losses in the range of milli-amplitude.

Finally, the higher output voltage and higher efficiency, reduced % ripple (Table 3) and faster settling time (Table 5), verify that the proposed dc-dc converter (hardware prototype) has better power density factor as per standard [20-23, 27-29]. Also notable that the output settles less than 1 sec in all investigation, yet still DSP has its own sampling rate to interface with external hardware modules

Table 5. Performance comparison between P-I and fuzzy logic controller.

Performance Parameters	P-I	Fuzzy Logic
Peak over-shoot (M_p)	1.0833%	1.016%
Settling time (t_s)	1 sec	0.4 sec
Steady state error (ess)	200mv	75mv
Over shoot in line variations	1.125%	1.0416%
Under shoot in line variations	1.15%	1.0833%
Over shoot in load variations	1.125%	1.0666%
Under shoot in load variations	1.15%	1.0833%
Settling time in line variations	1 sec	0.28 sec
Settling time in line variations	1.2 sec	0.25 sec

in real time. This in turn proves the exact viability for parasitic compensation and suit the high voltage needs of HVDC transmission systems and high voltage industrial applications.

7. Conclusions

The comparative performance study of control strategies based on P-I and fuzzy logic closed-loop with single (voltage feed-back) sensor algorithm for EHV DC-DC boost power converter is presented in this paper. The extra high-voltage DC-DC power boost converter circuit has been integrated with voltage-lift technique to generate higher output voltage and significantly overcomes the deficiencies of parasitic effects with reduced ripples at the output waveforms (voltage/current).

Experimental results prove that the fuzzy logic controller provided good performances during transient, steady-state and line/load perturbation conditions in comparison to standard P-I controller. The investigated EHV DC-DC boost converter along with fuzzy logic based control strategy is suitable for HVDC transmission system where high-voltage becomes mandatory with reduced ripple at the output.

References

1. Xuan Zhang, Chengcheng Yao, Cong Li, Lixing Fu, Feng Guo, and Jin Wang, A Wide Bandgap Device-Based Isolated Quasi-Switched-Capacitor DC/DC Converter, *Trans. IEEE Power Electron.* 29(5) (2014) 2500-2510.
2. Ching-Tsai Pan, Chen-Feng Chuang, and Chia-Chi Chu, "A Novel Transformerless Interleaved High Step-Down Conversion Ratio DC–DC Converter With Low Switch Voltage Stress", *IEEE Trans. Ind. Electron.* 61(10) (2014). 5290-5299.
3. C.M.Young, M.H.Chen, and C.C.Ko, High power factor transformerless single-stage single-phase ac to high-voltage dc converter with voltage multiplier, *IET Power Electron. J.* 5(2) (2012) 49-157.
4. M. Narimani, and G. Moschopoulos, An Investigation on the Novel Use of High-Power Three-Level Converter Topologies to Improve Light-Load Efficiency in Low Power DC/DC Full-Bridge Converters, *IEEE Trans. Ind. Electron.* 61(10) (2014) 5690-5692.
5. P.N.Marinus van Wesenbeeck, J. B. Klaassens, Ulrich von Stockhausen, Ana Munoz de Morales Anciola, and Stanimir Stoyanov Valtchev, A Multiple-Switch High-Voltage DC–DC Converter, *IEEE Trans. Ind. Electron.* 44(6) (1997) 780-786.
6. A. Amir, S. Taib, and S. Iqbal, Voltage multiplier-based continuous conduction LCCL series resonant inverter fed

high voltage DC-DC converter, *Intl. Symposium Proc. on Ind. Electron. Appl., ISIEA'13*. (2013) 105-110.
7. T.Soong, and P.Lehn, A transformerless high boost DC-DC converter for use in medium / high voltage applications, *The 38th Annual Conf. on IEEE Ind. Electron. Society, IECON'12*. (2012) 174-179.
8. Wu, Peng Xu, Haibing Hu, Zihu Zhou, and Yan Xing, Multiport Converters Based on Integration of Full-Bridge and Bidirectional DC–DC Topologies for Renewable Generation Systems, *IEEE Trans. Ind. Electron.* 61(2) (2014) 856-869.
9. Chung-Ming Young, and Ming-Hui Chen, A novel single-phase ac to high voltage dc converter based on Cockcroft-Walton cascade rectifier, *Intl. Conf. Power Electron. & Drive Systems, PEDS'09*. (2009) 822-826.
10. Ting-Ting Song, Huai Wang, H.S.Chung, S.Tapuhi, and A.Ioinovici, A High-Voltage ZVZCS DC--DC Converter With Low Voltage Stress, *IEEE Trans. Power Electron.* 23(6) (2008) 2630-2647.
11. Y. Tsuruta, Y. Ito, and A. Kawamura, Snubber-Assisted Zero-Voltage and Zero-Current Transition Bilateral Buck and Boost Chopper for EV Drive Application and Test Evaluation at 25 kW, *IEEE Trans. Ind. Electron.* 56(1) (2009) 4-11.
12. T.Soong, and P.Lehn, A transformerless high boost DC-DC converter for use in medium / high voltage applications, *The 38th Annual Conf. on IEEE Ind. Electron. Society, IECON'12*. (2012) 174-179.
13. A.Shahin, M.Hinaje, J.P.Martin, S.Pierfederici, S.Rae, and B.Davat, High Voltage Ratio DC–DC Converter for Fuel-Cell Applications, *IEEE Trans. Ind. Electron.* 57(12) (2010) 3944-3955.
14. Yi-Ping Hsieh, Jiann-Fuh Chen, Lung-Sheng Yang, Chang-Ying Wu, and Wei-Shih Liu, High-Conversion-Ratio Bidirectional DC–DC Converter With Coupled Inductor, *IEEE Trans. Ind. Electron.* 61(1) (2014) 210-222.
15. Biao Zhao, Qiang Song, Wenhua Liu, and Yandong Sun, A Synthetic Discrete Design Methodology of High-Frequency Isolated Bidirectional DC/DC Converter for Grid-Connected Battery Energy Storage System Using Advanced Components, *IEEE Trans. Ind. Electron.* 61(10) (2014) 5402-5410.
16. Q. Zhang, R. Min, Q. Tong, X. Zou, Z. Liu, and A. Shen, Sensorless Predictive Current Controlled DC–DC Converter With a Self-Correction Differential Current Observer, *IEEE Trans. Ind. Electron.* 61(12) (2014) 6747-6757.
17. F.L.Luo, and Y.Hong, Positive Output Super-Lift Converters, *IEEE Trans. Power Electron.* 18(1) (2003) 105-113.
18. G.C. Silveira, F.L. Tofoli, L.D.S. Bezerra, and R.P. Torrico-Bascope, A Nonisolated DC–DC Boost Converter With High Voltage Gain and Balanced Output Voltage, *IEEE Trans. Ind. Electron.* 61(12) (2014) 6739-6746.
19. Rong-Jong Wai, Chung-You Lin, Rou-Yong Duan, Yand ung-Ruei Chang, High-Efficiency DC-DC Converter With High Voltage Gain and Reduced Switch Stress, *IEEE Trans. Ind. Electron.* 54(1) (2007) 354-364.
20. Miaosen Shen, Fang Zheng Peng, and Leon M.Tolbert. Multilevel DC-DC power conversion system with multiple DC sources, *IEEE Trans. Power Electron.* 23(1) (2008) 420-426.
21. Johann Kolar, Uwe Drofenik, Juergen Biel, Marcelo Heldwein, Hans Ertl, Thomas Friedli, and Simon Round. PWM converter power density barriers, *IEEE Trans. Ind. Appl.* 128(4) (2008) 1-14.
22. Jeff Ham, "Thermal Considerations: Assuring Performance of Vicor's Maxi, Mini, Micro Series High-Density DC-DC Converter Modules, *The Power Bench*, *Published by Vicor Corporation*, Andover, MA 01810, 1-3.
23. Katsuhiko Ogata, Modern Control Engineering, Second Edition Prentice-Hall,India, (1996).
24. A.Matthew Porter, An investigation of DC-DC Converter Power Density Using Si and SiC MOSFETS, *U.S.N.A., Trident Scholar Project Report*. (391) 2010.
25. P.Sanjeevikumar, A.Iqbal, Haitham Abu-Rub, and M.Bishal, Implementation and control of extra high voltage dc-dc boost converter, *The 7th IET Intl. Conf. on Sustainable Energy and Intelligent System, IET-SEISCON'14*, Chennai (India). (2013).
26. P.Sanjeevikumar, and K.Rajambal, Extra high voltage DC-DC boost converters with simplified control strategy, *Intl. J. of Modeling and Simulation, Hindawi Publishing Corporation, US,* (2008).
27. P.Sanjeevikumar, Ersan Kabalci, Atif Iqbal, Haitham Abu-Rub, and Olorunfemi Ojo, Control Strategy and Hardware Implementation for DC-DC Boost Power Conversion Based on Proportional-Integral Compensator for High Voltage Application, *Engg. Science and Technology: An Intl. J. (JESTECH), Elsevier Publications.* 18(2) (2015) 163–170.
28. P. Sanjeevikumar, G.Grandi, Patrick W.Wheeler, Frede Blaabjerg, and J.Loncarski, A Simple MPPT Algorithm for Novel PV Power Generation system by High Output Voltage DC-DC Boost Converter, *Conf. Proc., 24th IEEE Intl. Symposium on Ind. Electron., IEEE-ISIE'15, Rio de Janeiro (Brazil)*. (2015) 214–220.
29. P.Sanjeevikumar, Frede Blaabjerg, Pierluigi Siano, Luigi Martirano, Zbigniew Leonowicz, and Kiran M. Pandav, PI and Fuzzy Control Strategies for High Voltage Output DC-DC Boost Power Converter – Hardware Implementation And Analysis, *Conf. Proc. of 16 IEEE Intl. Conf. on Environment and Electrical Engg.,* Florence (Italy). (2016).
30. M.Nasir Uddin, T.S.Radwan, and A.M.Rahman, Performances of Fuzzy-Logic-Based Indirect Vector

Control for Induction Motor Drive, *IEEE Trans. Ind. Appl.* 38(50) (2002) 1219-1225.

31. P.Sanjeevikumar, J.L.Febin Daya, Frede Blaabjerg, Nazim Mir-Nasiri, and Ahmet H.Ertas, Numerical Implementation of Wavelet and Fuzzy Transform IFOC for Three-Phase Induction Motor, *Engg. Science and Technology: An Intl. J (JESTECH), Elsevier Publications,* 19(1) (2016) 96-100.
32. P.Sanjeevikumar, J.L.Febin Daya, Frede Blaabjerg, Patrick Wheeler, Pawel Szcześniak, Valentin Oleschuk, and Ahmet H.Ertas, Wavelet-Fuzzy Speed Indirect Field Oriented Controller for Three-Phase AC Motor Drive-Investigation and Implementation, *Engg. Science and Technology: An Intl. J (JESTECH), Elsevier Publications,* (2015). Doi: 10.1016/j.jestch.2015.11.007.