Experimental Comparison of Devices Thermal Cycling in Direct Matrix Converters (DMC) and Indirect Matrix Converters (IMC) using SiC MOSFETs

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Abstract— This paper presents an experimental comparison between a Direct Matrix Converter and an Indirect Matrix Converter in terms of semiconductor devices thermal cycling. Both converters have been designed and built using SiC MOSFETs; the Indirect Matrix Converter has also been tested using a hybrid solution with Silicon IGBT on the input stage and SiC MOSFETs on the output stage.

I. INTRODUCTION

A Direct Matrix Converter (DMC), shown in figure 1(a), normally known as "Matrix Converter", is a bidirectional power converter topology which allows direct AC/AC conversion in a single stage using nine bidirectional switches in the case of a 3-phase to 3-phase converter [1][2]. The Indirect Matrix Converter (IMC), shown in figure 1(b), is also a direct AC/AC power converter topology, but the conversion is achieved in two stages [3][4]. DMC and IMC can have identical behavior with respect to input and output waveforms if identical choices are made regarding the modulation techniques; however the efficiency profile of the converters is different and changes with load conditions [5]. Matrix Converters (MCs) have no intermediate stage and no large energy storage elements, so these topologies offer the prospect of a very high power density if the chosen switching frequency is high enough to ensure a low volume input filter [6]. MCs and derived topologies are beginning to find applications in areas where weight and volume of the converter are critical, for example aerospace and integrated motor drives [2]. The use of SiC switching devices in a DMC or IMC enables the converter to operate with a higher switching frequency as well as presenting lower switching losses. Hence the use of SiC devices can lead to a reduction in the input filter weight and volume for a given input power quality as well as improvements in converter efficiency, which in turn leads to reduced heat sink size and weight. Some scientific papers, which consider the design and construction of DMCs [7]-[9] and IMCs [10]–[12], in particular utilizing SiC JFETs and SiC MOSFETs [11], have recently appeared in scientific literature. Moreover in [5] authors report an experimental comparison of the two Matrix Converter topologies using traditional Si IGBTs and diodes based on the converters efficiency.

The main scope of this paper is instead to experimentally evaluate and compare the low frequency thermal cycles (or losses distribution among the single devices) of the DMC and the IMC when using SiC MOSFETs.

In the past few years some publications [13]-[19] have reported the use of simulation results or simple variables measurements, such as device count, in order to compare IMCs and MCs with traditional back to back topologies; however, no experimental validation of the losses distribution in the power converters have been shown. A proper understanding of these effects is critical for the detailed and accurate design of power converters above all in challenging and emerging applications. Therefore this paper presents a comparison between the DMC and IMC, in terms of losses distribution and including experimental validation, in three different design configurations (two for the IMC, one for the MC):

1) DMC with 18 SiC MOSFETs
2) IMC with 18 SiC MOSFETs
3) IMC with 6 SiC MOSFETs (on the output stage) and 12 IGBTs (on the input stage) [15]

The comparison presented in this paper will show the low frequency thermal behavior of the devices in the converters, which highlights the different loss distribution between the devices.
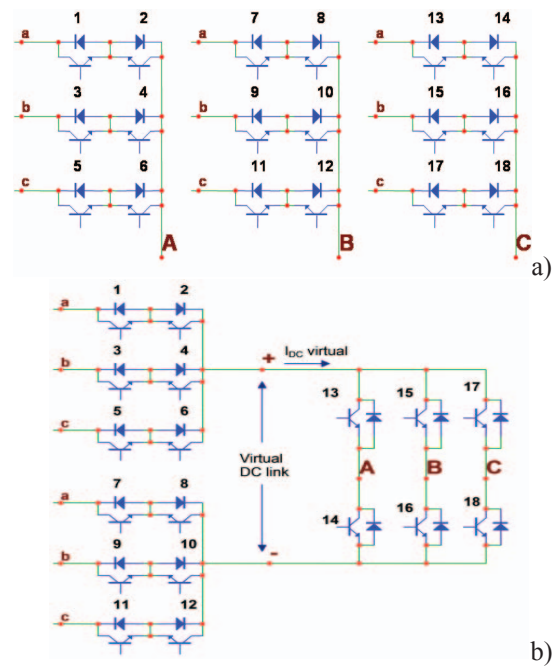

Fig. 1 Schematic circuits of the DMC (a) and the IMC (b), where a,b,c are the input connections and A,B,C are the output connections

II. CONVERTER MODULATION

In order to obtain a fair comparison, it is vital that both converters present the same performance regarding input and output waveform quality. In this study the same Space Vector Modulation (SVM) scheme was used for both converters [5],[20]-[21].

Table I Switching sequences for input current sector K_i=4 and output voltage sector K_V=1, for the DMC and for the IMC using three different ways to obtain the null vector

| | MATRIX CONVERTER | | | TWO STAGE MODULATION 1 | | | | | | TWO STAGE MODULATION 3 | | | | | |
| | OUTPUT PHASE | | | virtual dclink | | IDC_vir | inverter status | | | virtual dclink | | IDC_vir | inverter status | | |
time	A	B	C	+	-		A	B	C	+	-		A	B	C
T0/8	c	c	c	c	a	0	H	H	H	c	c	0	H	H	H
T1/2	c	c	a	c	a	(IA+IB)=-IC	H	H	L	c	a	(IA+IB)=-IC	H	H	L
T3/2	c	a	a	c	a	IA=-(IB+IC)	H	L	L	c	a	IA=-(IB+IC)	H	L	L
T0/4	a	a	a	c / b	a / a	0 / 0	L	L	L	a	a	0	L	L	L
T4/2	b	a	a	b	a	IA=-(IB+IC)	H	L	L	b	a	IA=-(IB+IC)	H	L	L
T2/2	b	b	a	b	a	(IA+IB)=-IC	H	H	L	b	a	(IA+IB)=-IC	H	H	L
T0/4	b	b	b	b / b	a / a	0 / 0	H	H	H	b / b	b / b	0	H	H	H
T2/2	b	b	a	b	a	(IA+IB)=-IC	H	H	L	b	a	(IA+IB)=-IC	H	H	L
T4/2	b	a	a	b	a	IA=-(IB+IC)	H	L	L	b	a	IA=-(IB+IC)	H	L	L
T0/4	a	a	a	b / c	a / a	0 / 0	L	L	L	a	a	0	L	L	L
T3/2	c	a	a	c	a	IA=-(IB+IC)	H	L	L	c	a	IA=-(IB+IC)	H	L	L
T1/2	c	c	a	c	a	(IA+IB)=-IC	H	H	L	c	a	(IA+IB)=-IC	H	H	L
T0/8	c	c	c	c	a	0	H	H	H	c	c	0	H	H	H

One of the main differences between the two converters operation mode is that using the IMC there can be two different ways to apply the same null vector, producing the following two strategies (named after [5]):

- Using only the output stage, referred to as *modulation one* [3],[5]
- Using also the input stage, referred to as *modulation three* [5],[12],[16]

Table I shows the switching sequence for a particular input/output sector when using a double-sided symmetrical arrangement of the active vectors and zero vectors. The vectors are arranged to minimize the number of commutations per modulation period and to use the three different types of zero vector. This arrangement of the vectors has been used for all three converters.

In Table I the red lines indicate the points where a hard commutation occurs, while the blue lines indicate where a soft commutation occurs at either zero current, for *modulation one,* or at zero voltage for *modulation three*. This arrangement of the active and zero vectors results in four commutations for each output current phase in each modulation period.

It is clear that, by using *modulation one* for the IMC, all the switching losses are concentrated in the output stage of the converter and the switching frequency of every device is twice the modulation frequency. If the same converter is operated using *modulation three* then the switching losses are distributed between the input and output stages. For this reason if *modulation one* is used for the IMC, it is a good idea to use fast SiC MOSFETs only for the output stage and use standard Si IGBTs for the input stage as the IGBTs will be more cost effective and there is no advantage to using very fast devices in a location in the circuit where there are no hard commutations. If *modulation three* is used for the IMC then all the switching devices should be the same, in this case all SiC MOSFETs.

When an IMC uses *modulation three,* two commutations occur at the same time. To make sure that the switching losses are seen in the input stage, a small delay time between these two coincident commutations must be applied (in our case this delay was set to 200nsec). By inserting this small delay the input stage will only conduct the current during the zero vector for a very short period of time. This input stage zero vector conduction time will be equal to the delay time and will therefore be insignificant in terms of additional conduction loss.

III EXPERIMENTAL TESTS FOR THE DEVICES THERMAL CYCLING

The losses in a MC are not function of the modulation index (ratio between output/input voltages), but only of the output current [9]. In an IMC the losses are also function of the modulation index and the type of modulation used. In all experimental tests and analysis regarding the low frequency thermal cycling of the power semiconductor devices in this paper, the modulation index was set to about 0.5; the actual reference demand for the output voltage has been differently set for each converter, so that the output current remained constant for the same load conditions. This choice was adopted because each converter has a different forward voltage drop for the same output voltage demand.

The converters were all tested at two different output current levels (6.67A and 10A) and two different switching frequencies (10kHz and 15kHz). The main difference between the two converter topologies is represented by the different losses distribution; this will generate a different thermal cycling between the devices. Various critical operating points can be defined for the two converter topologies. These critical operating points generate a very different power loss distribution between the semiconductor devices and are function of the ratio between the output frequency (f_{out}) and input frequency (f_{inp}) $\eta = f_{out}/f_{inp}$, where

in the majority of applications f_{inp} is fixed, and in this case equals to 50Hz.

The critical operating point for the IMC is when $\eta=0$ (ie. when the output frequency is zero and two devices in the output stage will take the majority of the converter conduction losses). The DMC, instead, presents more than one critical operating point: $\eta=0$, plus all points where the input frequency is a multiple of the output frequency or vice-versa; for example when $\eta=0.25$, $\eta=0.5$, $\eta=1$ and $\eta=2$. However the two most critical of these points are those for $\eta=0$ and $\eta=1$ (i.e. when the output frequency equals the input frequency and hence one switch in each leg takes the majority of the converter conduction losses). It would be very unusual for any power converter to work on these exact operating points for a significant amount of time. It is more likely that a converter would operate under conditions near these two critical operating points. For the cases $\eta=0.25$-0.5-1-2 the output frequency would have to be exactly synchronized to the input frequency. The case $\eta=0$ it is very rare; in fact even if the converter is used to drive a linear electro mechanical actuator, due to the backlash effect that is always present, the converter will never work precisely at $\eta=0$.

If the converter works very close to these critical operating points, the devices will present a low frequency thermal cycling; one of the purposes of this work is to show experimental data on the low frequency thermal cycling of the devices under these conditions and to make a comparison between the devices behavior in the two converters under these conditions. This low frequency thermal cycling is a critical design point for the power converter as it will define the required thermal paths needed for each device and will have a major role in the determination of the reliability and lifetime of the converter [16].

During the experimental tests the temperature of the semiconductor devices cases was recorded using a high speed thermal camera capable of a sampling frequency of 383Hz. Figs 2 to 5 show the thermal cycling of the devices for the three power converter configurations at different operating points.

For the MC it can be seen that the device temperatures oscillate slowly when the output frequency is low and also when the difference between the output frequency and the input frequency is low. As the output frequency or difference in output and input frequencies is increased, the magnitude of the temperature oscillations reduces The average temperatures of the 6 Matrix Converter devices (M7-M12) should theoretically be the same or should oscillate around the same value, since the losses are equal. However the experimental data highlights a range of case temperatures with a variation of up to 5ºC. There are two main reasons for this variation:

- the devices may not be identical: for example they may present small differences in $R_{DS,on}$ or in the properties of the internal thermal paths within the package which will generate different conducting losses or thermal resistances

- the temperature of the heat sink in not constant due to factors such as geometry

In both the IMC configurations the output stage devices (M13, M14) should have the same average temperature, but again a difference is noted due to the same reasons as for the variation shown in the MC circuit tests. For the IMC using *modulation 1* and using the Silicon IGBTs (M11 and M12) only the diode in M11 and the IGBT in M12 carry the current because $i_{dc\_virtual} > 0$ at all times (load power factor larger that 0.83). Hence the two packages will generate two different conduction losses. Using this modulation strategy there are also no hard switching losses in these two devices, hence the use of Silicon devices rather than Silicon Carbide. For the IMC using *modulation 3* the two devices in the input bridge (M11 and M12) are SiC devices. Since $i_{dc\_virtual} > 0$ at all times, there is no switching losses (expect for the recovery losses of the body diode) in M11, the turn-on and turn-off losses will therefore be concentrated in M12, as can be seen from Figs 5-8. The conduction losses for M11 and M12 in this case should be identical because they should have the same R_{DS}; however, as it was mentioned earlier this is maybe not true leading to a slight difference in the average losses in each device package.
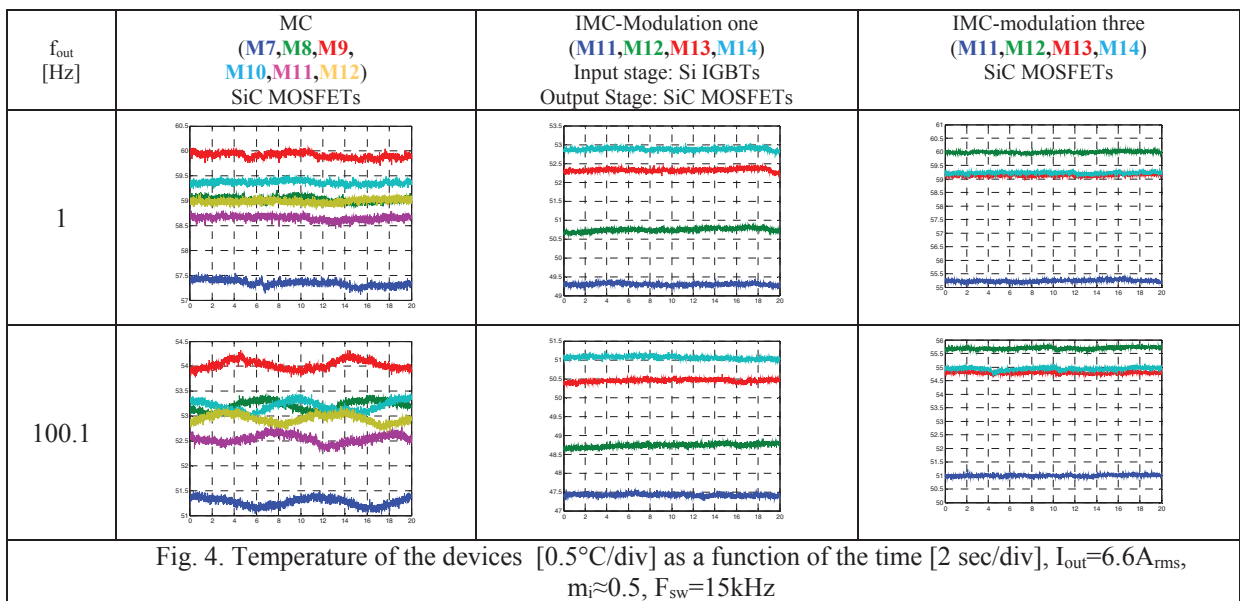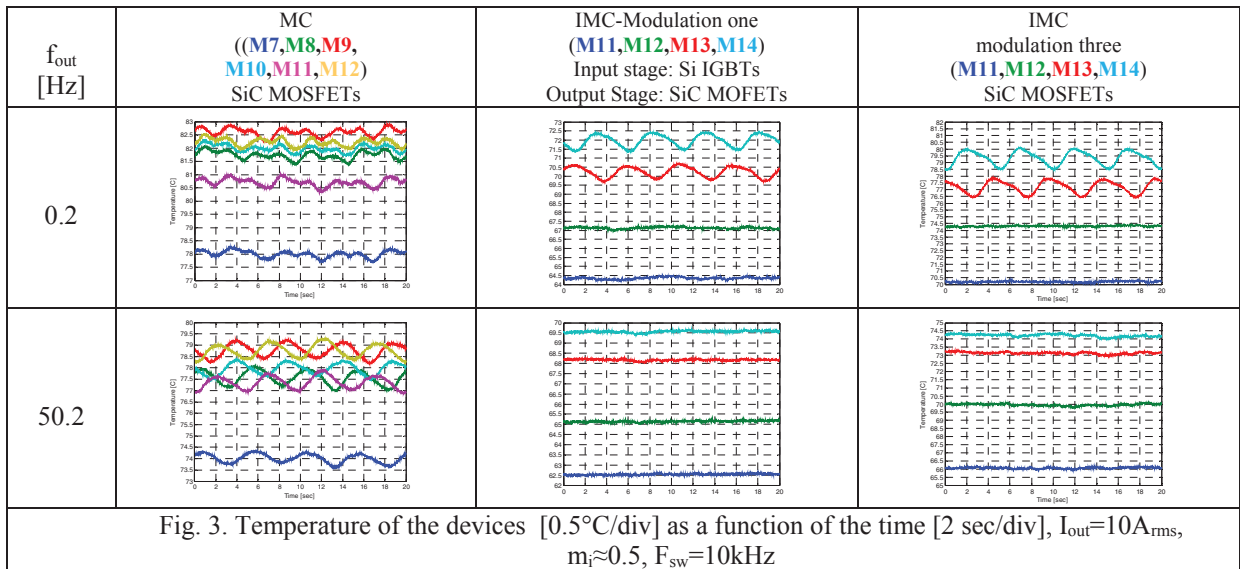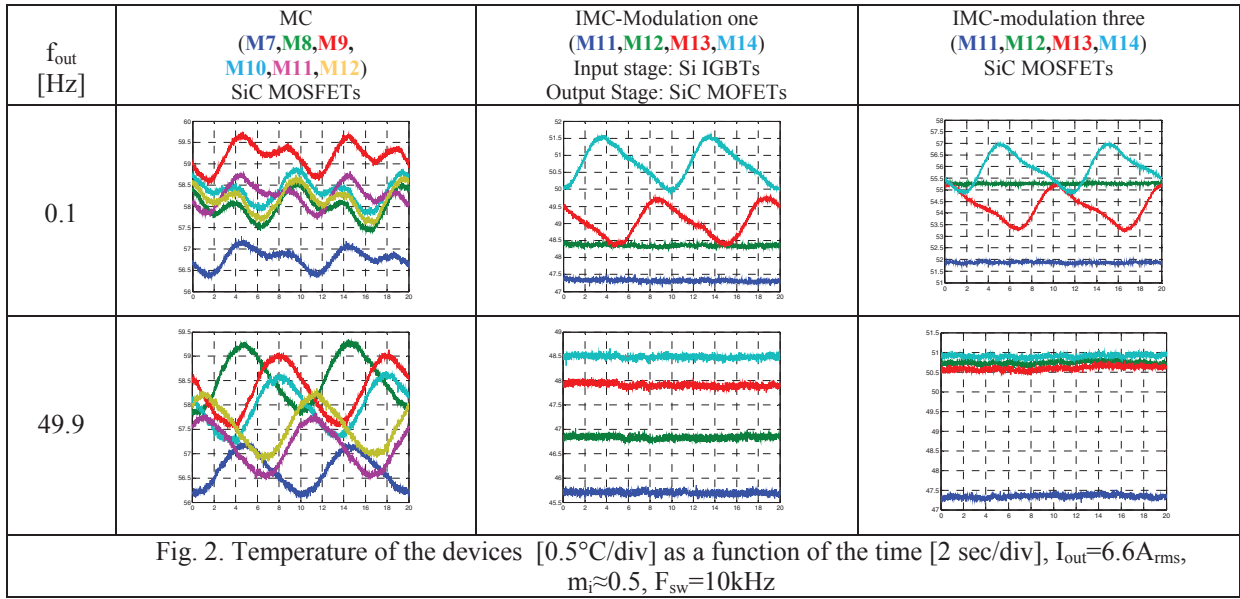
In both IMCs if the power flow of the converter is inverted (meaning $i_{dc\_virtual} < 0$) then the losses in M11 and M12 (all bidirectional switches) are inverted. For the MC there is no difference in the distribution of the power losses if the power flow is reversed. For the IMC it is clear that the output stage it is affected by the low frequency thermal cycles only around zero frequency as predicted, while the input stage it is not affect by the low thermal cycling. However there are differences between the losses in the two devices within each bidirectional switch and this depends on the power flow direction. It is also to be noticed that increasing the modulation frequency (F_{sw}) from 10kHz to 15kHz does not have a substantial impact on the temperature of the device packages because the additional switching losses in the SiC MOSFETs is low due to their fast switching times. This is a very useful property of these devices as it allows higher switching frequencies to be used, reducing the size of the required input filter to meet a given set of power quality standards.

Figures 6-8 show the different devices temperature of both converters under the same conditions of figure 5.

IV DEVICES JUNCTION TEMPERATURE ESTIMATION

Starting from the knowledge of the case temperature of each device package, it is possible to make an estimate of the temperature of the device junction using two assumptions:

o The cases itself will dissipate a very small amount of power compared to the device heat sink. The thermal resistance of the TO-247 SiC MOSFETs (on its own, without the heat sink) is around 40 °K/W, but the heat is dissipated mostly from the back of the devices, bolted here onto the heatsink, so it was assumed that the thermal resistance between the ambient air and the front of the case (R_{case_amb}) is double.
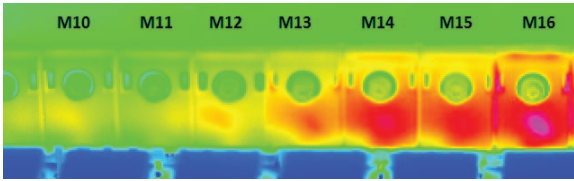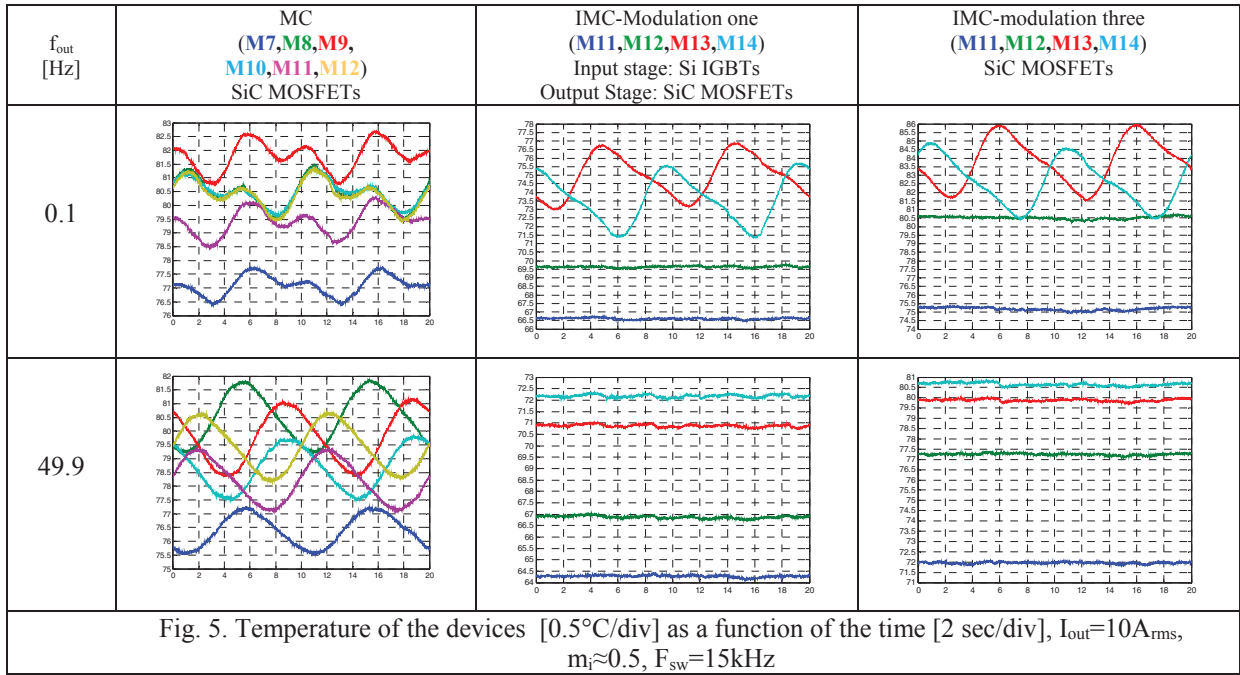
f_{out} [Hz]	MC (**M7**,**M8**,**M9**, **M10**,**M11**,**M12**) SiC MOSFETs	IMC-Modulation one (**M11**,**M12**,**M13**,**M14**) Input stage: Si IGBTs Output Stage: SiC MOFETs	IMC-modulation three (**M11**,**M12**,**M13**,**M14**) SiC MOSFETs
0.1			
49.9			

Fig. 2. Temperature of the devices [0.5°C/div] as a function of the time [2 sec/div], I_{out}=6.6A_{rms}, m_i≈0.5, F_{sw}=10kHz

f_{out} [Hz]	MC ((**M7**,**M8**,**M9**, **M10**,**M11**,**M12**) SiC MOSFETs	IMC-Modulation one (**M11**,**M12**,**M13**,**M14**) Input stage: Si IGBTs Output Stage: SiC MOFETs	IMC modulation three (**M11**,**M12**,**M13**,**M14**) SiC MOSFETs
0.2			
50.2			

Fig. 3. Temperature of the devices [0.5°C/div] as a function of the time [2 sec/div], I_{out}=10A_{rms}, m_i≈0.5, F_{sw}=10kHz

f_{out} [Hz]	MC (**M7**,**M8**,**M9**, **M10**,**M11**,**M12**) SiC MOSFETs	IMC-Modulation one (**M11**,**M12**,**M13**,**M14**) Input stage: Si IGBTs Output Stage: SiC MOSFETs	IMC-modulation three (**M11**,**M12**,**M13**,**M14**) SiC MOSFETs
1			
100.1			

Fig. 4. Temperature of the devices [0.5°C/div] as a function of the time [2 sec/div], I_{out}=6.6A_{rms}, m_i≈0.5, F_{sw}=15kHz

f_{out} [Hz]	MC (**M7**,**M8**,**M9**, **M10**,**M11**,**M12**) SiC MOSFETs	IMC-Modulation one (**M11**,**M12**,**M13**,**M14**) Input stage: Si IGBTs Output Stage: SiC MOSFETs	IMC-modulation three (**M11**,**M12**,**M13**,**M14**) SiC MOSFETs
0.1			
49.9			

Fig. 5. Temperature of the devices [0.5°C/div] as a function of the time [2 sec/div], I_{out}=10A$_{rms}$, m_i≈0.5, F_{sw}=15kHz

Fig. 6. Device temperatures for the IMC with *modulation one* f_{sw} = 15KHz, I_{out} = 10Arms, m_i≈0.5
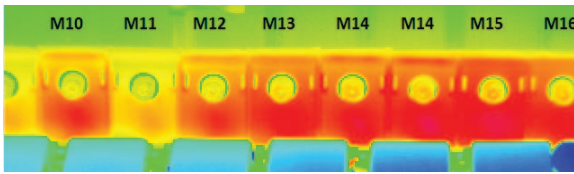
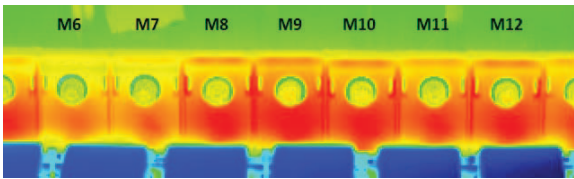Fig. 7. Device temperatures for the IMC with *modulation three,* f_{sw} = 15KHz, I_{out} = 10A , m_i≈0.5

Fig. 8. Device temperatures for the MC, f_{sw} = 15KHz, I_{out} = 10A, m_i≈0.5

- The thermal model between the device junction and the front of the case can be approximated with a first order filter as shown in Fig. 9.

In order to parameterize the thermal model a set of tests were conducted with a constant gate voltage V_{GS}=20V and a controlled drain current. Various parameters were then recorded including (with reference to Fig. 9): P_{mos}, $T_{\_heat\_sink}$, Ta_{mb} and T_{case_front}. The model parameters R1-R4 and C1-C4 were then extrapolated from the data sheet

information for the MOSFETs and R5 from the data sheet of the thermal pad utilized. Using this information it is then possible to find the value of the two parameters that were unknown: R_{case} and C_{case}. The time constant (τ=R_{case}*C_{case}) of the thermal model of the device packages has been calculated around 7.2 seconds. Using an FFT of the measured temperature of the device packages and multiplying each single harmonic by the gain of the filter used in the thermal model, an estimation temperature of the junction can be obtained. This procedure was applied up to a frequency of 10 Hz because for frequencies above this frequency the model becomes unreliable due to the accuracy of the model parameters.. The results of this process are shown in Fig. 10. From Fig. 10 it is clear that an oscillation of few degrees on the front of the packages can generate 30-40°C oscillation in the device junction temperature.
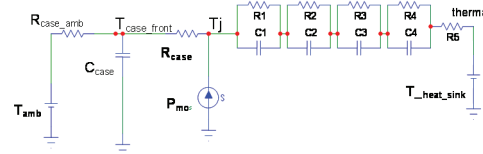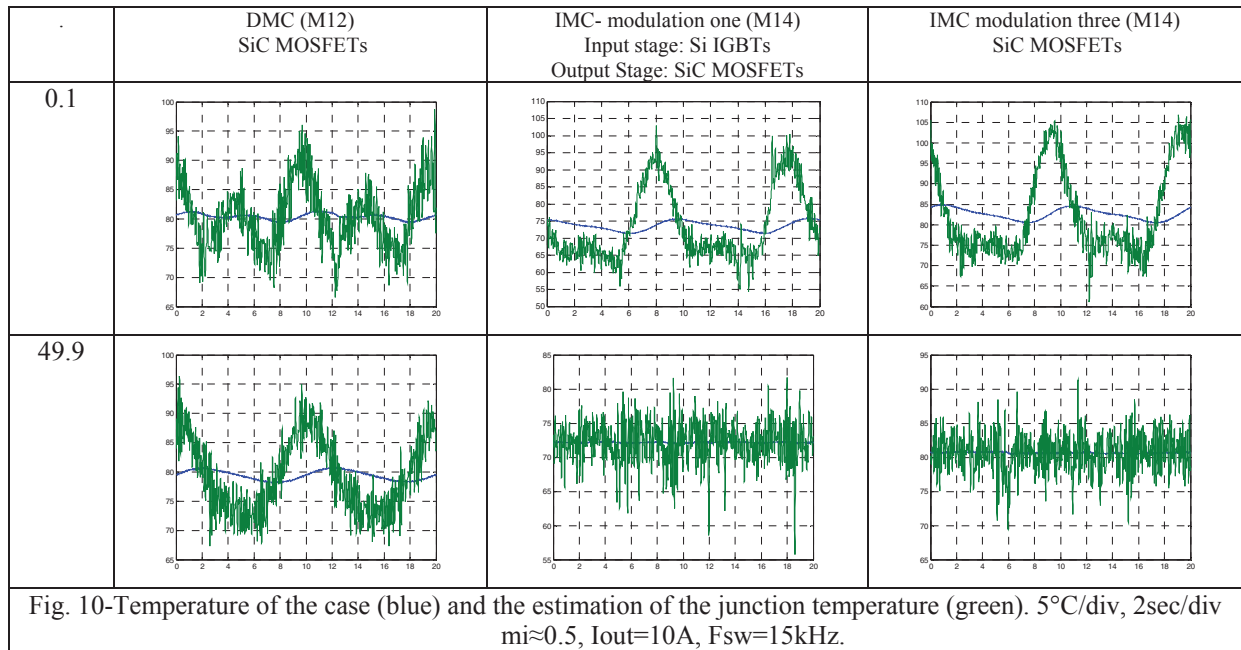

Fig. 9. Assumed Thermal Model of the TO-247 SiC MOSFETs

V CONLUCSION

This paper has compared the lower frequency thermal behavior of the devices within three direct AC/AC power converter configurations. From the observations of the low frequency thermal cycles of the single devices in each circuit configuration it can be concluded that the IMC has a not balanced losses distribution only at very low output frequency s, while the MC has the same problem also when the output frequency is identical or nearly identical to the input frequency. At low frequency (near zero Hz) the magnitude of the thermal cycling of the devices in the DMC

.	DMC (M12) SiC MOSFETs	IMC- modulation one (M14) Input stage: Si IGBTs Output Stage: SiC MOSFETs	IMC modulation three (M14) SiC MOSFETs
0.1			
49.9			

Fig. 10-Temperature of the case (blue) and the estimation of the junction temperature (green). 5°C/div, 2sec/div mi≈0.5, Iout=10A, Fsw=15kHz.

is lower than in the IMC case, which suggests that the DMC should be the "best choice" topology in applications where the converter is likely to be requested to generate low frequency currents, for example applications such as lifts or hoists. In applications where the output frequency is likely to be similar to the input frequency the use of an IMC it is instead the best choice; at high output frequency (>twice the input frequency) the distribution of losses in the MC are better than for the IMC.

In the IMC the output stage will have a very good distribution of losses between devices, but in the input stage the losses in the bidirectional switches are not equally distributed between the two devices. In the case of *modulation 1* with the IGBTs in the input stage, the losses are only in one diode and one IGBT; however in the case of *modulation 3* the switching losses of the bidirectional switches are concentrated in one MOSFET, assuming $i_{dc\_virtual}$ is unidirectional (loads with high power factor).

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