Z-Source Matrix Rectifier

Liu Hongchen[1], Ji Yuliang[1], Zhao Dan[1], Pat wheeler[2], Fan Guolei[1]

(1. School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin 150001, China)
(2. Department of Electrical and Electronics Engineering, University of Nottingham, Nottingham NG7 2RD, UK)

Abstract—This paper presents a novel Z-source matrix rectifier(ZSMR). To overcome the inherent disadvantage that the voltage transfer ratio for traditional matrix rectifier cannot be more than 0.866, a Z-source network has been combined with the matrix rectifier. The proposed rectifier realizes a voltage-boost function and the Z-source network also serves as power storage and guarantees double filtration grade at the output of the rectifier. The open-circuit zero state is required to obtain the voltage-boost function and ensure the output angle of the current vector to be invariant to obtain the expected power factor. In addition, to widely extend the voltage transfer ratio of the proposed rectifier, this paper presents the switched-inductor matrix rectifier(SL-ZSMR) and tapped-inductor matrix rectifier(TL-ZSMR). The corresponding circuit topologies, control strategies and operating principles are introduced. Both simulation and experiment results are shown to verify the theoretical analysis.

Index Terms—Z-source matrix rectifier, voltage-boost function, voltage transfer ratio

I. INTRODUCTION

The matrix rectifier (MR) originated from conventional matrix converter (MC) is a new type rectifier. Since the MR is the front-end rectification stage for indirect matrix converters, MRs and MCs share some same advantages such as input current with low harmonic content [1,8], controllable input power factor [2] and bidirectional energy flow [3]. The circuit has some potential applications and has recent attention in the field of power electronics [4]-[10]. For the high voltage ac-ac applications, the Z-source matrix converter is presented and researched such as the modulation strategies [11] and motor drives [12].

Similarly, the MR has some disadvantages that have restricted applications in the high voltage transfer ratio circumstance such as wind energy system [13] and electric vehicle charging system [14]. Since the Z-source network of the Z-source matrix rectifier presented by [15-18] serves as the filter at the dc side and does not play a voltage-boost role, the Z-source matrix rectifier presented by [15-18] is a voltage-buck ac-dc matrix rectifier, which does not satisfy the need for higher voltage transfer ratios. So, this paper presents a novel Z-source matrix rectifier (ZSMR) by improving the switch position, the switch count and the modulation scheme to realize the voltage-boost function.

In [19], the Z-source network was first proposed for solving voltage-boost problems in the traditional voltage source inverter. Z-source inverters can realize the voltage-boost ability through the shoot-through state, which solves the dead zone problem and reduces the associated harmonics. In [20-24], improved Z-source

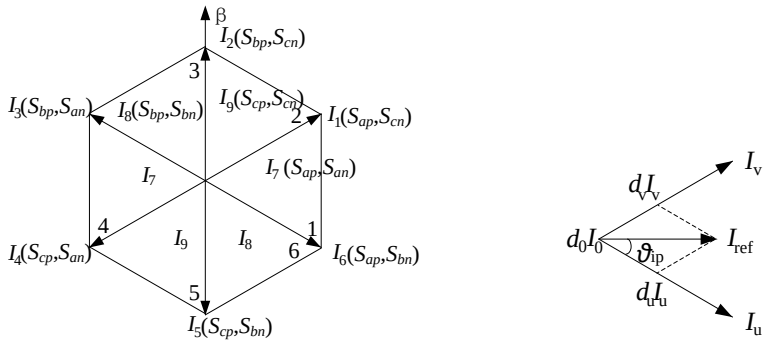
topologies with higher boost ability, reduced device voltage stress and improved the output quality are proposed.

The ZSMR can be constructed by putting a Z-source network between a matrix converter and the output filter, in which the position of Z-source network in ZSMR is different from that of a Z-source network in [19-24]. Not only does ZSMR reserve the original advantages of the MR but also it realizes the voltage-boost feature. At the same time, the Z-source network also serves as energy storage component and guarantees double filtration grade at the output of the ZSMR.

To improve the relationship between boost factor and the modulation index of the ZSMR, this paper propose to replace the Z-source inductor cell with a switched-inductor cell or a tapped-inductor cell. The resulting structures of ZSMR, SL-ZSMR and TL-ZSMR are similar to the Z-source inverters in [19, 20, 25]. The TL-ZSMR is more compact with its turn ratio freely adjustable to produce the desired voltage gain when compared to the ZSMR and SL-ZSMR.

II. MODULATION STRATEGY AND EXPERIMENTAL PRINCIPLE OF PROPOSED MATRIX RECTIFIERS

The modulation scheme for the traditional matrix rectifier can be achieved with a current-type Space Vector Pulse Width Modulation (SVPWM) strategy. As shown in Fig.1(a), one period of three-phase sinusoid input current can be divided into six sectors with nine switching states (six active states and three short zero states) [2].



(a) (b)

Fig.1.(a) Current space vector.(b) Current vector synthesis.

As shown in Fig.1(b), the input current vector at any direction and amplitude can be synthesized by the two nearest adjacent current vectors (I_i and I_{i+1}, i=1,…6) and one of the three zero vectors(I_7 , I_8, or I_9 when both of the upper and lower switches are short together). According to the current space vector synthesis theory, the reference vector can be expressed as follows:

$$I_{ref} = d_u I_u + d_v I_v + d_0 I_0 \tag{1}$$

d_u, d_v and d_0 can be written:

$$\begin{cases} d_u = \dfrac{T_u}{T_s} = \dfrac{2}{\sqrt{3}} \dfrac{|I_{ref}|}{|I_u|} \cdot \sin(\dfrac{\pi}{3} - \theta_i) = \dfrac{I_{im}}{I_{dc}} \cdot \sin(\dfrac{\pi}{3} - \theta_i) = m \sin(\dfrac{\pi}{3} - \theta_i) \\ d_v = \dfrac{T_v}{T_s} = \dfrac{2}{\sqrt{3}} \dfrac{|I_{ref}|}{|I_v|} \cdot \sin\theta_i = \dfrac{I_{im}}{I_{dc}} \cdot \sin\theta_i = m \sin\theta_i \\ d_0 = \dfrac{T_0}{T_s} = 1 - d_u - d_v \end{cases} \tag{2}$$

Where T_u is the operation interval of the starting vector, and T_v is the operation interval of the ending vector in the sector. θ_i is the angle between the reference vector and the starting vector, m ($m = \frac{I_{im}}{I_{dc}}$) is the modulation index and its range is between 0 and 1. In the sector 1, the input current I_{ref} can be expressed as follows:

$$I_{ref}=\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}=\begin{bmatrix} d_u+d_v \\ -d_u \\ -d_v \end{bmatrix} I_{dc}\begin{bmatrix} \cos(\omega_i t-\theta_i) \\ -\sin(\omega_i t-\theta_i) \\ -\sin\theta_i \end{bmatrix}=\frac{\sqrt{3}}{2}mI_{dc}\begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t-\frac{\pi}{2}) \\ \cos(\omega_i t+\frac{\pi}{2}) \end{bmatrix} \quad (3)$$

According to the equation (3), it is obvious that input reference current changes as the balanced three-phase sine law.

The above description is the modulation method used for traditional MRs, from which we can see that the traditional MR is a voltage-buck rectifier. So, to obtain the higher voltage-boost ratio, the modulation strategy for MRs should be modified. This paper introduces an extra open-circuit zero state forbidden in the matrix rectifier into the traditional current space vector control strategy.

An open-circuit zero state corresponds to the additional zero state different from traditional zero states produced by the shoot-though state of top and bottom arms (I_7, I_8, or I_9). The open-circuit zero state is the tenth switching state (I_{10}) where the switch S_1 is turned on and all the switching devices of the MR should be turned off to ensure the energy to flow from the capacitors to the inductors. The open-circuit zero state can solve the output open-circuit problem, which destroys the switch devices in a classical MR, and gives the Z-source inductor and inductive load current to a conduction path. The open-circuit zero state is similar to the shoot-though state in [17-23], and the non-open-circuit zero state is similar to nonshoot-though state.

To combine open-circuit zero state and keep the active states of the matrix rectifier unchanged, this paper proposes turning some of the short zero states(I_7, I_8, or I_9) into open-circuit zero states， as shown in Fig.2.(a) (operating at sector 1). Not only does the modified modulation strategy realize the voltage-boost feature in the open-circuit

zero state, but also ensure the angle of the output current vector to be invariant to obtain the expected power factor.

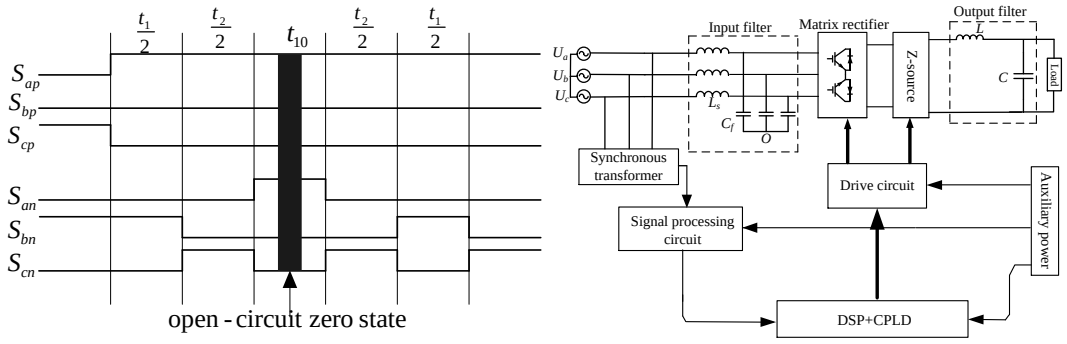


Fig.2. (a) open-circuit zero state inserted into tradition zero.(b) the system structure for the experimental ZSMR.

As shown in Fig.2(b), the ZSMR mainly consists of six parts: three-phase power, input filter, matrix rectifier, Z-source network, output filter and load. ZSMR is connected to the input voltage through the synchronous transformer. The measured input voltage is processed to realize the pass-zero comparison and voltage transform.

To realize unity input power factor, the modulation algorithm selects the output current vector angle to be consistent with the input voltage vector angle, which is determined from the measured three-phase voltages. From the calculated current vector angle, the output interval of starting vector and ending vector from equation (2) can be obtained. Therefore, the switch signals can be obtained and applied to the converter.

III. TOPOLOGY ANALYSIS OF THE PROPOSED MATRIX RECTIFIERS

A. ZSMR Topology Analysis

As shown in Fig.3(a), the MR includes twelve switching components which can be controlled to realize the chosen modulation scheme. The Z-source network includes inductors L_1 and L_2, capacitors C_1 and C_2 and a parallel IGBT.

The circuit is similar to Z-source inverters [19] in that the operation states in a period are divided into two states: the open-circuit zero state(I_{10}) and non-open-circuit zero states $(I_1 \sim I_9)$. If the system is in open-circuit zero state, S_1 is on and Z-source network is disconnected with the MR. The equivalent circuit is shown in Fig.3(b). It can be seen that the energy stored in the capacitors transfers to the inductors. If the system is in a non-open-circuit zero state, then S_1 is off and the load is supplied by the MR and the Z-source network. The equivalent circuit is shown in Fig.3(c). It can be seen that the energy stored in the capacitors is supplied by matrix rectifier.

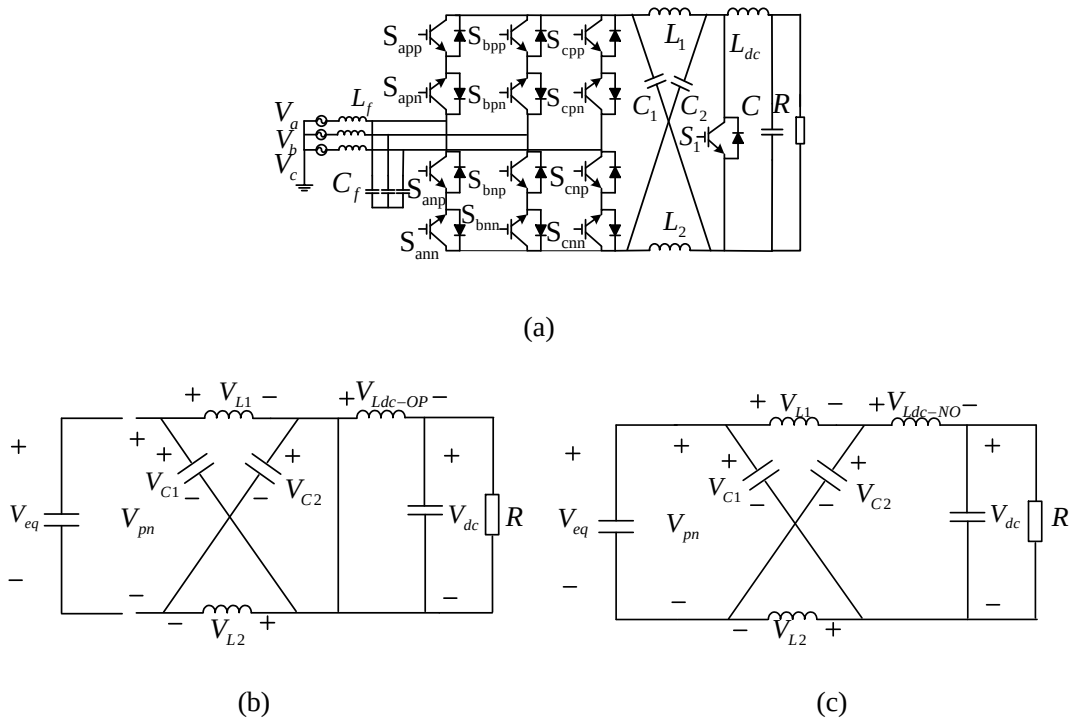


Fig.3. (a) The proposed Z-source matrix rectifier (b) Equivalent circuit of open-circuit zero state (c) Equivalent circuit of non-open-circuit zero state

According to the chosen MR modulation scheme, the average output voltage V_{eq} of MR can be expressed as follows [26]:

$$V_{dc} = d_u(u_a - u_b) + d_v(u_a - u_c) + d_0(u_a - u_a) = \frac{3}{2} m V_{im} \cos\varphi_i \qquad (4)$$

V_{im} is the amplitude of the input phase voltage and φ_i is input power factor angle. From (4), we know that the output voltage range of the matrix rectifier can be $(0 \sim 1.5)V_{im}$. Due to the symmetry of Z-source network, the values of inductances and capacitors are usually chosen to be equal, $L_1 = L_2 = L$ and $C_1 = C_2 = C$. Form the equivalent circuit, we can obtain the equations for Z-source inductors and capacitors:

$$V_{L1} = V_{L2} = V_L, \quad V_{C1} = V_{C2} = V_C \tag{5}$$

As shown in Fig.3 (b), it can be shown that:

$$V_{L-OP} = V_C, \quad V_{Ldc-OP} = -V_{dc} \tag{6}$$

Similarly, we can obtain from Fig.3 (c):

$$V_{L-NO} = V_{eq} - V_C, \quad V_{Ldc-NO} = V_C - V_{dc} - V_{L-NO} \tag{7}$$

Where V_{eq} is the dc-link voltage, and V_{dc} is the dc output voltage. $V_{Ldc\text{-}OP}$ and $V_{Ldc\text{-}NO}$ are the filter inductor voltages in the open-circuit zero state and non-open-circuit zero state. Similarly, $V_{L\text{-}OP}$ and $V_{L\text{-}NO}$ are the Z-source inductor voltages.

The average voltage across the inductor over one switching period should be zero in steady state, therefore from (6) and (7) :

$$T_0(V_C) + T_1(V_{eq} - V_C) = 0 \tag{8}$$

$$\text{Hence,} \quad \frac{V_C}{V_{eq}} = \frac{T_1}{T_1 - T_0} = \frac{1 - D}{1 - 2D} \tag{9}$$

Similarly, applying volt-second balance to filter inductor L_{dc},

$$T_0(-V_{dc}) + T_1(2V_C - V_{eq} - V_{dc}) = 0 \tag{10}$$

Where T_0 is the interval of the open-circuit zero state, D is the open-circuit duty cycle. We can obtain the relationship between V_{dc} and V_{eq} from (10):

$$\frac{V_{dc}}{V_{eq}} = \frac{T_1}{T_1 - T_0} \tag{11}$$

Therefore the boost factor B_z can be derived:

$$B_z = \frac{V_{dc}}{V_{eq}} = \frac{T_1}{T_1 - T_0} = \frac{1-D}{1-2D} \tag{12}$$

From (4) and (12), the output voltage can be expressed by:

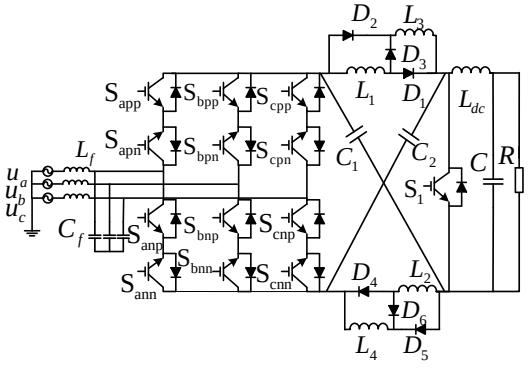
$$V_{dc} = \frac{3}{2} \cdot m \cdot V_{im} \cdot \cos\varphi_i \cdot B_z \tag{13}$$

Where $0 \le \cos\varphi_i \le 1 \text{and} 0 \le m \le 1$. M($M = m \cdot \cos\varphi_i$) is the modulation index with a value range between 0 and 1. So, the output voltage range of the ZSMR is $(0-0.866)B_z \cdot \sqrt{3}V_{im}$. The voltage transfer ratio of ZSMR can be obtained:

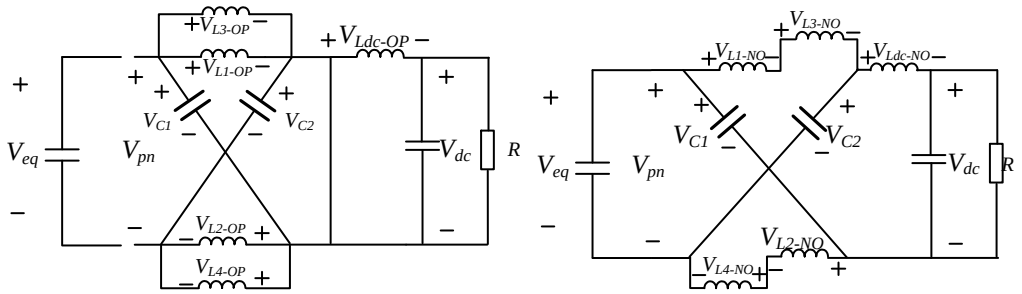
$$G_Z = \frac{V_{dc}}{\sqrt{3}V_{im}} = \frac{\sqrt{3}}{2} M \cdot B_z = \frac{\sqrt{3}}{2} M \cdot \frac{1-D}{1-2D} \tag{14}$$

B SL-ZSMR Topology Analysis

In [20], a SL cell is introduced into the Z-source network to enlarge voltage-boost ability. Consequently, the SL-ZSMR is proposed as shown in Fig.4(a). The inductors of the Z-source network are replaced by the SL cell, and the other parts have not been changed. The top SL cell consists of two inductors (L_1 and L_3) and three additional diodes (D_1, D_2 and D_3). Similarly, the bottom SL cell consists of L_2, L_4, D_4, D_5, D_6.



(a)



(b) (c)

Fig. 4. (a)The proposed switched-inductor Z-source matrix rectifier (b) Equivalent circuit of open-circuit zero state (c) Equivalent circuit of non-open-circuit zero state.

The same states also exist in SL-ZSMR: including the open-circuit zero state and non-open-circuit zero states. If switch S_1 is on, the proposed SL-ZSMR operates in an open-circuit zero state. For the top SL cell, D_1 and D_2 are on, and D_3 is off. L_1 and L_3 are charged by C_1 in parallel. For the bottom SL cell, D_4 and D_5 are on, and D_6 is off. L_2 and L_4 are charged by C_2 in parallel. Its equivalent circuit is shown in Fig.4 (b). It can be shown that both the top and bottom SL cells perform the same function, absorbing the energy stored in the capacitors. If switch S_1 is off, SL-ZSMR operates in the non-open-circuit zero state. For the top SL cell, D_1 and D_2 are off, and D_3 is on. L_1 and L_3 are connected in series. D_4 and D_5 are off, and D_6 is on in the bottom SL cell. L_2 and L_4 are connected in series. The equivalent circuit is shown in Fig.4 (c) and the energy stored in inductances is transferred to the main circuit.

For the convenience of mathematical derivation, the values of inductances and capacitors are usually chosen to be equal. Therefore the Z-source capacitor voltage is:

$$V_{C1} = V_{C2} = V_C \tag{15}$$

According to the equivalent circuit in Fig.4 (b), we have

$$V_{L1-OP} = V_{L3-OP} = V_C, \quad V_{Ldc-OP} = -V_{dc} \tag{16}$$

Similarly, from the equivalent circuit in Fig.4 (c),

$$V_{eq} = V_C + V_{L1-NO} + V_{L3-NO},\ V_{Ldc-NO} = V_C - (V_{L1-NO} + V_{L3-NO}) - V_{dc} \tag{17}$$

Applying the volt-second balance principle to L_1, it can be shown that the corresponding voltage across L_1 during non-open-circuit zero state, $V_{L1\text{-}NO}$, can be expressed by:

$$V_{L1-NO} = -\frac{D}{1-D} V_C \tag{18}$$

Applying the volt-second balance principle to L_3, we have:

$$T_0 V_C + T_1 (V_{eq} - V_C + V_{L1-NO}) = 0 \tag{19}$$

Hence,

$$V_{C1} = V_{C2} = V_C = \frac{1-D}{1-3D} V_{eq} \tag{20}$$

Applying the volt-second balance principle to L_{dc}, the following equations can be obtained from (16) and (17):

$$T_0 (-V_{dc}) + T_1 (V_C - V_{L1-NO} - V_{L3-NO} - V_{dc}) = 0 \tag{21}$$

This gives the relationship of V_{dc} and V_{eq}:

$$\frac{V_{dc}}{V_{eq}} = \frac{1-D^2}{1-3D} \tag{22}$$

So, B_{SL}, the boost factor of SL-ZSMR, can be expressed as:

$$B_{SL} = \frac{(T_1 + 2T_0)T_1}{T_1 - 2T_0} = \frac{1-D^2}{1-3D} \tag{23}$$

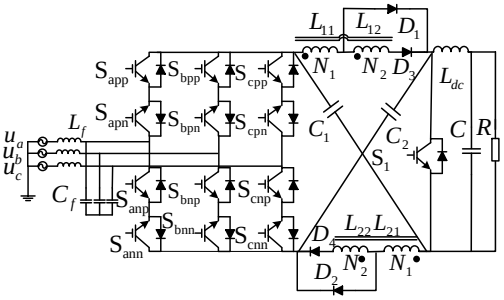
Similarly, the voltage transfer ratio of SL-ZSMR can be obtained:

$$G_{z-s} = \frac{V_{dc}}{\sqrt{3} V_{im}} = \frac{\sqrt{3}}{2} M \cdot B_{SL} = \frac{\sqrt{3}}{2} M \cdot \frac{1-D^2}{1-3D} \tag{24}$$

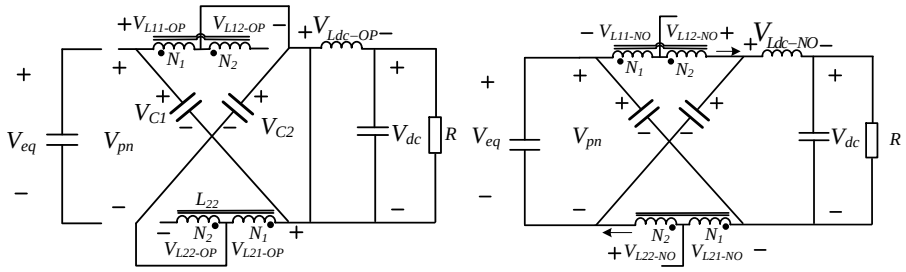
C. TL-ZSMR Topology Analysis

The topology of the TL-ZSMR is shown in Fig.5(a). The TL cells consist of tapped

inductors (L_{11}, L_{12}, L_{21}, L_{22}), four additional diodes (D_1, D_2, D_3 and D_4) and two capacitors (C_1 and C_2). The combination of L_{11}-L_{12}-D_1-D_3 performs the function of the top TL cell and the combination of L_{21}-L_{22}-D_2-D_4 performs the function of the bottom TL cell.



(a)



(b) (c)

Fig.5. (a)The proposed tapped-inductor Z-source matrix rectifier (b) Equivalent circuit of open-circuit zero state (c) Equivalent circuit of non-open-circuit zero state

If switch S_1 is on, then the TL-ZSMR operates in the open-circuit zero state. For the top TL cell, D_1 is on, and D_3 is off. L_{11} is charged by C_1 in parallel. For the bottom TL cell, D_2 is on, and D_4 is off. L_{21} is charged by C_2 in parallel. The equivalent circuit is shown in Fig.5 (b). It can be seen that both the top and bottom TL cells perform the same function to absorb the energy stored in the capacitors. In the non-open-circuit zero state, the S_1 is off. For the top cell, D_1 is off and D_3 are on. L_{11} and L_{12} are connected in series. For the bottom TL cell, D_2 is off, and D_4 is on. L_{21} and L_{22} are connected in series. The equivalent circuit is shown in Fig.5 (c) and the energy stored

in tapped-inductor cells is transferred to the main circuit. The capacitor C_1 is charged by V_{eq} via the bottom TL cell, hence the capacitor C_2 is charged via the top TL cell.

The inductors and capacitors are usually chosen to be equal.

$$V_{C1} = V_{C2} = V_C \tag{25}$$

For the TL cells, their turn ratios are also set to be the equal, $N = N_2 / N_1$, where N_1 is the number of winding L_{11} and L_{21}, and N_2 is the number of winding L_{12} and L_{22}. With these inductive symbols defined, the expressions relating them can be deduced,

$$\begin{cases} L_{11} = L_{21} = (\dfrac{N_1}{N_1 + N_2})^2 L = (\dfrac{1}{1+N})^2 L \\ L_{12} = L_{22} = (\dfrac{N_2}{N_1 + N_2})^2 L = (\dfrac{N}{1+N})^2 L \end{cases} \tag{26}$$

Besides the self-inductances, the mutual inductance L_M of the TL cells should also be considered, since it provides a means for measuring energy coupling efficiency within each TL cell. For an ideal TL cell whose coupling coefficient k is 1, L_M can be simplified to:

$$L_M = k\sqrt{L_{11}L_{12}} = \frac{N}{(1+N)^2} L \tag{27}$$

As for the TL cells, current flowing through L_{11} as an example is noted to increase during open-circuit zero state, and decrease during non-open-circuit zero state.

From the equivalent circuit in Fig.5 (b), we can obtain:

$$V_{L11-OP} = V_{L21-OP} = V_C\,,\ \ V_{Ldc-OP} = -V_{dc} \tag{28}$$

According to the equivalent circuit in Fig.5 (c), we have:

$$V_{eq} = V_C + V_{L11-NO} + V_{L12-NO}\,, V_{Ldc-NO} = V_C - (V_{L11-NO} + V_{L12-NO}) - V_{dc} \tag{29}$$

Where $V_{L11\text{-}OP}$ and $V_{L12\text{-}OP}$ are the voltages for tapped-inductor winding L_{11} *and* L_{12} in open-circuit zero state. Similarly, $V_{L11\text{-}NO}$ and $V_{L12\text{-}NO}$ are the voltages in non-open-circuit zero state.

The magnetic fluxes within TL cells are designed to increase linearly during

open-circuit zero state:

$$V_{L11-OP} = N_1 \frac{d\varphi_{L11-S}}{dt} \quad , \quad V_{L12-OP} = N_2 \frac{d\varphi_{L11-M}}{dt} \tag{30}$$

φ_{L11-S} is the self magnetic flux produced by $i_{L11\text{-}op}$ for linking the coil of L_{11}. In contrast, φ_{L11-M} is the mutual magnetic flux produced by $i_{L11\text{-}op}$ for linking the coil of L_{12}. For a perfectly coupled TL, φ_{L11-S} and φ_{L11-M} are equal, inferring that $V_{L12\text{-}OP}$ can be rewritten as:

$$V_{L12-OP} = NN_1 \frac{d\varphi_{L11-S}}{dt} = NV_{L11-OP} \tag{31}$$

Applying the volt-second balance principle to L_{11}, the corresponding voltage across L_{11} during non-open-circuit zero state, $V_{L1\text{-}NO}$, can be expressed:

$$V_{L11-NO} = -\frac{D}{1-D} V_C \tag{32}$$

Applying the volt-second balance principle to L_{12}, we have

$$T_0 V_{L12-OP} + T_1 V_{L12-NO} = 0 \tag{33}$$

Hence,

$$V_{L12-NO} = -\frac{ND}{1-D} V_C \tag{34}$$

From (28)to (34), we have:

$$V_C = \frac{1-D}{1-2D-DN} V_{eq} \tag{35}$$

From (28) ,(29)and (35), we have:

$$T_0(-V_{dc}) + T_1(V_C - V_{L11-NO} - V_{L12-NO} - V_{dc}) = 0 \tag{36}$$

$$\text{So,} \quad \frac{V_{dc}}{V_{eq}} = \frac{(1-D)(1+DN)}{1-2D-DN} \tag{37}$$

Hence, B_{TL}, the boost factor of TL-ZSMR, can be expressed by:

$$B_{TL} = \frac{(1-T_0/T)(1+(T_0/T)N)}{1-2(T_0/T)-(T_0/T)N} = \frac{(1-D)(1+DN)}{1-2D-DN} \tag{38}$$

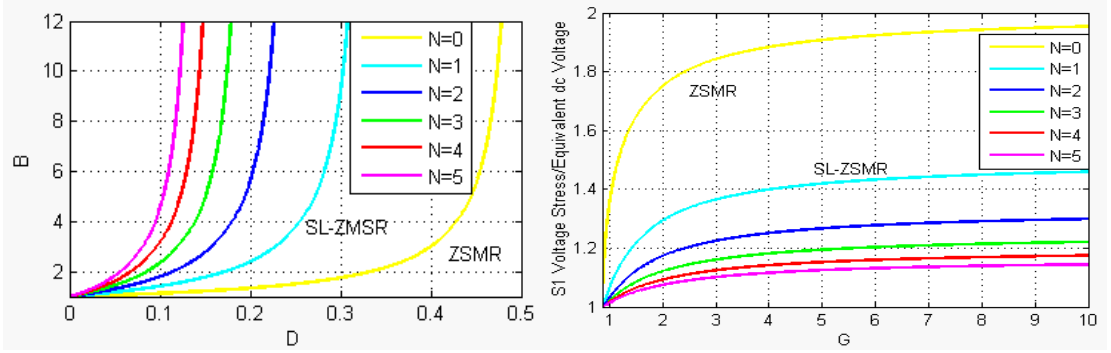
Similarly, the voltage transfer ratio of TL-ZSMR can be obtained

$$G_{z-T} = \frac{V_{dc}}{\sqrt{3}V_{im}} = \frac{\sqrt{3}}{2}M \cdot B_{TL} = \frac{\sqrt{3}}{2}M \cdot \frac{(1-D)(1+DN)}{1-2D-DN} \tag{39}$$

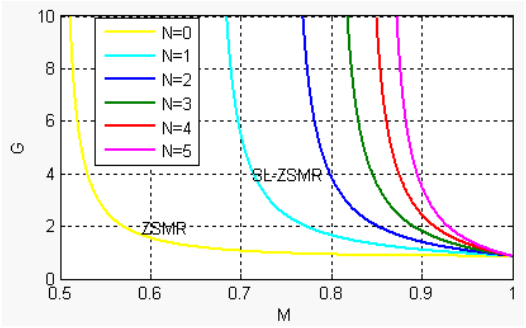
IV. FEATURES COMPARISON

A. Feature Comparisons Of Proposed Rectifiers

The boost factors *B* versus *D* for the ZMSR, SL-ZSMR and TL-ZSMR with various turn ratios are shown in Fig.6 (a). When N=0, $B = \frac{1-D}{1-2D}$, the secondary winding of tapped inductor is omitted, and the TL-ZSMR becomes a ZSMR. When $N = 1$, $B = \frac{1-D^2}{1-3D}$, the boost factor is equal to that of SL-ZSMR. It can be seen that the voltage-boost capability of the proposed TL network at a specified *D* value improves as *N* increases. The voltage stress for switching device is different under different voltage-boost levels. Fig.6(b) shows the voltage stress comparison of switching device S_1 for the ZMSR, SL-ZSMR and TL-ZSMR. As shown in Fig.6(b), for the same output voltage gain, the proposed TL-ZSMR has a lower voltage stress compared ZSMR and SL-ZSMR as *N* increases.



(a) (b)



(c)

Fig.6. (a)Boost ability of proposed ZMSR,SL-ZSMR and TL-ZSMR with various turn ratios of N (b)Switching device S_1 voltage stress of proposed ZMSR,SL-ZSMR and TL-ZSMR with various turn ratios of N (c) Voltage conversion ratios versus modulation index of proposed ZMSR, SL-ZSMR and TL-ZSMR with various turn ratios of N.

Fig.6(c) shows the voltage conversion ratios versus modulation indices of the proposed three rectifiers. The proposed three rectifiers can all provide higher voltage boost inversion by using the same modulation index. For the same output voltage gain, the proposed TL-ZSMR uses a higher modulation index to decrease the total harmonic distortion value and improve the rectifier output quality. Table I compares the corresponding governing equations of the proposed ZSMR, SL-ZSMR and TL-ZSMR. From Table I, it can be seen that the TL-ZSMR has the higher voltage stresses of diodes and capacitors due to its stronger voltage-boost ability in the same D.

TABLE I

Stress comparison to three topologies

	ZSMR	SLZSMR	TLZSMR(N=2)
V_c / V_{eq}	$\frac{1-D}{1-2D}$	$\frac{1-D}{1-3D}$	$\frac{1-D}{1-4D}$
V_{dc} / V_{eq}	$\frac{1-D}{1-2D}$	$\frac{1-D^2}{1-3D}$	$\frac{1+D-2D^2}{1-4D}$

Diode stress	0	$\frac{D}{1-3D}$ (D_1) $\frac{1-D}{1-3D}$ (D_3)	$\frac{2D}{1-4D}$ (D_1) $\frac{2(1-D)}{1-4D}$ (D_3)
$G=\frac{V_{dc}}{\sqrt{3}V_{im}}$	$\frac{\sqrt{3}}{2}M\frac{1-D}{1-2D}$	$\frac{\sqrt{3}}{2}M\frac{1-D^2}{1-3D}$	$\frac{\sqrt{3}}{2}M\frac{1+D-2D^2}{1-4D}$

B. Differences Among Proposed Rectifiers And Converters Published In Other References

The converters [4-7] are the traditional ac-ac matrix converters without the Z-source network and the voltage-boost function. The converters [11, 12] are the voltage-boost ac-ac Z-source matrix converters but without the ac-dc rectifier function. The converters [15-18], different from ac-ac Z-source matrix converters [11, 12], can realize the ac-dc rectifier function but a buck Z-source matrix rectifier. The differences among proposed rectifiers and the converter [15] by “keping you” are analyzed as follows.

Firstly, the topology differences among proposed rectifiers and converter [15] are shown in Table II. From Table II, it can be seen that the component counts of proposed rectifiers are different from those of the converter [15]. As shown in Fig.7(a), the converter [15] includes three switches (*X1*, *X2* and *S1*) and a battery. The three switch count and the switch position are different from those of proposed rectifiers and proposed rectifiers do not include the battery, which are the topology differences among proposed ZSMR and the converter [15]. From Fig.4 and Fig.5, it can be seen that the proposed SL-ZSMR and TL-ZSMR exist the larger topology differences compared with the converter [15].

Secondly, the topology differences among proposed rectifiers and the converter [15]

need different operation principles. The proposed ZSMR, SL-ZSMR and TL-ZSMR introduce the additional open-circuit zero state where the switch S_1 is turned on and all the switching devices to realize the voltage-boost ac-dc function. The auxiliary switch S_1 ensures the energy to flow from the capacitors (C_1 and C_2) to the inductors (L_1 and L_2) and provides the conduction path for the capacitor C and inductor L_{dc}. The equivalent circuits of proposed ZSMR, SL-ZSMR and TL-ZSMR are shown in Fig.3, Fig.4 and Fig.5.

Differently, the auxiliary switch *X1* and the diode *D* of the rectifier in [15] mainly block the energy flow and the current of three-phase ac sources to the battery. Fig.7(b) shows the equivalent configuration of the converter [15] in ac-dc rectification mode. In this mode, the switch *X1* and *S1* are in the OFF-state; *X2* and *X3* are closed. As shown in Fig.7(b), the Z-source network of the converter in [15] under ac-dc rectification mode serves as the filter at the dc side. The converter in [15] without the voltage-boost process is a ac-dc buck rectifier, which is essential difference from proposed rectifiers.

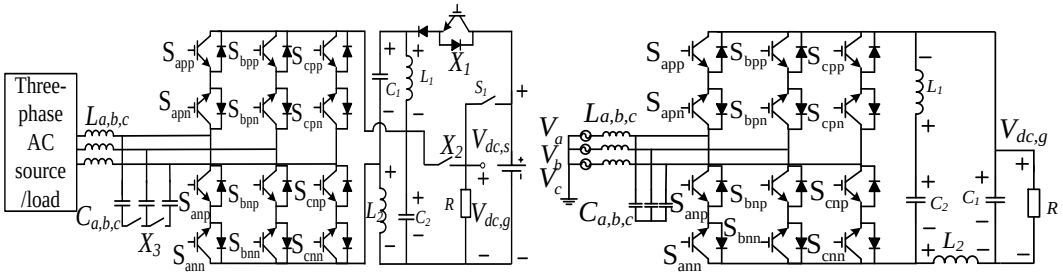


Fig.7. (a) The general topology structure in [15] and (b) Equivalent structure of the converter in [15] when it is in the ac-dc rectification mode.

TABLE II

The topology differences among proposed rectifiers and rectifiers [15]

Topology	ZSMR	SL-ZSMR	TL-ZSMR	rectifier in [15]
Numbers of switches	13	13	13	17
Numbers of diodes	0	6	4	1
Numbers of inductors	6	8	6	5
Numbers of capacitors	6	6	6	5

V. SIMULATION VERIFICATION

To verify the theoretical analysis for the proposed ZSMR, SL-ZSMR and TL-ZSMR, simulations are set up for the topologies shown in Fig.3(a), Fig.4(a) and Fig.5(a). The balanced three-phase input voltage for these three simulations is 20V/50Hz, and the load per phase is 10Ω. For the ZSMR L_1=L_2=2mH and C_1=C_2=470uF; for the SL-ZSMR L_1=L_2=L_3=L_4=1mH and C_1=C_2=470uF; and for the TL-ZSMR L_{11}=L_{21}=0.22mH, L_{12}=L_{22}=0.88mH and C_1=C_2=470uF. In the simulations, all the components are assumed to be ideal.

The simulation results are shown in Fig.8, Fig.9 and Fig.10 for the ZSMR, SLZSMR and TLZSMR respectively for the condition when M=0.8 and D=0.1. It can be seen from Fig.8 that the capacitor voltage V_C and output voltage V_{dc} are 26.5V which is closed to the theoretical value 27V calculated from (9) and (13). Then, from (12) and (14), we get the voltage transfer ratio G=0.779 and the boost factor B=1.125. Fig.8 also shows the enlarged waveform of Z-source inductor current I_{L1}. It can be seen from the Fig.8 that the inductor charges or discharges when S_1 is turned on or off.

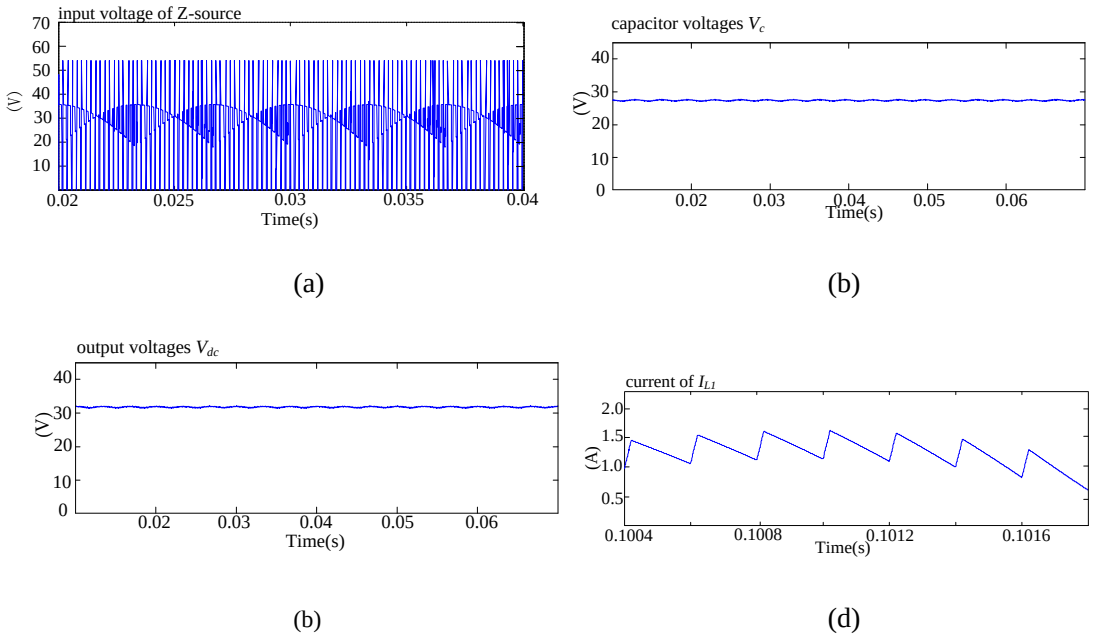
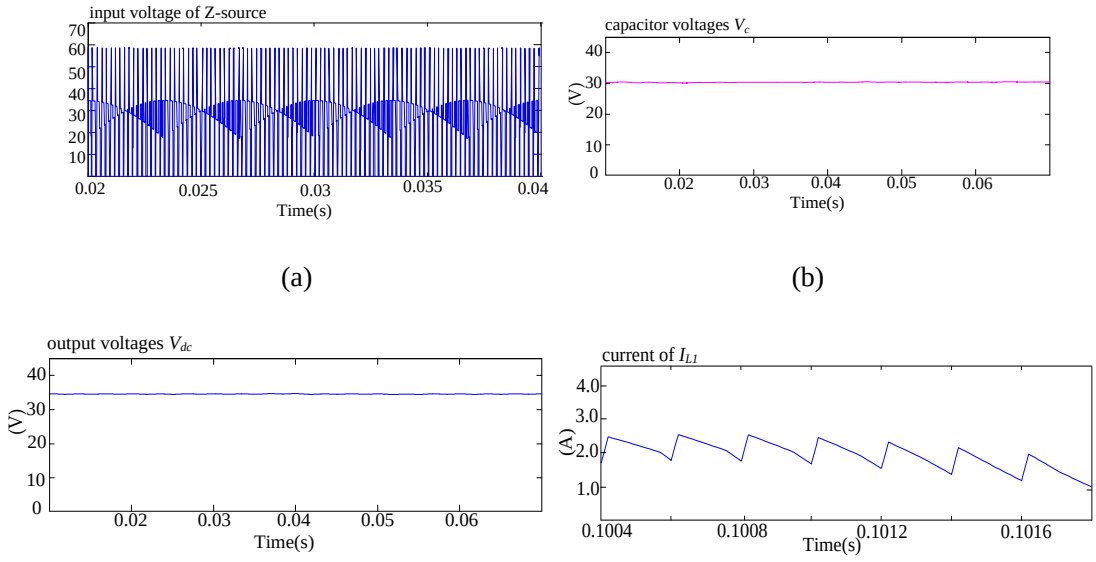


Fig.8. Simulation results of ZSMR

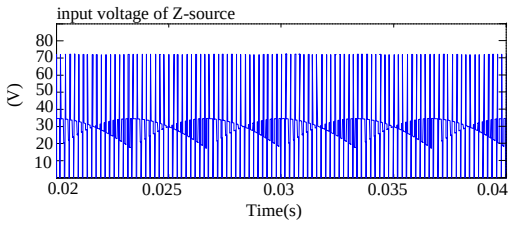
As shown in Fig.9, it can be seen that the capacitor voltage V_C is 30.2V close to the theoretical value of 30.86V, and the output voltage V_{dc} is 33.5V which is close to the theoretical value of 33.94V. It is obvious that the input voltage of Z-source network, the capacitor voltage and the output voltage for SL-ZSMR are much higher than those of the ZSMR for the same D and M. So, the corresponding voltage transfer ratio, 0.975 from (24), is greater than ZSMR, verifying that the voltage-boost ability of the circuit is significantly higher.



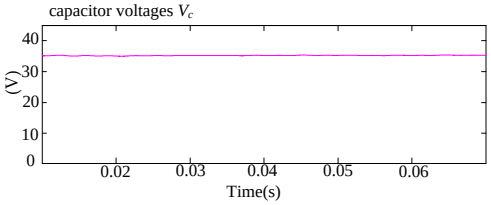
(b) (d)

Fig.9. Simulation results of SL-ZSMR

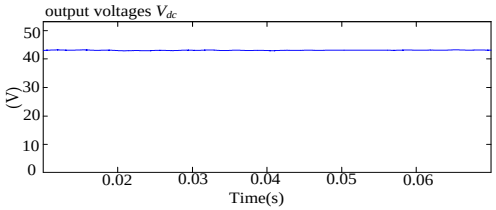
The voltage transfer ratio can be realized optimally by the proposed TL-ZSMR, as shown in Fig.10. From Fig.10, it can be seen that the capacitor voltage V_C and output voltage V_{dc} are consistent with the theoretical values, and the input voltage of Z-source network is the highest of the three topologies. The corresponding voltage transfer ratio is 1.24 calculated by equation (39). Obviously, when D and M are the same, the voltage transfer ratio of the TL-ZSMR is the highest. Fig.10 also shows the enlarged waveforms of the current of tapped-inductor L_{L11} and L_{L12}, and it can be seen that the waveforms of I_{L11} and I_{L12} are complementary, which is consistent with the theoretical analysis. So, by the simulations, we have verified the availability of the proposed rectifiers.



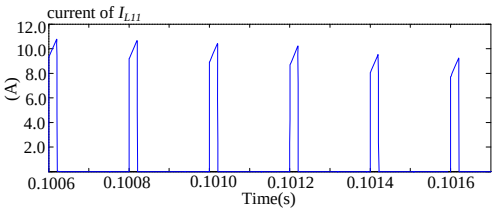
(a)



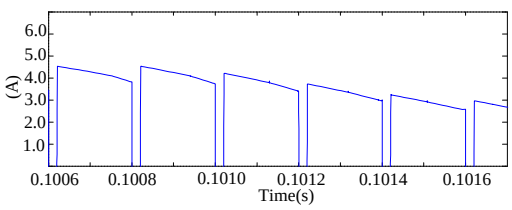
(b)



(b)



(d)



(e)

Fig.10. Simulation results of TL-ZSMR

VI. EXPERIMENTAL RESULTS

The same parameters are chosen to construct a testing hardware circuit according to the simulations. The switching frequency is 5 kHz. The switch devices are 1MBH60D-100 and the drive circuit, DA962D6, can independently drive six IGBTs at the same time. The switch turn-on time is about 0.3us, and the turn-off time is about 0.85us. The commutation delays are less than or equal to 1.15us, the addition both turn-off time and turn-on time. The core material of ZSMR utilizes H5C2 and the number of turns is 21. The core material of SL-ZSMR also utilizes H5C2 and the number of turns is 14. The core material of TL-ZSMR is PC40. The primary turn number is 18 and the secondary turn number is 36. The average dc accuracy of the oscilloscope is about +/-3%. The modulation scheme and control strategy are implemented in a high-performance DSP (TMSF320F2812). Fig.11, Fig.12 and Fig.13 correspond to the experiment results for the ZSMR, SL-ZSMR and TL-ZSMR, respectively. From Fig.11, Fig.12 and Fig.13, it can be seen that the experimental results are consistent with the simulation results. The capacitor voltage values and the output voltage values for the ZSMR, SLZSMR and TLZSMR are listed in Table III. The capacitor voltage value for ZSMR is about 25.9V close to the theoretical value $V_C = \frac{1-D}{1-2D} \times V_{eq} = \frac{0.9}{0.8} \times 24 = 27V$, and the output voltage value is about 25.3V. So, the corresponding voltage transfer ratio is $G_z = \frac{V_{dc}}{\sqrt{3}V_{im}} = 0.730$, which is 0.049 less than that of the simulation because of IGBT device voltage drop.

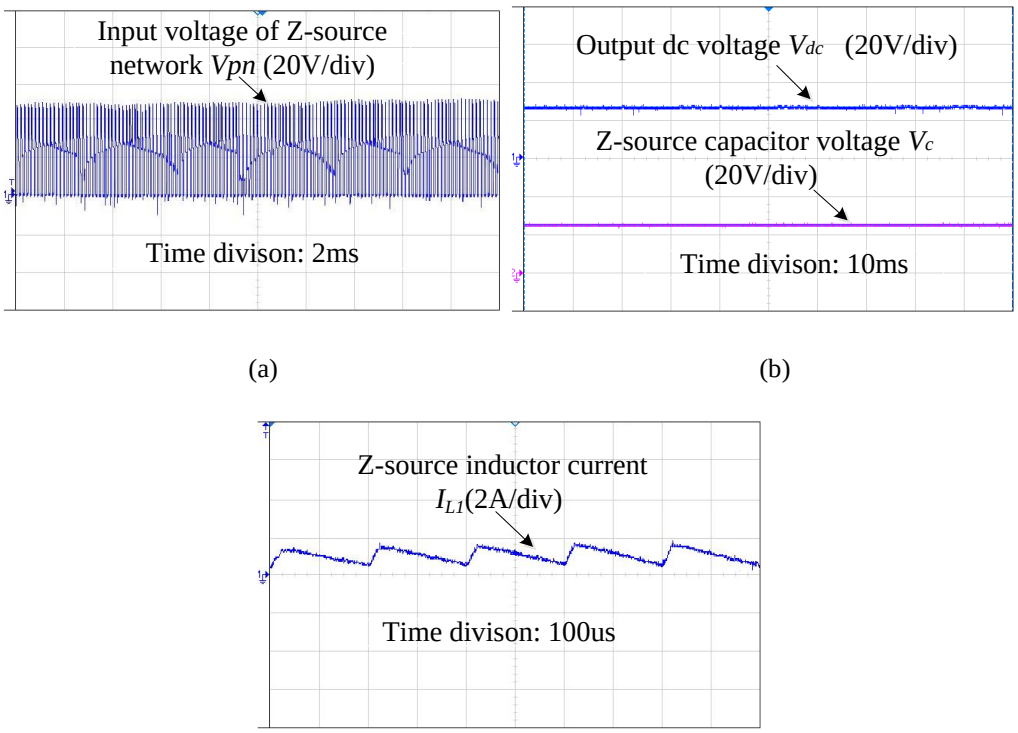


Fig.11. Experiment results of ZSMR

TABLE III

	ZSMR	SLZSMR	TLZSMR(N=2)
V_C	25.8V	28.9V	34.8V
V_{dc}	25.8V	31.9V	42.1V

Fig.12 shows the Z-source input voltage for SL-ZSMR, whose magnitude is higher than the ZSMR. From the Table III, it can be seen the capacitor voltage for the SL-ZSMR is about 28.9V close to the theoretical value $V_C = \frac{1-D}{1-3D} V_{eq} = \frac{1-0.1}{1-3\times 0.1} \times 24 = 30.85V$. The output voltage is about 31.9V close to the theoretical value $V_{dc} = \frac{1-D^2}{1-3D} V_{eq} = \frac{1-0.1^2}{1-3\times 0.1} \times 24 = 33.94V$, which is higher 6.6V than for the ZSMR using the same D. Due to IGBT power tube voltage drop there, and three-phase input voltage is not very symmetrical, the actual output voltage to be slightly smaller, but little impact. Therefore, the SLZSMR has a better voltage transfer ratio (0.92).

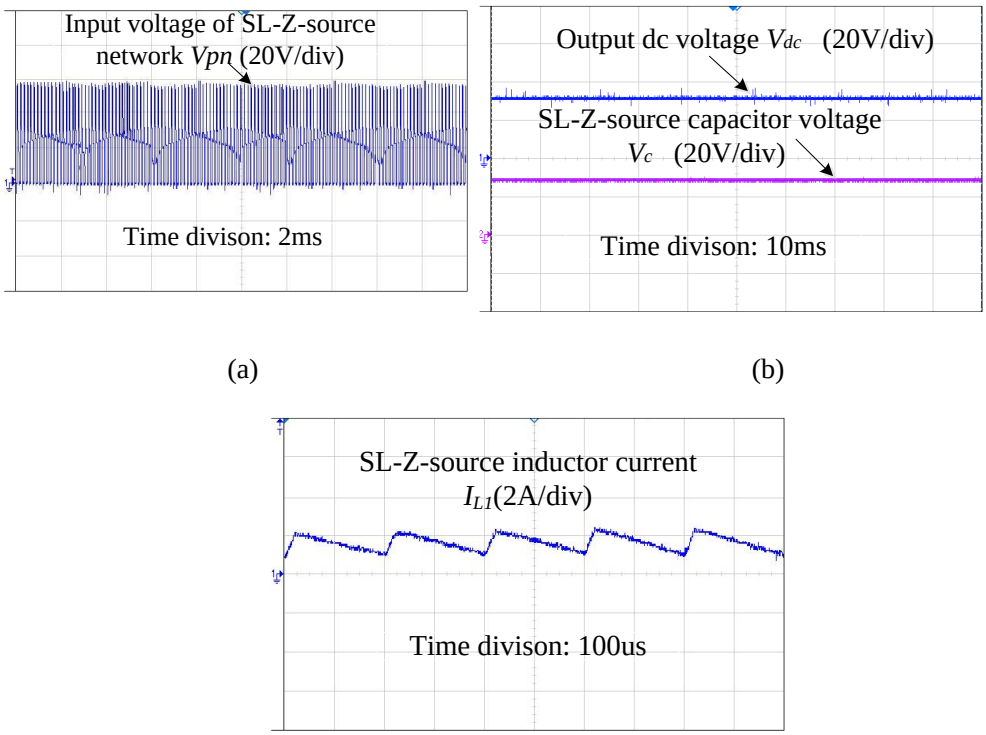


Fig.12. Experiment results of SL-ZSMR

The experiment results for the TL-ZSMR are shown in Fig.13, which includes the Z-source input voltage, output voltage, capacitor voltage and the tapped-inductor current. It can be seen that the capacitor voltage is about 34.8V close to the theoretical value $V_C = \frac{1-D}{1-4D} V_{eq} = \frac{1-0.1}{1-4\times 0.1} \times 24 = 36V$. The output voltage is about 42.1V close to the theoretical value $V_{dc} = \frac{(1+2D)(1-D)}{1-4D} V_{eq} = \frac{(1+2\times 0.1)(1-0.1)}{1-4\times 0.1} \times 24 = 43.2V$, which is higher 16.8V than for the ZSMR with the same D. The corresponding voltage transfer ratio is 1.21. Obviously, the voltage-boost ability of the TLZSMR is the highest of the three circuits. Based on the simulation and experiment results, the validity and advantages of the proposed rectifiers have been proven to be a good agreement with the theoretical analysis results.

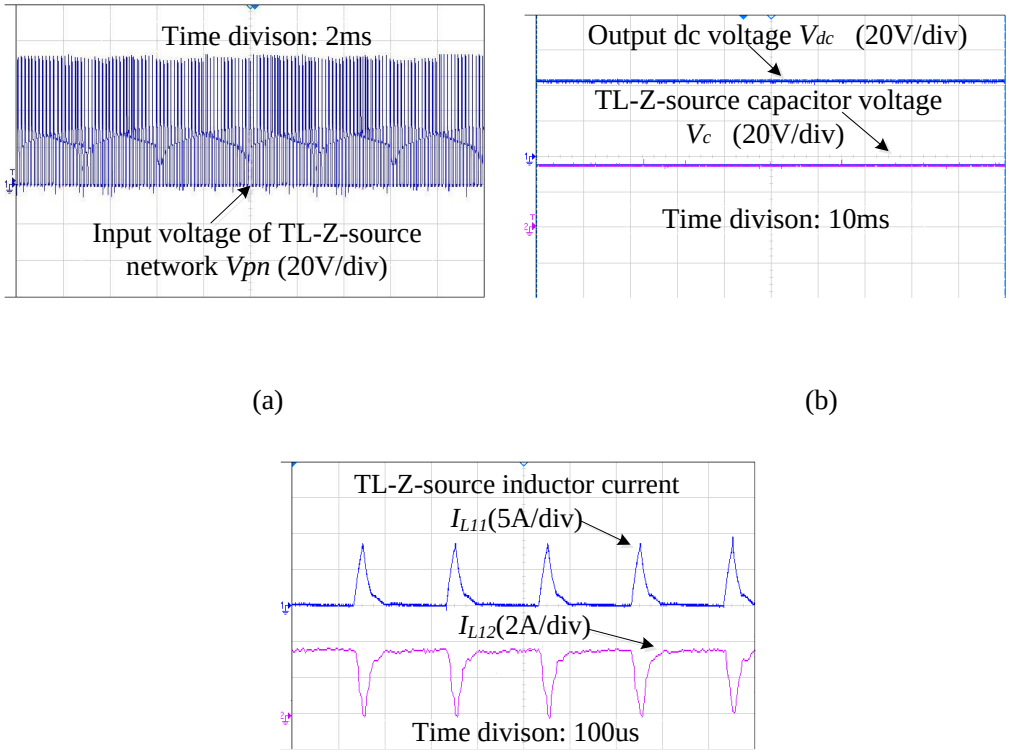


Fig.13. Experiment results of TL-ZSMR

VII CONCLUSION

This paper has presented a novel Z-source matrix rectifier by combining a matrix rectifier and three Z-source networks. The proposed rectifiers introduce a modified modulation strategy by taking an open-circuit zero state into the traditional zero states to overcome a voltage-boost drawback in traditional matrix rectifier. And the new increased Z-source network also serves as energy storage and guarantees double filtration grade at the output of the rectifier. Finally, the validity of the three topologies considered and the modified modulation strategies for the proposed ZSMR, SL-ZSMR and TL-ZSMR circuits is verified using both the simulation and experiment results.

REFERENCES

[1] Lozano-Garcia, J. M., Ramirez, J. M.: ‘Voltage compensator based on a direct matrix converter without energy storage’, IET Power Electron., 2015, 8, (3), pp. 321-332.

[2] Huber L, Borojevic D. Space vector modulated three-phase to three-phase matrix converter with input power factor correction[J]. Industry Applications, IEEE Transactions on, 1995, 31(6): 1234-1246.

[3] Ortega, M., Jurado, F., Carpio, J.: ‘Control of indirect matrix converter with bidirectional output stage for micro-turbine’, IET Power Electron., 2012, 5, (6), pp. 659-668

[4] R. Cárdenas, R. Peña, R. Peña, and J. Clare, “Experimental validation of a space vector modulation algorithm for four-leg matrix converters,” IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1282-1293, Apr. 2011.

[5] Jahan, H. K., Banaei, M. R.: ‘Implementation of a stepped down frequency eight switches matrix converter suitable for microturbine generation’, IET Power Electron., 2014, 7, (5), pp. 1092-1098

[6] M. Hamouda, H. F. Blanchette, K. Al-Haddad, and F. Fnaiech, “An efficient DSP-FPGA-based real-time implementation method of SVM algorithms for an indirect matrix converter,” IEEE Trans. Ind. Electron., vol. 58, no. 11, pp. 5024–5031, Nov. 2011.

[7] Shi, T., Huang, Q., Yan, Y., Xia, C.: ‘Suppression of common mode voltage for matrix converter based on improved double line voltage synthesis strategy’, IET Power Electron., 2014, 7, (6), pp. 1384-1395

[8] Rivera, M., Rojas, C., Rodriguez, J., Espinoza, J.: ‘Methods of source current

reference generation for predictive control in a direct matrix converter', IET Power Electron., 2013, 6, (5), pp. 894-901

[9] Rajendran, S., Govindarajan, U., Parvathi Sankar, D.S.: 'Active and reactive power regulation in grid connected wind energy systems with permanent magnet synchronous generator and matrix converter', IET Power Electron., 2013, 7, (3), pp. 591-603

[10] S. Khwan-on, L. De Lillo, L. Empringham, P. Wheeler, and C. Gerada, "Fault-tolerant, matrix converter, permanent magnet synchronous motor drive for open-circuit failures," IET Electric Power Appl., vol. 5, no. 8, pp. 654-667, 2011.

[11] X. Liu, P. C. Loh, P. Wang, and X. Han, "Improved modulation schemes for indirect Z-source matrix converter with sinusoidal input and output waveforms," IEEE Trans. Power Electron., vol. 27, no. 9, pp. 4039–4050,Sep. 2012.

[12] S. Khwan-on, L. De Lillo, L. Empringham, P. Wheeler, and C. Gerada, " A Quasi-Z-Source Direct Matrix Converter Feeding a Vector Controlled Induction Motor Drive," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 2, pp. 339-348, 2015.

[13] E. Karaman, M. Farasat, and A. M. Trzynadlowski, "Permanent-magnet synchronous-generator wind-energy systems with boost matrix converters," in Proc. Energy Convers. Congr. Exposit. (ECCE), 2013, pp. 2977-2981.

[14] S. Lei, X. Haiping, L. Dongxu, Y. Zengquan, "A novel high power factor PWM rectifier inverter for electric vehicle charging station," in Proc. IEEE Int. Conf. Elect. Machines and Systems, Beijing, China, pp. 1-6, Aug. 2011.

[15] K. You and M. F. Rahman, "A matrix-Z-source converter with ac-dc

bidirectional power flow for an integrated starter alternator system," *IEEE Trans. Ind. Appl.*, vol. 45, no. 1, pp. 239-248, Jan./Feb. 2009.

[16] Keping You, M. F. Rahman; " Analytical Comparison of Conduction and Switching Losses of A Novel Matrix-Z-Source Converter and A Conventional VSI Converter for Automotive ISA 42 V System ",PESC2006, the 37th IEEE Powver Electronics Specialists Conference, June 18 to 22, 2006, Jeju, Korea.

[17] You Keping and Rahman M.F., "Analysis of conduction and switching losses of a matrix-Z-source converter," the 7th International Conference on Power Electronics, pp. 1071-1076, 2007.

[18] You Keping and Rahman M.F., "A matrix-Z-source converter for automotive integrated starter alternator system," Proc. IEEE Applied Power Electronics Conference and Exposition, pp. 273-279, 2008.

[19] F.Z. Peng, "Z-source inverter," in Proc. IEEE-IAS Annu. Meeting, 2002, pp. 775-781. March/April 2003.

[20] M. Zhu, K. Yu, and F. L. Luo, "Switched inductor Z-source inverter," IEEE Trans. Power Electron., vol. 25, no. 8, pp. 2150–2158, Aug. 2010.

[21] Soon, J. J., Low, K. S.: 'Sigma-Z-source inverters', IET Power Electron., 2015, 8, (5), pp. 715-723

[22] Ahmed, T., Mekhilef, S.: 'Semi-Z-source inverter topology for grid-connected photovoltaic system', IET Power Electron., 2015, 8, (1), pp. 63-75.

[23] Mo, W., Loh, P. C., Blaabjerg, F., Wang, P.: 'Trans-Z-source and Γ-Z-source neutral-point-clampedinverters', IET Power Electron., 2015, 8, (3), pp. 371-377

[24] Nguyen, M. K., Lim, Y. C., Park, S. J., Shin, D. S.: ‘Family of high-boost Z-source inverters with combined switched-inductor and transformer cells’, IET Power Electron., 2013, 6, (6), pp. 1175-1187

[25] M. Zhu, D. Li, P. C. Loh, and F. Blaabjerg, “Tapped-inductor Z-source inverters with enhanced voltage boost inversion abilities,” in Proc. IEEEICSET, Dec. 2010, pp. 1-6.

[26] S. Zhang, K. J. Tseng, and T. D. Nguyen, “Novel three-phase AC-DC-AC Z-source converter using matrix converter theory,” in Proc. Energy Convers. Congr. Exposit. (ECCE), 2009, pp. 3036–3070.