Short-circuit fault analysis and isolation strategy for matrix converters

WANG Li-na(王莉娜)[1], L. De Lillo[2], C. Brunson[2], L. Empringham[2], P. Wheeler [2],

1. School of Automation science and Electrical Engineering, Beihang University, Beijing, 100191, China
2. Department of Electrical and Electronic Engineering, The University of Nottingham, Nottingham, NG7 2RD, UK

Abstract: The behavior of Matrix Converter (MC) drive systems under the condition of MC short-circuit faults is comprehensively investigated. Two isolation strategies using semiconductors and high speed fuses (HSFs) for MC short-circuit faults are examined and their performances are compared. The behavior of MC drive systems during the fuse action time under different operating conditions is explored. The feasibility of fault-tolerant operation during the fuse action time is also studied. The basic selection laws for the HSFs and the requirements for the passive components of the MC drive system from the point view of short-circuit faults are also discussed. Simulation results are used to demonstrate the feasibility of the proposed isolation strategies.

Index Terms: matrix converter; short-circuit fault; fault analysis; fault behavior; fault isolation

1 INTRODUCTION

Although conventional voltage source converters based on AC-DC-AC structures have been well developed, the bulky and limited life-time dc-link capacitors can be a negative factor in some AC drive applications, especially in aerospace and military electric vehicle applications where space and weight, as well as high-temperature operation, are critical issues. In recent years Matrix Converters (MC's) have been increasingly attractive for these application areas[1-2].

In aerospace applications, good reliability is of great importance and continuous operation after faults can be one of the key points. Faults in motor drive systems include faults in motors, in power sources and in power converter components. All will affect the normal operation of motor drive systems. However the faults in the power converter is the focus of this paper.

A number of studies have been undertaken to deal with open-circuit faults in MCs. Several effective methods to manage open-circuit faults have been proposed[3-11]. However, very few papers consider MC short-circuit faults. In the literature, a couple of papers just briefly say that the protection mechanisms should be actuated to safely stop the system under short-circuit faults in MC switches[12-13]. No papers consider the behavior of MC motor drive systems under switch short-circuit faults.

Papers [14] and [15] describe the short-circuit fault isolation strategies and fault-tolerant operation for MC. In [14], three bidirectional switches, which connect the load input terminals to the supply neutral, and three fast acting fuses, which are connected in series with each of the MC output terminals, are used. In this method, once a shorted-switch fault is detected, all the gate signals for the faulty MC phase will be turned off. At the same time the connecting switch to the faulty phase is turned on to blow the corresponding fuse. The faulty MC phase is then isolated from the motor. The connecting switch continuously conducts during the post-shorted failure operation. In [15], in order to get rid of the need for the supply neutral, line-to-line input voltages are used to blow the fuses, at the expense of adding six TRIACs and six fast-acting fuses. After the right fuse is blown, the fourth leg replaces the faulty leg. Then the reconfigured MC is operated as a healthy full MC. However, since two fuses are used in the isolation circuit, a disaster may be induced if the wrong fuse blows first. The selection rules for the fuses and the method to solve this problem are not mentioned. Furthermore, papers [14] and [15] did not tell what should be done to secure the safety of the drive system during the fuse action time. The I^2t values of fuses are usually larger than those of IGBTs at the same ratings. Overcurrent and overvoltage stresses on both faulty and healthy devices can be caused by uncontrollable shorted circuit during the fuse action time. It is therefore important to understand the post-fault operation of the converter during the period before the fuses are blown.

This paper starts with the presentation of comprehensive analyses of the short-circuit faults in MC drive systems. Then two short-circuit fault isolation strategies are described. Their isolation performance is analyzed and compared. The behavior and characteristics of a MC-PMSM drive system during the fuse action time are explored. The feasibility of fault-tolerant operation during the fuse action time is also considered. The basic selection laws for HSFs and the requirements for the passive components of a MC drive system from the point view of short-circuit faults are summarized. The effects and the feasibility of the proposed isolation strategy are then verified, stressing the practical aspects in a typical MC-PMSM drive system. However, detection of short-circuit faults is not the focus of this paper, it assumes that the device short-circuit fault is accurately detected and located by a fault diagnosis technique described in another of our papers.

Foundation Item: Project (No.50807002) supported by National Natural Science Foundation of China, Project (SKLD10KM05) supported by State Key Lab. of Power System, Project(No.201206025007) supported by the State Scholarship Fund.
Received date: 2014-08-01, **Accepted date:** 2014-12-17
Corresponding author: (WANG Li-na, Associate professor, PhD, 86-010-82317304, wangln@buaa.edu.cn)

2 OPERATION OF THREE-PHASE MCs UNDER NORMAL CONDITIONS

A typical three-phase MC-PMSM drive system is shown in Fig.1. The input filter in the figuration, merged with the impedance of the source, is used to attenuate the high frequency switching harmonics in the input currents. The clamp circuit protects the power switches from overvoltage that occurs during transients and provides a current path under faulty operations. The bidirectional switch in MC is the common-emitter configuration of an anti-series connection of two standard insulated-gate bipolar transistors (IGBTs) with anti-parallel diodes.

Due to lack of space, this paper focuses on faults in IGBTs. Several types of faults can appear in these IGBTs. They can be broadly categorized as open-circuit faults, short-circuit faults, and intermittent gate-misfiring faults[16-17]. This paper will focus on short-circuit faults.

For the case of a short-circuit fault in an MC, we may have a short circuit in only one of those IGBTs (faults F1 and F2 in Fig.1) or a short circuit in both IGBTs of the same bidirectional switch (fault F3). The superscript 'F' in Fig.1 denoting 'forward' refers to current flowing from the supply side to the load side, while the superscript 'R' denoting 'reverse' refers to the opposite direction.

For the sake of completeness of this paper and for an easy understanding of the faulty operation of an MC, the basic mathematical relations that rule the normal operation of an MC will be presented first, proceeding afterward to the analysis of the operation of the MC with a short-circuit fault.

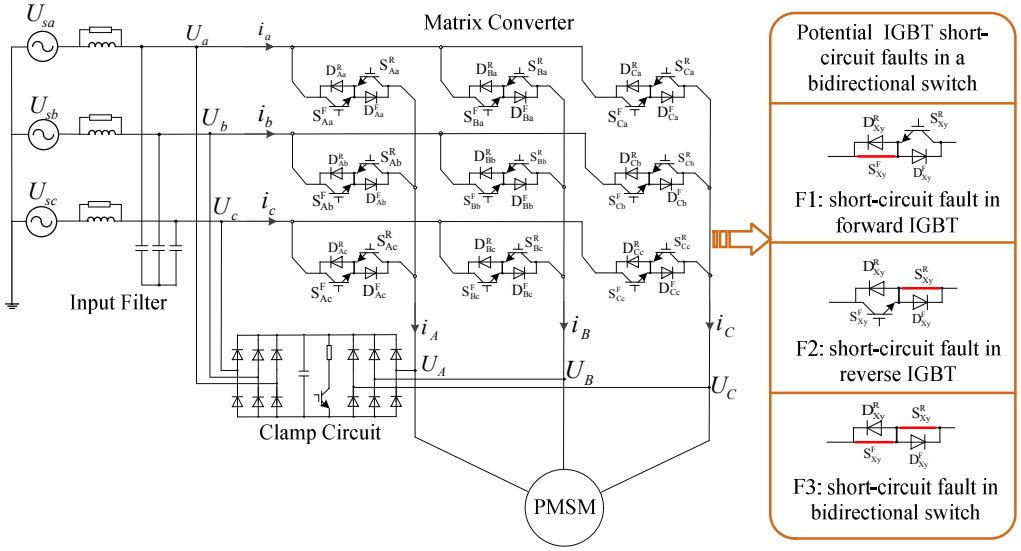


Fig.1 Configuration of MC-PMSM drive system and potential types of IGBT short-circuit fault

In normal condition, each output phase of the converter can be connected to any input phase voltage for a period of time, depending on which switch is turned on. Therefore, the output voltages of the MC can be expressed in terms of the input voltages and the switching states of the nine bidirectional switches, as given in (1).

$$\begin{bmatrix} U_A \\ U_B \\ U_C \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} \quad (1)$$

where U_A, U_B, U_C and U_a, U_b, U_c are the output and input voltages respectively. $S_{jk}(j = A,B,C \text{ and } k = a,b,c)$ represents the switching state of each bidirectional switch connected between the input phase 'k' and the output phase 'j' of MC. Note that S_{jk} is defined as '1' or '0' when the switch is turned on or turned off, respectively.

Likewise, the input currents (after the input filter of converter) can be estimated by

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \quad (2)$$

where i_A, i_B, i_C and i_a, i_b, i_c are the output and input currents respectively.

Since the MC is supplied by a voltage source, the input phases must never be shorted, and due to the inductive nature of the motor, the output phases must not be left open. This basic operating principle of the converter can be expressed as in (3).

$$S_{ja} + S_{jb} + S_{jc} = 1 \quad (3)$$

In order to get the switching state of each bidirectional switch, different modulation strategies have been proposed. Among the most popular modulation schemes are the Optimum AV (OAV) method, the SVM method and the carrier-based PWM method. Due to the lack of space and for simplicity of analysis, only the investigated knowledge based on the SVM method is presented in this paper.

3 OPERATION OF THREE-PHASE MCs UNDE R FAULTY CONDITIONS

Equations (1)-(3) are valid as long as all switches of the MC do not experience any fault. When a fault appears in MC, those relations do not remain valid.

To better understand the effect of a single switch shorted fault, the supply voltages are divided into six intervals as shown in Fig.2. And assume the following conditions as an example.

1) A short-circuit fault occurs in the forward switch S^F_{Aa}.
2) Neglect the threshold voltage requirement of the diodes.
3) Suppose the voltages U_a, U_b, U_c at the input terminals of the MC are sampled as the input voltages for SVM calculation.

3.1 Short-circuit Faults (F1 and F2 Types)

Since the analysis of the MC behavior under F1 and F2 faulty conditions is similar, F1 Type fault is taken as an example.

3.1.1 The phase angle of the supply voltages presently locates in intervals 1-2.

During intervals 1-2, U_{sa} has the largest value among three supply voltages. No matter S^R_{Ab} or S^R_{Ac} turns on, the short circuit between two input voltages will be created, in spite of the current direction of the load. Consider the case that S^R_{Ab} is turned on. Normally, S^F_{Aa} should have been turned off before S^R_{Ab} is on. Unfortunately, S^F_{Aa} is suffering a short-circuit fault, so normal control action leads to a short circuit between U_a and U_b. High current circulating in S^F_{Aa}-D^F_{Aa}-S^R_{Ab}-D^R_{Ab} will happen.

The high current has two main sources: 1) the discharging current of the capacitors of the input filter, as shown in Fig. 3(A). 2) the short-circuit current between two supply voltages, as shown in Fig. 3(B).

The first source only lasts a very short time. But it can arouse a very large surge current limited only by the impedance of two capacitors, two diodes and one IGBT. And its discharging time is decided by the voltages and capacitance of two filter capacitors and the resistance in the circuit. In order to prevent damages caused by this surge current, capacitors with low capacitance is preferable for the input filter. And the components involved in these short circuits should be designed to endure these surge currents.

The second source also leads to a very large current limited mainly by the impedances of the series part of the input filter, which are generally very low in order to get a small voltage loss. Comparatively, the current caused by the first source is much higher than that by the second source.

As a consequence of the short circuit between two input voltages, both U_a and U_b deviate from its normal values towards $(U_{sa}+U_{sb})/2$. The output voltages of the two healthy phases will also be affected if they are commanded to connect with the input phase *a* or *b*. The result is the distortions of the load voltages and currents, as shown in Fig.4(E) during intervals 1-2. Fig.4 shows the behavior of an open-loop controlled MC-RL system under the condition of short-circuit failure of S^F_{Aa}. For comparison, Fig.4 also displays the behavior of the MC-RL system during other intervals.

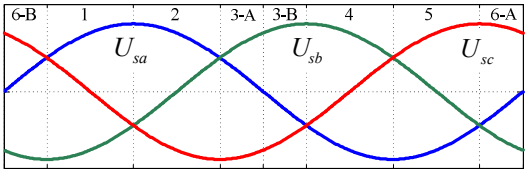
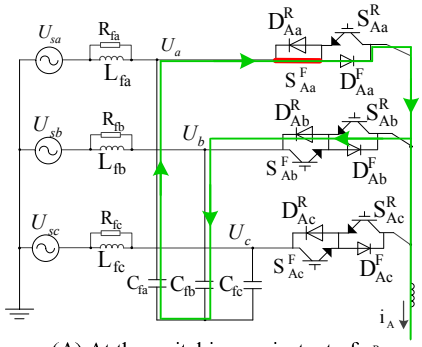
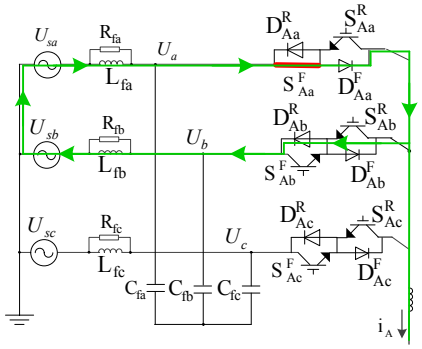


Fig.2 Interval division of the supply voltages



(A) At the switching-on instant of S^R_{Ab}



(B)After the energies stored in C_{fa} and C_{fb} are released

Fig.3 Two sources of the short circuit current under short-circuit fault in S^F_{Aa}

If S_{Ab} keeps being on during the next switching state, the effects caused by the second high current source will continue. As for the first high current source, whether it continues or not depends on whether U_a and U_b equal to each other.

If S_{Ac} is turned on during the next switching state, the same situations will happen to the input phases *a* and *c* like the aforementioned situations happen to the input phases *a* and *b*.

However, if S_{Aa} is turned on during the next switching state, the short circuit at the input side will be broken. The abrupt interruption of the high short-circuit current will cause high induced voltage across the series inductors. This results in overvoltage both at the input side and at the output side, as shown in Fig.4(B).

Small resistors in parallel with the input filter inductors help to suppress the overvoltage. But small resistors will

decrease the filtering effect. From this sense, the filter inductors with a small inductance again are preferable aside from the consideration of a small voltage loss on the input filter. Compare the simulation results in Fig.4 and Fig.5 with a 63uH and 630uH input filter inductor respectively. It can be seen that the situation of overvoltage at the MC input side and overcurrent of the motor are much better with a smaller input filter inductor.

Of course, the overvoltage will be finally clamped by the clamp circuit. But, if the above situation is not stopped in time, the rise of the clamp capacitor voltage will be inevitable because of the extremely high short-circuit currents, as shown in Fig.4(D) and Fig.5(D). Since the discharging time constant of the clamp capacitor is generally limited, over-rise of the clamp capacitor voltage will finally invalidate the overvoltage protection function of the clamp circuit and put the components at the risk of overvoltage damage.

Load currents will inevitably be affected by the overvoltage, as shown in Fig.4(E) and Fig.5(E), that are most likely to actuate the protection mechanisms to safely stop the system.

In conclusion, during intervals 1-2, under the condition of a short-circuit fault in S^F_{Aa}, high short-circuit currents and overvoltage at the input side, overcurrent and overvoltage at the output side, violent oscillations of the motor torque, severe vibration of the motor speed will be caused if the MC drive system is controlled without variation. If closed-loop motor control methods are used, the situations will get even worse.

Fig.6 shows the behavior of a closed-loop controlled MC-PMSM drive system under the condition of short-circuit failure of S^F_{Aa}. It can be seen that the overvoltage and overcurrent at the input side, the overvoltage of the clamp capacitor and the motor operation are all get worse than the case of a RL load. So, in

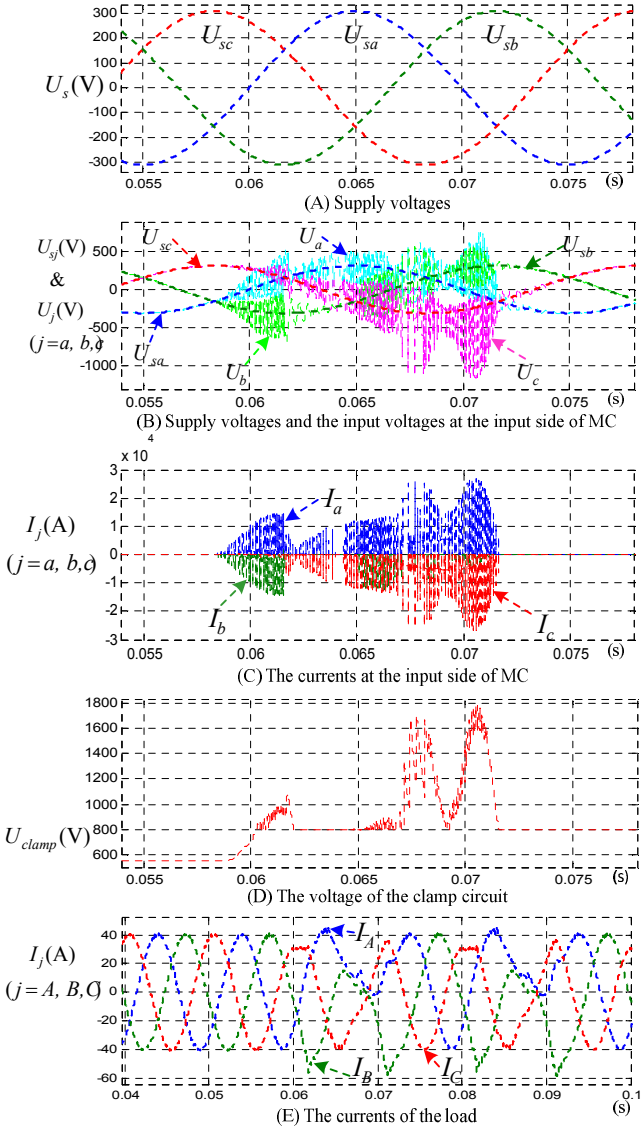


Fig.4 Fault behavior under the case of shorted S^F_{Aa} with an open-loop controlled RL load, f_{out}=100Hz, input filter parameters: L_f=63uH, C_f=60uF, R_f=10Ω

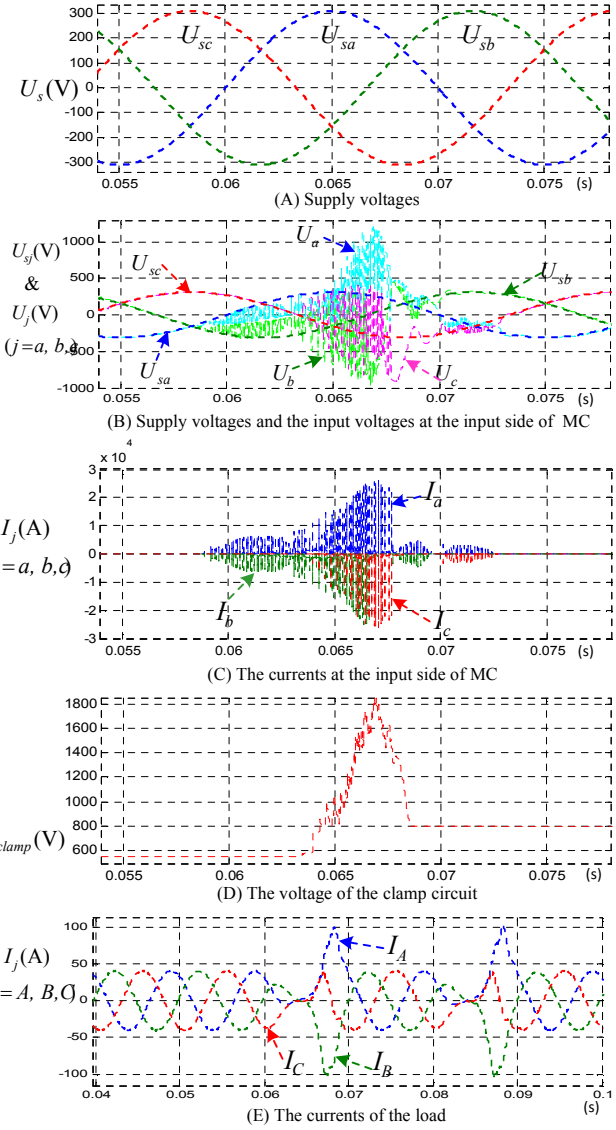


Fig.5 Fault behavior under the case of shorted S^F_{Aa} with an open-loop controlled RL load, f_{out}=100Hz, input filter parameters: L_f=630uH, C_f=60uF, R_f=10Ω

the analysis behind, intervals 1-2 are called '*severe intervals*' of the witch S^F_{Aa}. Likewise, the '*severe intervals*' of other switches are listed in Table 1 denoted by '××'.

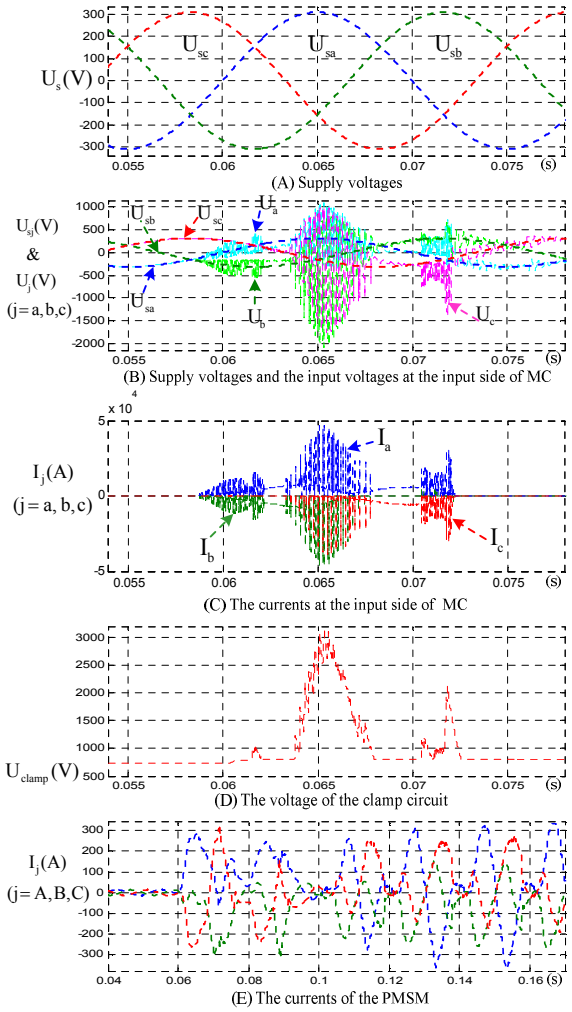


Fig.6 Fault behavior under the case of shorted S^F_{Aa} with a closed-loop controlled PMSM load, input filter parameters:L_f=63uH, C_f=60uF, R_f=10Ω

Table 1 Interval types under a single short-circuit faulty switch

Interval		1	2	3	4	5	6
Forward Switches (j=A, B, C)	S^F_{ja}	××	××	×	o	o	×
	S^F_{jb}	o	×	××	××	×	o
	S^F_{jc}	×	o	o	×	××	××
Reverse Switches (j=A, B, C)	S^R_{ja}	o	o	×	××	××	×
	S^R_{jb}	××	×	o	o	×	××
	S^R_{jc}	×	××	××	×	o	o

Annotation: (1) '××' denotes *severe interval*, (2)'×' denotes *less severe interval*, (3) 'o' denotes *safe interval*.

From the above analysis, it can be concluded that, once a short-circuit fault is detected in the '*severe intervals*', the first thing should be done is to prevent the formation of short circuits at the input side to avoid damages caused by huge short-circuit currents and its byproduct overvoltage. The often used method is to turn off the gate signals of all the IGBTs in the faulty MC phase immediately. However, since the output phase and the input phase has a fixed connection by the faulty IGBT, an uncontrollable situation can be induced during the '*severe intervals*' if the faulty switch is not cleared from the circuit. For example, the output phase-*A* has a fixed and uncontrollable connection with the input phase-*a* by the faulty S^F_{Aa} during intervals 1-2. This condition makes the motor phase-*A* have the highest voltage during intervals 1-2. It results that a non-negative phase-*A* current will be generated no matter what the voltages of the other two motor phases and the motor neutral point are. It will put the PMSM drive system in an uncontrollable and dangerous operation, especially under closed-loop control. The motor will run in a mess, let alone fault-tolerant operation. The best option is to isolate the faulty switch as soon as possible. This condition will be in effect for one third of the power supply cycle. For the power supply at 50Hz, it is 6.7ms.

3.1.2 The phase angle of supply voltages presently locates in intervals 4-5

During intervals 4-5, U_{sa} has the lowest value. No matter S_{Ab} or S_{Ac} is on or off, the short circuit between two input voltages is prevented by the reverse blocking capability of the diode D^F_{Aa} in series with the faulty S^F_{Aa}. So, if the short-circuit fault of S^F_{Aa} happens in these intervals, neither will high short circuit currents appear at the source side nor will the distortions happen to the load voltages and currents during these intervals, as shown in Fig.4-6. The motor can be controlled as normally. The reason of Fig.6(E) is the effect of abrupt acceleration and deceleration of the closed-loop controlled motor. So in the analysis behind, intervals 4-5 are called '*safe intervals*' of S^F_{Aa}. They also last one third of the power supply cycle. Likewise, the '*safe intervals*' of other switches are listed in Table 1 denoted by 'o'. In '*safe intervals*', since no malfunction characteristic is shown, fault detection will be delayed until supply voltage phase goes out of these intervals.

3.1.3 The phase angle of supply voltages presently locates in intervals 3,6

The common feature of intervals 3 and 6 is that U_{sa} has the medium value among three supply voltages. In interval 3, U_{sb} is larger than U_{sa} and U_{sa} is larger than U_{sc}, while in interval 6, U_{sc} is larger than U_{sa} and U_{sa} is larger than U_{sb}. Take interval 3 as an example for analysis. Similar behavior occurs in interval 6.

During the interval 3, when S^R_{Ab} is on, the short circuit between *a-b* input voltages is prevented by the reverse blockage of D^F_{Aa} and D^R_{Ab}. When S_{Aa} is on, there is no short circuits created either. However, when S^R_{Ac} is on, the short circuit between *a-c* input voltages will be created. Like the

situations in intervals 1-2, high short circuit currents will occur at the input side and distortions will appear on the load voltages and currents no matter the direction of the load current. If S^{R}_{Ac} keeps being on in the next switching state, the high short circuit currents at the input side and the distortions of the load voltages and currents will continue. If S_{Aa} or S_{Ab} is turned on during the next switching state, the short circuit at the input side will be broken. Again overvoltage will be incurred at the input and output sides of the MC and consequently the load current will be distorted. But the situations are less severe than the situations in intervals 1-2 because the value of U_{sa} is lower and overvoltage at the input side only occur in *a* and *c* phases in interval 3, as shown in Fig.4-6.

So, under the condition of a short-circuit fault in S^{F}_{Aa}, intervals 3 and 6 are called '*less severe intervals*' of S^{F}_{Aa}. They also last one third of the power supply cycle. Likewise, the '*less severe intervals*' of other switches are listed in Table 1 denoted by '×'.

For an AC motor load at high speed, the contradiction of the large back EMF of the motor and the low voltage output capability of the faulty MC phase makes the fault-tolerant operation very hard in '*less severe intervals*'. In order to avoid the formation of the short circuits at the input side, only two of three input voltages can be utilized to synthetize the output voltage of the faulty leg. For example, under the condition of a short-circuit fault in S^{F}_{Aa} during the interval 3, only U_a and U_b can be used to synthetize the output voltage U_A. So, during the interval 3-A, only positive voltage is available for U_A. And its amplitude range is very limited, especially during the beginning period of the interval 3-A. During the interval 3-B, the available voltage range of U_A becomes wider and a small negative value becomes available. But, compared with the normal condition, the available U_A voltage is still very limited until at the end of interval 3-B.

If the gate signals of all the IGBTs in the faulty MC leg are turned off immediately once a short-circuit fault is detected, the short-circuit currents at the input side and their bad effects on the whole MC drive system can be avoided. Again, since the output phase-*A* has an uncontrollable connection with the input phase-*a* by the faulty S^{F}_{Aa}, uncontrollable currents circulating in motor windings will be incurred if the back EMF of motor phase-*A* is different from the voltage U_a.

In conclusion, under the condition of F1 or F2 fault Types, fault-tolerant strategies can hardly be implemented without isolating the faulty switch from the circuit during '*severe intervals*' and '*less severe intervals*'. Only during '*safe intervals*' which only cover one third of the power supply cycle, operation can be continued without sacrificing the performance of the MC drive system. Under the case of a heavy load with small inertia, continued and less violent operation is nearly impossible. So in order to get sustainable and slightly milder fault-tolerant operation, the most important thing should be done is to clear the faulty switch from the circuit as soon as possible.

3.2 Short-circuit Faults (F3 Type)

This fault type combines the effects of F1 and F2 types. The '*severe intervals*' cover the summation of that of F1 and F2 types. And there're no '*safe intervals*' anymore. For example, intervals 1-2 and 4-5 are all '*severe intervals*' for S_{Aa}. The remaining intervals 3 and 6 are '*less severe intervals*'. That is to say two thirds of the power cycle is '*severe intervals*' and one third is '*less severe intervals*'.

According to the above theoretical analysis, fault-tolerant operation is infeasible with the faulty switch remaining in the circuit in '*severe intervals*'. In '*less severe intervals*', restricted by the limited safe switch combinations, the available voltage range of U_A is very limited. PMSM fault-tolerant operation at high speed is infeasible due to the contradiction of the large back EMF of the motor and the low voltage output capability of the faulty MC phase.

The conclusion is, for faults of F3 Type, fault-tolerant operation is not a practical way out. In next section, it indicates that the practical way is to stop the whole drive system and isolate the faulty bidirectional switch as soon as possible. Only after the faulty switch is isolated from the converter, fault-tolerant strategies can be considered.

4 SHORT-CIRCUIT ISOLATION METHOD

4.1 Traditional short-circuit fault isolation structure

The structure in Fig.7 was proposed in [14], which employs three connecting devices (T_A, T_B, T_C), which are TRIACs or back-to-back connected SCRs, and three HSFs (F_A, F_B and F_C). T_A, T_B and T_C are open and do not appear in the circuit in normal operating condition. In [14], it is only briefly said: once a single switch short-circuit fault is detected, the system controller automatically commands to open the other IGBTs in the faulty phase to avoid the short circuit of two supply voltages. The connecting device linked to the faulty phase is fired at the same time. As a result, the short circuit is constructed through the input voltage, the faulty switch, the fast-blow fuse and the connecting device. Therefore, the fuse blows and clears the phase with the faulty switch from the converter. The connecting device is forced to continuously conduct during the post-shorted failure operation. By regulating the output voltages and currents in the two remaining phases with the magnitude increased by $\sqrt{3}$ and the phase shifted by 30°away from the axis of the faulty phase, three-phase balanced sinusoidal output currents in the load motor can be generated.

However, paper [14] does not give clues about how to control the MC drive system and the behavior of the MC drive system during the fuse action time. Normally, only a few microseconds are needed to open IGBTs, while usually longer time are needed to break a HSF with the same ratings.

And IGBTs have much smaller I^2t values than HSFs and nearly have no overvoltage endurance capability. So, for the safety of the system, it is very necessary to investigate the behavior of the MC drive system during the action time of the HSF.

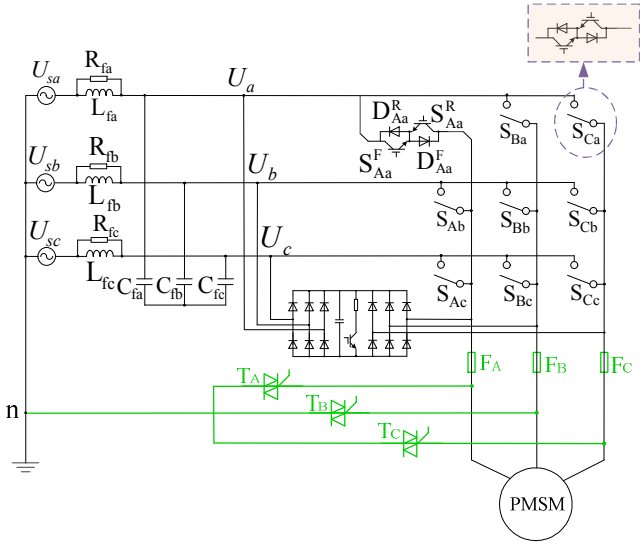


Fig.7 Traditional short-circuit fault isolation structure

Again consider the case that a short-circuit fault occurs in S^F_{Aa}. Assume S_{Ab} and S_{Ac} has been opened and T_A has been closed. As a result, during the positive half cycle of U_{sa}, there will be a high short-circuit current circulating in U_{sa}-R_{fa}//L_{fa}-S^F_{Aa}-D^F_{Aa}-F_A-T_A-n (supply neutral) to melt the fuse-link. Since under the unmelted status, the fuse resistance is very small (the resistance of a 200A fuse in size 30 is lower than $10^{-3}\Omega$). So is the connecting device T_A. Most of the supply voltage drops on the input filter inductor. The voltage U_a at the input terminal of the MC drops to a very small value, as shown in Fig.8(A). The operation of the two healthy MC phases will be affected inevitably. This condition is in effect during the entire positive half cycle of U_{sa}.

In practice, due to the filter inductor, the duration of this condition is extended to a time longer than the positive half cycle of U_{sa}. The extended duration is determined by the current amplitude and the ratio of the inductance by the resistance in the short circuit. Fig.8(A) shows a worst situation that the switch short-circuit fault happens at the beginning of the positive cycle of U_a. Nearly one fourth supply cycle is extended for the parameters listed in Table 2. The larger the filter inductance is, the worse the situation is.

Under the condition of a RL load, the modulation method used under normal condition should be revised to adapt to the severe imbalance of the input voltages. Traditional SVM method, traditional Venturini modulation method and traditional Direct Duty-ration PWM (DDPWM) are not applicable any more, since they intrinsically assume a balanced three-phase supply and a balanced three-phase output. Even though a viable modulation method based on instantaneous values could be found, the output capability of the MC is very limited due to the great voltage drop of U_a.

Under the condition of a motor load (PMSM or IM), large voltage difference between the motor back-EMF at high speed and the decreased MC output voltage capability will cause uncontrollable large motor currents. Fig.8 shows some results under the condition of a PMSM load with the application of the unchanged control and the traditional SVM method. In hundreds of microseconds, the motor currents rise to more than two times its rated current. The large currents will probably actuate the protection mechanisms to stop the system before the fuse blows. So the relatively safe way for motor load is turning off the whole MC by turning off all the gate-drive signals during the fuse action time. Fig.8 is just used to show the perceived behavior of the MC drive system during fuse action, assuming the fuse is under the unmelted status all the time.

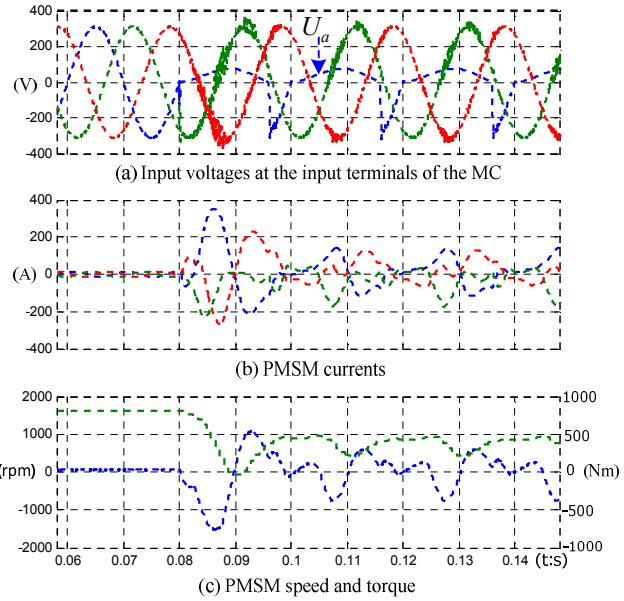


Fig.8 Perceived behavior of the MC-PMSM drive system when unchanged traditional SVM is used during fuse action period under the case of a shorted S^F_{Aa}, input filter parameters: L_f=63uH, C_f=60uF, R_f=1Ω

However, even if the drive system is completely shut off by turning off all the gate-drive signals during the fuse action time, large current circuiting in motor stator windings should also be paid attention to. Though the clamp circuit provides a free-wheeling path for motor currents, the kinetic energy stored in motor rotor can't be completely released immediately. So PMSM will act as a generator. Large current spikes, several times or even more than ten times the rated motor current, will occur due to the voltage difference between the back EMF and the voltage of the supply neutral point or DC-side voltage of the clamp circuit, as shown in Fig.9(B). Fortunately, the duration of the large current spikes is very short, a maximum of 15ms in the simulation. And they circulate in the motor windings, the clamp circuit and the connection device. At the design stage, these current spikes should be taken into consideration.

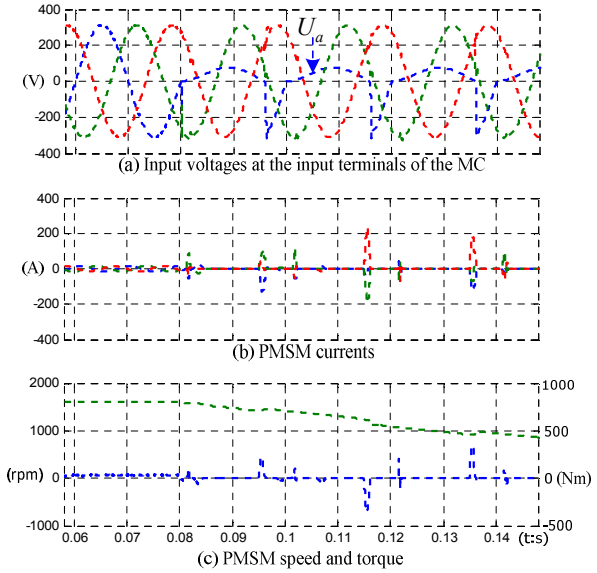


Fig.9 Perceived behavior of the MC-PMSM drive system when all the gate-drive signals are turned off during fuse action period under the case of a shorted S^F_{Aa}, input filter parameters: L_f=63uH, C_f=60uF, R_f=1Ω

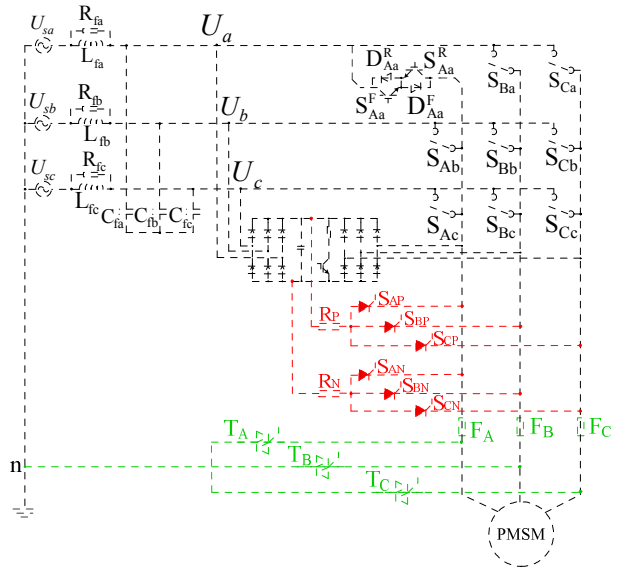


Fig.10 Proposed short-circuit fault isolation structure

At this point, a conclusion can be reached that, for the isolation structure in Fig.7, during the fuse action time, fault-tolerant operation is nearly infeasible for motor load. Unexpected large current may be caused by the back EMF of the motor at high speed and the decreased voltage output capability of the MC. Even if the whole MC is turned off, large current spike still remains a threat. Since motor speed is uncontrollable during this time, the back EMF of the motor is uncontrollable. Consequently, the large current spikes are uncontrollable. So the best way out is to turn off the whole MC and isolate the faulty switch as soon as possible. After the failure phase is cleared out from the main circuit, fault tolerant operation can be put into practice.

4.2 Proposed short-circuit fault isolation structure

In order to isolate the faulty switch immediately, a new structure for isolating short-circuit fault is proposed, as shown in Fig.10. Six SCRs and two resistors are added on the base of the structure in Fig.7. $S_{jp}(j=A,B,C)$ and R_p are used when a short-circuit fault locates in the forward switch S^F_{jk}, while $S_{jN}(j=A,B,C)$ and R_N are used when a short-circuit fault locates in the reverse switch S^R_{jk}.

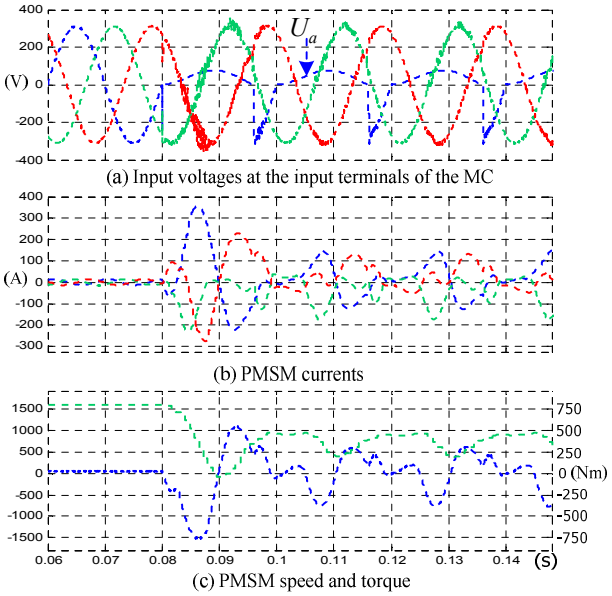
For example, once the short-circuit fault in S^F_{Aa} is detected, the system controller immediately commands to open S_{Ab} and S_{Ac} and turn on T_A and S_{Ap}. As a result of the above operation, high current will be induced in the fuse F_A. The high current has four main sources: 1) the discharging current of the capacitors of the clamp circuit. 2) the short-circuit current through U_{sa}-R_{fa}//L_{fa}-S^F_{Aa}-D^F_{Aa}-F_A-T_A-n (supply neutral). 3) the short-circuit current through U_{sb}-R_{fb}//L_{fb}-clamp circuit diode-R_P-S_{AP}-F_A-T_A-n. 4) the short-circuit current through U_{sc}-R_{fc}//L_{fc}-clamp circuit diode-R_P-S_{AP}-F_A-T_A-n.

Due to the four sources, there is always high current circulating in F_A during the whole power cycle until the fuse-link breaks, not like the case with the structure in Fig.7 that high current circulates only during the positive half cycle of U_a.

The first current source acts at the closing instant of S_{AP}. The second current source works through the faulty switch during the positive period of U_a. The third current source is ignited through the clamping-circuit diode and the switch S_{AP} during U_{sb} being the maximum value among three supply voltages. The fourth current source is activated through the clamping-circuit diode and the switch S_{AP} during U_{sc} being the maximum value among three supply voltages. And the first two current sources can act together with the other current sources.

The interaction result of the four main current sources is high currents incessantly circulate in F_A during the whole power cycle until the fuse-link breaks. Consequently, the fuse can be blown more quickly.

During the fuse action time, turning off the whole MC or executing the fault-tolerant operation strategy depends on the failure occurring time. During the positive period of U_a, U_{sa} provides the melting energy and the voltage U_a at the input side of the MC will also drop greatly like the situation of the structure in Fig.7. The operation of the other two phase-legs will also be inevitably affected. Fig.11 shows some simulation results of the structure in Fig.10 assuming that the switch short-circuit fault occurs at the beginning of the positive cycle of U_a and that the unchanged closed-loop PMSM control with traditional SVM is used during fuse action period.



(a) Input voltages at the input terminals of the MC

(b) PMSM currents

(c) PMSM speed and torque

Fig.11 Perceived behavior of the MC-PMSM drive system when unchanged traditional SVM is used during fuse action period under the case of a shorted S^F_{Aa}, input filter parameters: L_f=63uH, C_f=60uF, R_f=1Ω

Comparing Fig.11 with Fig.8, it can be seen that the voltages at the input side of MC and the motor behavior during the fuse action time is similar for two isolation structures.

However, the difference lies in the fuse current. The fuse current in Fig.7 only circulates during the positive period of U_a and its amplitude is decided by the amplitude of U_a. However, there is always high current circulating in the fuse of Fig.10 and always the maximum one works. The significance of this feature makes it possible that the short-circuit fault can been cleared from the system as soon as possible if the short-circuit fault occurs during the intervals 3-6.

So, for the isolation structure in Fig.10, if short-circuit faults occurs during the positive cycle of U_a, the best option still is turning off the whole MC during the fuse action time. After the faulty switch is cleared from the circuit, the fault-tolerant operation strategy is started to work.

However, if the failure occurs during the negative cycle of U_a, the fault-tolerant operation strategy stated in [14] can be triggered to work during the fuse action time. This feature is very conducive for the continuous motor operation and the stabilization of the motor torque and speed after switch faults. But care should be taken when this feature is utilized in practical applications. In high power applications, high power rating HSFs should be used, which need more melting energy. If HSFs can't be blown during the present negative cycle of U_a, the fault-tolerant operation strategy can't be used uninterruptedly during the fuse action time.

R_p and R_N are added to suppress large voltage drops on the input filter so that the fault-tolerant operation of the system can't be affected while using the other two supply voltages to melt the fuse. The values of R_p and R_N are set according to the impedance of the series part of the input filter at the power fundamental frequency in order for limiting the voltage loss caused by it. So the proposed isolation structure is more applicable to the MC drive system with a small input filter. Fortunately, only small input filter is needed for MC drive systems, which is one of its advantages over the traditional AC-DC-AC converters and back to back converters.

5 VERIFICATION RESULTS

The validity of the proposed isolation strategy was verified through the developed Matlab/Simulink model of a 14kW MC-PMSM drive system. The parameters are as shown in Table 2. An indirect SVM technique was adopted to control the MC, along with a four-step commutation strategy in the simulation model.

According to the parameters of the MC-PMSM drive system, 250V/50A Bussmann HSFs FWX50 are selected, the current rating of which is greater than the starting current of the motor and an allowance of around 15% is provided in order to avoid nuisance blowing. Though a fuse with a bit smaller rating is more eligible, FWX50 is selected without loss of generality. According to the datasheet, the pre-arcing I^2t of FWX50 is 100A^2s, while its clearing I^2t at 250V and at power factor of 15% is 520A^2s. For lower voltage or higher power factor, the clearing I^2t should be corrected by a correction factor less than 1. Here we use the clearing I^2t of 520 A^2s to estimate the needed clearing time conservatively. After checking, its arc voltage, current rating and breaking capacity all satisfy the requirement of the MC-PMSM drive system in Table 2. In the simulation, the fuse is modeled as a constant impedance with R_{fuse}=0.001Ω, L_{fuse}=10nH[18] without considering its current limiting effect.

Prior to the artificial short-circuit fault, the system is in steady state, with the speed regulated at 1600 r/min under a 75Nm load. At some instant, S^F_{Aa} is shorted by the program to produce the phenomenon of a short-switch fault. In order to compare the performance of two isolation structures, ten different triggering moments of the artificial short-circuit fault are set, as shown in Fig.12.

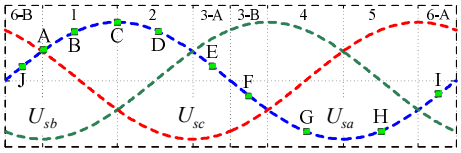


Fig.12 Artificial short-circuit fault triggering moments the traditional

The unrestricted currents circulating in the fuse of the two isolation structures are shown in Fig.13 and Fig.14, which doesn't consider the current limiting effect of the fuse and assumes the unmelted status of the fuse all the time. In fact, when fuse begins to melt, its resistance will rise. When the fuse is blown, it has infinite resistance in theory. So in fact,

the actual fuse current peak won't be so large and won't last so long as Fig.13 and Fig.14 shows. Fig.13 and Fig.14 are just used to show the effects of two isolation structures during different supply intervals. Fig.13 and Fig.14 again assume that the switch short-circuit fault happens at the beginning of the positive cycle of U_a. When the switch short-circuit fault happens at other moments, the waveform of the fuse current during the beginning phase will be different.

The time needed for fuse pre-arcing and clearing for the traditional isolation structure and the proposed isolation structure at different fault triggering moment is shown in Table 3.

From the simulation results, it can be seen that time needed for the proposed isolation structure is less than that for the traditional isolation structure in general. It is consistent with the previous theoretical analysis. Big difference between two isolation structures occurs in interval 3. For the traditional isolation structure, the

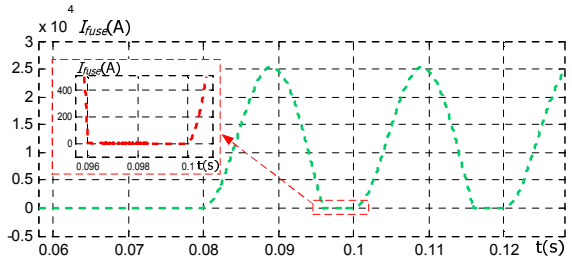


Fig.13 The perceived currents circulating in the fuse after isolation structure is put into force

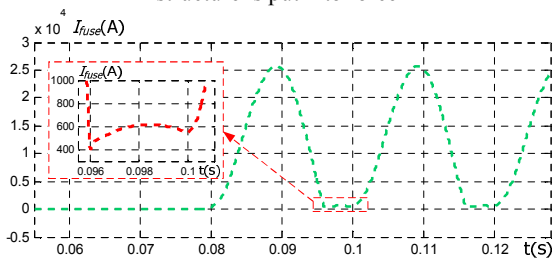


Fig.14 The perceived currents circulating in the fuse after the proposed isolation structure is put into force

Table 2 Parameters of a MC-PMSM system

parameter	value	parameter	value
Supply phase rms voltage U_s/(V)	220	Supply frequency (Hz)	50
Input filter inductance L_f/(uH)	63	Input filter capacitance C_f/(uF)	60
Input filter resistance R_f/(Ω)	10	Clamp circuit capacitance C/(uF)	150
Rated torque T_N/(N·m)	75	Rated current I_N/(A)	24.8
85ms starting current I_{st}/(A)	42.5	Rated speed *n*/(rpm)	1 700
Stator d–axis inductance L/(mH)	2.1	Stator q–axis inductance L/(mH)	2.1
Stator winding resistance R/(Ω)	0.331	Magnet fluxψ_f/(Wb)	0.353 7
Pole pairs p_n	4	Back EMF coefficient K_e/(r/min)	0.256 6
Rotor inertia J/(kg·m^2)	0.025 2	Friction coefficient B/(N·m·s)	0.000 1
Converter control frequency f_s/(Hz)	10k	Switch commutation dead time T_d/(μs)	0.1
Current sampling frequency /(Hz)	10k	Speed sampling frequency /(Hz)	1k
Cut frequency of current filter /(Hz)	5k	Time constant of speed filter/(ms)	1
Current-limiting resistance R_P/(Ω)	0.5	Current-limiting resistance R_N/(Ω)	0.5
Fuse rated current/(A)	63	Fuse rated voltage/(V)	240
Fuse pre-arcing I^{2}t @240V /(A^{2}s)	180	Fuse clearing I^{2}t @240V/(A^{2}s)	2200

Table 3 Time for the fuse pre-arcing and clearing at different fault triggering moment

Fault ocurring instant	Struction of the traditional isolation structure ---Fig.7		Struction of the proposed isolation structure ---Fig.10	
	Time for pre-arcing (ms)	Time for clearing (ms)	Time for pre-arcing (ms)	Time for clearing (ms)
A(at the beginning of '*severe intervals*')	0.27	0.51	0.20	0.45
B(in the middle of '*severe intervals*')	0.18	0.32	0.18	0.32
C(in the middle of '*severe intervals*')	0.21	0.36	0.21	0.36
D(in the middle of '*severe intervals*')	0.21	0.40	0.21	0.40
E(in '*less severe intervals*')	0.56	11.8	0.29	0.69
F(in '*less severe intervals*')	10.4	10.8	0.45	1.60
G(in' *safe intervals*')	5.4①+2.5	5.4①+2.9	5.4①+0.47	5.4①+1.6
H(in '*safe intervals*')	0.95①+2.5	0.95①+2.9	0.95①+0.47	0.95①+1.6
I(in '*less severe intervals*')	1.6	2.0	0.46	1.4
J(in '*less severe intervals*')	0.42	0.77	0.24	0.58

①delay time in fault detection.

accumulated energy during the present positive period of U_{sa} in interval 3-A is not enough to clear the fuse. So fuse clearing is delayed to next positive period of U_{sa}. In interval 3-B, the current path to melt the fuse is blocked by the reverse blocking capability of the diode in series with the faulty IGBT, so fuse clearing is also delayed to next positive period of U_{sa}. But for the proposed isolation structure, fuse is cleared instantly with the melting energy provided continually by the other two supply voltages.

In safe intervals 4-5, short circuit between two supply voltages is prevented by the reverse blocking capability of the diode in series with the faulty IGBT, no failure symptom is shown. So there is a time delay for the fault detection for both isolation structures. Fortunately, in '*safe intervals*', no dangerous situation will be induced. Once the fault is detected, time needed for the proposed isolation structure is again less than that for the traditional isolation structure. For the sake of the circuit safety and continued post-fault operation, the shorter the clearing time is, the better it is. In this respect, the isolation performance of the proposed isolation structure outweighs the traditional isolation structure.

Moreover, it can be seen from the simulation results that, for the proposed isolation structure with the motor system in Table 3, it is possible in most situation to isolate the short-circuit fault from the system before it enters into '*severe intervals*'. It's very important for the safety of the system and post-shorted failure operation.

The disadvantage of the proposed isolation structure is requirement of six more unidirectional switches. However, increase in hardware is over the evil affects caused by short-circuit faults. For higher power applications, the advantage of the proposed isolation structure will be weakened.

6 CONCLUSION

1) Comprehensive analyses of switch short-circuit faults in MC drive systems is presented. From the analysis of the effects of short-circuit faults, it is pointed out that fault-tolerant strategies can hardly be implemented without isolating the faulty switch from the circuit during '*severe intervals*' and '*less severe intervals*'.

2) Two isolation structures for MC switch short-circuit faults are investigated and their performances are examined. As for the shorter action time, smaller possibility of IGBT rupture, higher safety of the system, and higher possibility of post-fault continued operation, the new isolation structure proposed in this paper has the better performance than the traditional isolation structure.

3) The feasibility of fault-tolerant operation during the fuse action time is also studied. For the traditional isolation structure, fault-tolerant operation during the fuse action time is infeasible. For the proposed isolation structure, the feasibility of fault-tolerant operation during the fuse action time depends on fault occurring moments and the power ratings of the applications.

4) The basic selection laws for HSFs and the requirements for the passive components of MC drive systems from the point view of short-circuit faults are summarized.

5) Simulation results demonstrate the feasibility of the proposed isolation structure on the simulation platform of MC-PMSM drive system.

REFERENCES

[1] Huber L, Borojevic D. Space vector modulated three-phase to three-phase matrix converter with input power factor correction[J]. IEEE Trans. on Ind. Electron., 1995, 31(6): 1234-1245.

[2] Wheeler P, Rodriguez J, Clare J, Empringham L, Weinstein A. Matrix converters: a technology review[J]. IEEE Trans. on Ind. Electron., 2002,49(4): 276-288.

[3] Kwak S, Toliyat H A. An approach to fault-tolerant three-phase matrix converter drives[J]. IEEE Trans. on Energy Conversion, 2007.22:855-863.

[4] Kwak S. Fault-tolerant structure and modulation strategies with fault detection method for matrix converters[J]. IEEE Trans. on Ind. Electron., 2010, 25(5): 1201-1210.

[5] Kwak S. Four-leg-based fault-tolerant matrix converter schemes based on switching function and space vector methods[J]. IEEE Trans. on Ind. Electron., 2012, 59(1): 235-243.

[6] Cruz S M A, Ferreira M, Mendes A M S, Cardoso A J M. Analysis and diagnosis of open-circuit faults in matrix converters[J]. IEEE Trans. on Ind. Electron., 2011, 58(5): 1648-1661.

[7] Cruz S M A, Mendes A M S, Cardoso A J M. A new fault diagnosis method and a fault-tolerant switching strategy for matrix converters operating with optimum Alesina-Venturini modulation[J]. IEEE Trans. on Ind. Electron., 2012, 59(5): 269-280.

[8] Khwan-on S, De Lillo L, Empringham L, Wheeler P. Fault-tolerant matrix converter motor drives with fault detection of open switch faults[J]. IEEE Trans. on Ind. Electron., 2012, 59(1): 257-268.

[9] Potamianos P G, Mitronikas E D, Safacas A N. Open-circuit fault diagnosis for matrix converter drives and remedial operation using carrier-based modulation methods[J]. IEEE Trans. on Ind. Electron., 2014, 61(1): 531-545.

[10] Nguyen-Duy K, LIU T H, CHEN D F, HUNG J Y. Improvement of matrix converter drive reliability by online fault detection and a fault-tolerant switching strategy[J]. IEEE Trans. on Ind. Electron., 2012, 59(1): 244-256.

[11] Brunson C, De Lillo L, Empringham L, Wheeler P, Clare J. Fault location in matrix converters using low frequency modulation matrices for SVM based modulation techniques[C]. Proc. Rec. of IEEE IECON. Montreal, Canada: IEEE, 2012:6082-6087.

[12] ZHOU D N, SUN K, LIU Z C, HUANG L P, K. Matsuse, and K. Sasagawa. A novel driving and protection circuit for reverse-blocking IGBT used in matrix converter[J]. IEEE Trans. Ind. Appl., 2007, 43(1):3–13.

[13] Nielsen P, Blaabjerg F, Pedersen J K. New protection issues of a matrix converter: Design considerations for adjustable-speed drives[J]. IEEE Trans. Ind. Appl., 1999, 35(5):1150–1161.

[14] Kwak S, Toliya H A. Fault-tolerant topologies and switching function algorithms for three-phase matrix converter based AC motor drives against open and short phase failures[C]. Proc. Rec. IEEE International Electric Machines & Drives Conference(IEMDC). Antalya, Turcky: IEEE, 2007:886-891.

[15] Kwak S, Kim T, Vodyakho O. Four-leg based matrix converter with fault resilient structures and controls for electric vehicle and propulsion systems[C]. Proc. Rec. Vehicle Power and Propulsion Con(VPPC). Arlington, America:IEEE, 2007:519-523.

[16] LU B, Sharma S K. A literature review of IGBT fault diagnostic and protection methods for power inverters[J]. IEEE Trans. Ind. Appl., 2009, 45(5):1770-1777.

[17] Chokhawala R S, Catt J, Kiraly L. A discussion on IGBT shortcircuit behavior and fault protection schemes[J]. IEEE Trans. Ind. Appl., 1995, 31(2):256–263

[18] Duong S V, Schaeffer C, Rouve L L, De Palma J F, Mullert C. Fuses for power IGBT-converters[C]. Proc. Rec. IEEE IAS Annu. Meeting. Denver, America: IEEE, 1994: 1336-1343.