Model Predictive Control of a High-Turn-Ratio Dual Active Bridge Converter Considering Interlinking Inductances

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***Abstract*—Within a more-electric aircraft (MEA) dc power distribution system, dual active bridge (DAB) converters are employed to manage power transfer between different dc buses, or power transfer from/to the energy storage devices, for example, batteries. However, due to the relatively high current slew rate and large current amplitude in the low-voltage (LV) H-bridge, the interlinking inductance between the LV board and the transformer becomes non-negligible, as it introduces a noticeable voltage drop across the transformer secondary side, potentially leading to inaccurate power control. To address this issue, this paper develops a comprehensive mathematical model of DAB converters for a moving discretized control set model predictive control (MDCS-MPC) approach to minimize steady-state errors. The proposed model explicitly incorporates the effect of interlinking inductance and further investigates the relationship between the transferred power and the resulting voltage drop on the LV side. Finally, the effectiveness of the proposed model and MDCS-MPC method is validated through experimental results on a 1000W DAB prototype, with transient performance comparisons against other conventional control strategies.**

***Index Terms*— more-electric aircraft (MEA), low voltage (LV) side voltage drops, moving discretized control set model predictive control (MDCS-MPC), dual-active bridge (DAB) converter.**

I. INTRODUCTION

THE concept of More Electric Aircraft (MEA) is seen to offer many potential benefits such higher efficiency, lower weight and maintenance cost, reduced CO_2 emission etc. [1]. The MEA is replacing the mechanical, hydraulic, and pneumatic subsystems with electrical ones. Compared with conventional aircraft, MEA demands more electrical power [2]. One of the most prospective architectures of MEA Electrical Power System (EPS) is the dc power distribution system due to potential cable savings compared with three-phase AC network. Application of DC network will inevitably result in different voltage levels. In [3], [4], dual dc buses are employed, comprising a high-voltage (HV) 270V dc bus and a low-voltage (LV) 28V dc bus. The 270V bus is typically utilized for high-power applications and the supply of large-scale loads, whereas the 28V bus is designated for low-voltage onboard systems, including avionics and battery charging [5]. Besides, the 28V dc bus is commonly referred to as the essential bus where flight critical loads are connected. The power flow and control between the 270V dc bus and 28V dc bus is thus of extreme interest for aircraft EPS studies. The isolated dual-active bridge (DAB) converters have been widely considered as good candidates for MEA applications due to their sufficient power density, high-frequency galvanic isolation, and bi-directional power transfer capability [6], [7].

The dual-active bridge converter is foreseen to be with great potentials for MEA applications [8]. Using a DAB for 270V/28V conversion is, however, not without challenges. A high turns-ratio transformer (10:1 turns ratio) is required for this DAB converter and this will lead to a significantly larger ac current on the LV side compared with the HV side. Considering a 3kW DAB converter, the current on the LV side will have been already over 100A. Considering such a large current on the LV side and a higher switching frequency due to applications of recently advanced SiC and GaN devices (switching frequency can be pushed beyond 100kHz), the impact of the interlinking inductance between the LV H-bridge board and the transformer, which have been neglected in state-of-the-art studies, need to be considered during modelling and control design for these DAB converters.

It is worth noting that the model has always served as the foundation for control algorithm implementation. The accuracy of the model is directly related to the performance of the control algorithm. Modelling technologies for DAB converters include the reduced-order model [22], [23], improved reduced-order model [24], generalized average model [25], and discretized-time model [26], [27]. Shuai *et al.* [28] have shown that the reduced-order model most accurately predicts the dynamic performance of DABs, considering various transient characteristics such as step changes in input voltage, load, and output reference. Consequently, it is widely employed in controller design.

The control of DAB converters has been extensive studied in the past, including conventional PI control [17], linearization

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control [29], hybrid control [18], virtual direct power control (VDPC) [19], disturbance-observer-based control (DOBC) [30], sliding mode control (SMC) [31]. The PI controller eliminates steady-state error through its integral action, but this comes at the cost of compromised dynamic performance. Moreover, its small-signal model is valid only near a specific operating point and cannot accommodate wide operating condition variations. To reduce transient response times, hybrid control has been introduced with a feedforward structure. Nevertheless, it is found that control performance can be worsened if the actual circuit parameters deviate from those assumed in the control algorithm. Consequently, another feedforward strategy, VDPC has been proposed to address this issue of robustness. In VDPC, a virtual desired power setting is employed to avoid the use of the actual leakage inductance values, resulting in considerable robustness against variations in circuit parameters. However, it is noted that VDPC is not suitable for light load conditions. Furthermore, sliding mode control has been introduced to ensure stability with large signal variations, but it suffers from inherent chattering.

Model predictive control (MPC) is becoming a promising solution for DAB converter control due to its fast dynamic response, convenient inclusion of constraints and nonlinearities, and convenient digital implementation [11]. The application of MPC in DAB converters has only recently emerged, notably through the introduction of the moving discretized control set model predictive control (MDCS-MPC) approach, as first proposed by Chen et al. in [11-13]. The philosophy of MDCS-MPC is very similar to the finite control set model predictive control (FCS-MPC) in drive systems [9], [10]. The MDCS-MPC method in [11] is implemented with triangular phase-shift (TPS) modulation to ensure fast dynamic response of the DAB converter across the full power range. In [12], MPC is applied to the naval DC to accommodate rapid fluctuations induced by pulse power loads. [13] provides a comprehensive stability analysis of the MDCS-MPC framework, offering theoretical support for its deployment in distributed power systems, including power grids. Although MDCS-MPC offers several advantages, its performance is highly dependent on the accuracy of the model. Inaccurate modelling can result in poor power control in DAB converters, such as large steady-state errors. However, due to the typically high conversion ratio and high switching frequency demands of DAB converters in MEA, the impact of the interlinking inductance cannot be neglected in the DAB model formulation. In contract, this effect is not considered in [11-13], because the DAB converters in those studies are designed for low voltage ratio or low switching frequency. Although [11-13] have proposed some effective approaches to address steady-state errors of the MDCS-MPC by introducing additional current or voltage compensations, the issue of DAB converter model accuracy is not fundamentally addressed.

This paper proposes a comprehensive mathematical model considering the impact of the interlinking inductance between the LV H-bridge board and the transformer. Furthermore, based on our developed model, the MDCS-MPC algorithm has been designed and successfully implemented to regulate the DAB currents for charging and discharging batteries onboard MEA. The experimental validation confirms that the proposed DAB mathematical model enhances the applicability of MDCS-MPC in MEA scenarios, offering fast dynamic response and precise control without steady-state errors.

This paper is organized as follows. Section II firstly discusses the basic operation modes of the DAB converter based on traditional SPS modulation, followed by a detailed derivation of the mathematical model including the LV side voltage drops. In Section III, the design of the PI controller and the operating principles of the proposed MDCS-MPC are introduced. Experimental results are provided for a 270V/28V 100-kHz DAB converter in Section IV. Finally, conclusions are drawn in Section V.

II. Mathematical Model for the Voltage Drop on the Low Voltage Side

A. Basic Operation Principles

A DAB converter is effectively using two H-bridges connected by a high-frequency transformer. Commonly used circuit of a DAB is presented in Fig. 1 The HV H-bridge is connected to a high-voltage DC bus with a voltage of V_{HV}. The LV H-bridge is connected to a low-voltage battery with a voltage of V_{LV}. The transformer is represented with an ideal transformer (T_r) and a leakage inductance L_k. Conventionally, the leakage inductance L_k includes leakage inductances from both HV and LV sides and is responsible for the converter power transfer. Considering V_{HV} and V_{LV} are constant values, square voltages v_{ac1} and v_{ac2} should be seen from H-bridges with a fundamental frequency f_s.

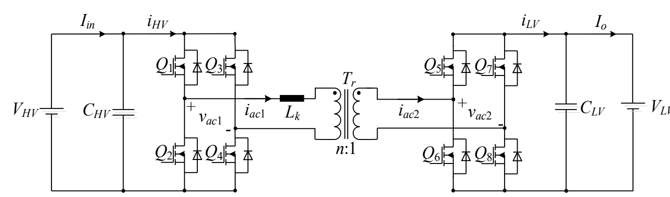


Fig. 1. Diagram of the DAB converter under investigation [15].

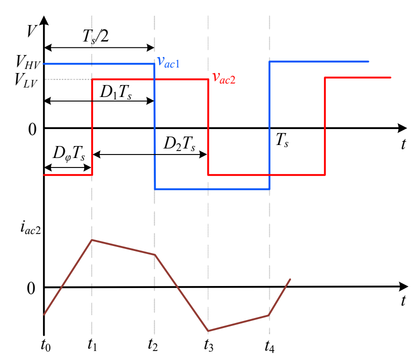


Fig. 2. Waveforms of the DAB converter modulated with traditional SPS.

Waveforms of a DAB converter with conventional single-phase-shift (SPS) modulation are shown in Fig. 2. There, D_1 and D_2 are the duty cycles of v_{ac1} and v_{ac2} respectively, and T_s represents one switching cycle. For the SPS modulation, D_1 and D_2 are commonly fixed at 0.5. The phase shift between square voltages v_{ac1} and v_{ac2} is represented as $D_\varphi T_s$. The phase shift

$D_\varphi T_s$ controls the power transfer between the HV and LV sides. D_φ is the phase shift ratio, and it is defined on the entire switching period with $D_\varphi \in [-0.25, 0.25]$. It is worth noting that a positive value of D_φ indicates the power is transferred from HV to the LV side, with v_{ac1} leading v_{ac2}, and vice versa [14]. These conventional presentations are normally without any issues if currents are low, and the H-bridge is with a relatively slow switching frequency. However, when the currents are large, especially on the LV side, with fast switching H-bridge devices, the impact of the interlinking inductance need to be considered, and an extra noticeable voltage drop may occur at LV side. This extra voltage drop will lead to inaccurate power flow control, for example, resulting in significant steady-state errors and thus degrade power converter performance.

B. Interlinking Inductance Consideration

Considering the interlinking inductance, the diagram of a DAB in Fig.1 can be revised by adding an equivalent inductance L_e between the transformer and LV H bridge as shown in Fig. 3. The voltage drop due to L_e is thus given as

$$V_{drop} = L_e \frac{\Delta i_{ac2}}{\Delta t} \tag{1}$$

where Δi_{ac2} is the current change of i_{ac2} during a time interval Δt. In Fig. 3, the nodes labelled v_{ac2} and v'_{ac2} indicate the actual measurement points under different power flow directions to explore the impact of the equivalent inductance L_e. It should be noted that when power flows from HV side to LV side, the equivalent inductance L_e includes both the interlinking inductance between the LV H-bridge and the transformer, and the potential stray inductances associated with the designed LV H-bridge. In contrast, equivalent inductance L_e represents only the interlinking inductance between the LV H-bridge and the transformer during reverse power flow. However, based on the following analysis and experimental results, it is demonstrated that the equivalent inductance L_e in our case consists only of the interlinking inductance.

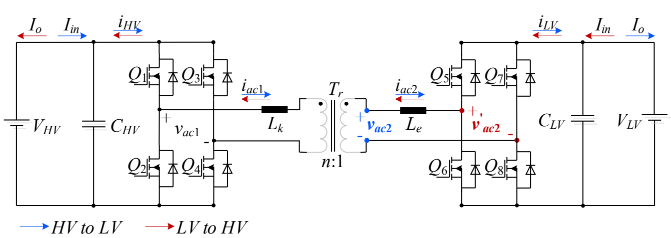


Fig. 3. Revised DAB model considering the interlinking inductance.

It should be noted that the interlinking inductance L_e does not participate in power transmission between the DC buses connected on both sides of the DAB converter, because it is not part of the transformer's leakage inductance. A detailed analysis of the voltage drop V_{drop} will be studied in detail in the next section.

C. Operation Modes of HV to LV Power Flow

Considering the power flow is from HV to LV side. The voltages at the transformer terminals considering the interlinking inductance at LV side are given as Fig. 4. It can be seen that v_{ac1} is leading v_{ac2} under this operation condition. A voltage drop can be noticed at time t_0 or t_2 when the slope of i_{ac2} changes. This results in a voltage step V_{drop} within v_{ac2}.

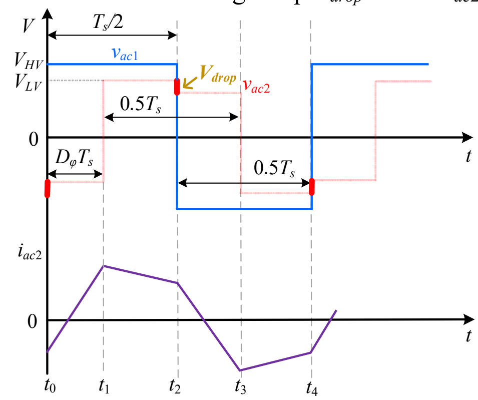


Fig. 4. Conceptual waveforms of the DAB converter modulated with SPS considering the impact of the interlinking inductance under forward power flow condition.

The switching cycle T_s can be divided into four operation modes. These operation modes under the condition of $t_0 \le t \le t_4$ are explained as follows. It is important to state that the relationship between the transformer current i_{ac1} and i_{ac2} is $i_{ac2} = ni_{ac1}$.

Additionally, a judgment criterion is established to determine whether the voltage drop should be considered in each mode, based on the current change of i_{ac2}. The criterion is as follows: when the polarities of the AC voltages differ (e.g., during t_0-t_1, where v_{ac1} is positive and v_{ac2} is negative), the voltage drop should be considered. Conversely, when the polarities of the AC voltages are the same (e.g., during t_1-t_2, where v_{ac1} and v_{ac2} are positive), the impact of voltage drop can be ignored.

1) Mode 1 during time interval ($t_0 - t_1$): In this mode, on the HV side, Q_1 and Q_4 (see Fig. 3) are turned 'ON' and Q_2 and Q_3 are switched 'OFF'. On the LV side, Q_6 and Q_7 are conducting and Q_5 and Q_8 are turned OFF. Due to the fast-change in the current i_{ac2}, the effect of the LV side voltage drop should be considered. As a result, the voltage across L_k is clamped at $V_{HV} + nV_{LV} - nV_{drop}$. During this mode, the current through L_k during this time interval can be expressed as:

$$i_{ac1}(t_1) = i_{ac1}(t_0) + \frac{V_{HV} + nV_{LV} - nV_{drop}}{L_k} D_\varphi T_s \tag{2}$$

2) Mode 2 during time interval ($t_1 - t_2$): In this mode, on the HV side, Q_1 and Q_4 are 'ON' (see Fig. 3), while Q_2 and Q_3 are 'OFF'. On the LV side, Q_5 and Q_8 are switched 'ON' while Q_6 and Q_7 are turned 'OFF'. During this period, the decrease in the instantaneous current is slow (as shown in Fig. 4), thus, voltage drop due to interlinking inductance on the LV side is neglectable. Hence, the voltage across L_k is $V_{HV} - nV_{LV}$, and the current within this time interval can be expressed as:

$$i_{ac1}(t_2) = i_{ac1}(t_1) + \frac{V_{HV} - nV_{LV}}{L_k}(0.5 - D_\varphi)T_s \tag{3}$$

3) Mode 3 during time interval ($t_2 - t_3$): In this mode, for the HV side, Q_2 and Q_3 are 'ON' and Q_1 and Q_4 are turned 'OFF'. However, on the LV side, Q_5 and Q_8 are still 'ON', while Q_6 and Q_7 are kept 'OFF'. As the current i_{ac2} is fast changing, the voltage drops due to interlinking inductance on the LV side need to be considered. The voltage across L_k is thus $-V_{HV} - nV_{LV} + nV_{drop}$. Within this time interval, the current through L_k is:

TABLE I
PROPOSED MODIFIED BASIC MATHEMATICAL MODEL OF DAB WITH SPS MODULATION

Variable	$\mathbf{0 \le D_\varphi \le 0.25}$	$\mathbf{-0.25 \le D_\varphi \le 0}$
$i_{ac1}(t_0)$	$\frac{(1-4D_\varphi)nV_{LV}-V_{HV}+2D_\varphi nV_{drop}}{4f_sL_k}$	$\frac{nV_{LV}-(4D_\varphi+1)V_{HV}+2D_\varphi nV_{drop}}{4f_sL_k}$
$i_{ac1}(t_1)$	$\frac{(4D_\varphi-1)V_{HV}+nV_{LV}-2D_\varphi nV_{drop}}{4f_sL_k}$	$\frac{(1+4D_\varphi)nV_{LV}-V_{HV}-2D_\varphi nV_{drop}}{4f_sL_k}$
$i_{ac1}(t_2)$	$\frac{(4D_\varphi-1)nV_{LV}+V_{HV}-2D_\varphi nV_{drop}}{4f_sL_k}$	$\frac{(4D_\varphi+1)V_{HV}-nV_{LV}-2D_\varphi nV_{drop}}{4f_sL_k}$
$i_{ac1}(t_3)$	$\frac{(1-4D_\varphi)V_{HV}-nV_{LV}+2D_\varphi nV_{drop}}{4f_sL_k}$	$\frac{V_{HV}-(1+4D_\varphi)nV_{LV}+2D_\varphi nV_{drop}}{4f_sL_k}$
P	$\frac{nV_{HV}D_\varphi(1-2D_\varphi)(2V_{LV}-V_{drop})}{2f_sL_k}$	$\frac{nV_{HV}D_\varphi(1+2D_\varphi)(2V_{LV}-V_{drop})}{2f_sL_k}$

$$i_{ac1}(t_3)=i_{ac1}(t_2)+\frac{-V_{HV}-nV_{LV}+nV_{drop}}{L_k}D_\varphi T_s \tag{4}$$

4) Mode 4 during time interval (t_3 – t_4): Similar to Mode 2, current i_{ac2} is with slower changing rate and the voltage across L_k is given as $-V_{HV}+nV_{LV}$. Thus, the current through L_k is:

$$i_{ac1}(t_4)=i_{ac1}(t_3)+\frac{-V_{HV}+nV_{LV}}{L_k}(0.5-D_\varphi)T_s \tag{5}$$

Considering the symmetry within one switching interval, the average current i_{ac1} over one switching cycle should be zero in steady state with

$$\begin{cases} i_{ac1}(t_3)=-i_{ac1}(t_1) \\ i_{ac1}(t_2)=-i_{ac1}(t_0) \end{cases} \tag{6}$$

The average transferred power can be expressed as [16]:

$$P=\frac{2}{T_s}\int_0^{T_s/2} v_{ac1}i_{ac1}(t)\,dt \tag{7}$$

Assuming $t_0 = 0$, then under the condition $-0.25 \le D_\varphi \le 0.25$: $t_1 = D_\varphi T_s$, $t_2 = 0.5T_s$, $t_3 = (D_\varphi + 0.5)T_s$, and $t_4 = T_s$. Combining (2) to (7), the peak currents of half a switching cycle, and the average transmission power can be derived as shown in Table I with all the different operation modes, where $f_s = 1/T_s$ is the switching frequency.

D. Explicit expression of V_{drop}

From Fig. 4, it can be seen that at time instant $t = t_0$ and $t = t_2$, a small voltage step can be noticed at transformer secondary side v_{ac2}. This voltage drop can be calculated based on the expression as:

$$V_{drop}=L_e\frac{\Delta i_{ac2}}{\Delta t}=nL_e\frac{\Delta i_{ac1}}{\Delta t} \tag{8}$$

where Δi_{ac1} is change of the HV side transformer ac current i_{ac1} during time interval Δt. When the power flow from HV to LV side, Δi_{ac1} is determined based on time interval [t_0, t_1] or [t_2, t_3].

$$\Delta i_{ac1}=\left|i_{ac1}(t_1)-i_{ac1}(t_0)\right|=\frac{(V_{HV}+nV_{LV}-nV_{drop})D_\varphi T_s}{L_k} \tag{9}$$

$$\Delta t=t_1-t_0=D_\varphi T_s \tag{10}$$

Substituting (9) and (10) into (8), the LV side voltage drop can be calculated, as shown in (11).

$$V_{drop}=\frac{(V_{HV}+nV_{LV})nL_e}{L_k+n^2L_e} \tag{11}$$

Substituting (11) of V_{drop} expression into Table I, the operation model of a DAB considering interlinking inductance on the LV side can be derived in detail and shown in Table II.

E. Operation Modes Analysis on Backward Power Flow

Under this operation condition, the power flow from LV to HV is achieved when v'_{ac2} leads v_{ac1}. In this situation, the value of the phase shift ratio is negative. Similar scenarios can also be noticed when the power is transferred from LV to the HV side and a voltage drop V_{drop} can be noticed when current i_{ac2} changing rates increased at t_0 and t_2 time instant, as shown in Fig. 5. Similar to the forward power flow operation condition, there are four operation modes from t_0 to t_4. Similar analysis can be done as that in previous section and will not be detailed in this paper.

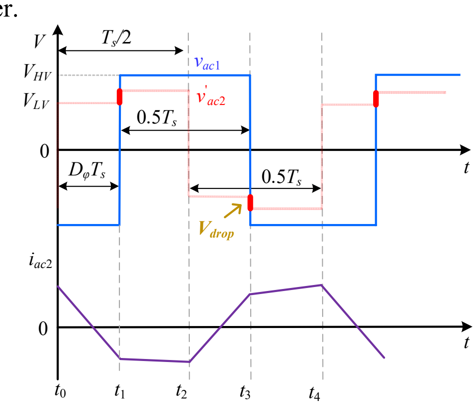


Fig. 5. Conceptual waveforms of the DAB converter modulated with SPS considering the impact of the interlinking inductance under backward power flow condition.

III. PI & MDCS-MPC FOR OUTPUT CURRENT REGULATION

As the studied DAB is to manage the power flow between two different DC buses (270Vdc bus and 28Vdc bus) on board more-electric aircraft, the main control objective of the studied DAB is to thus regulate the output current I_o of the converter on the LV side, charging or discharging a 28V dc battery from a 270V dc bus. The DC voltages on these two DC buses are defined by upper-steam power generation system at 270V at the

TABLE II
DETAILED PROPOSED MODIFIED BASIC MATHEMATICAL MODEL OF DAB INCLUDING LV VOLTAGE DROP EXPRESSION

Variable	$\mathbf{0 \le D_\varphi \le 0.25}$	$\mathbf{-0.25 \le D_\varphi \le 0}$
$i_{ac1}(t_0)$	$\frac{\left[\left(1-4D_\varphi\right)nV_{LV}-V_{HV}\right]L_k+\left(1-2D_\varphi\right)\left(nV_{LV}-V_{HV}\right)n^2L_e}{4f_sL_k\left(L_k+n^2L_e\right)}$	$\frac{\left[nV_{LV}-\left(4D_\varphi+1\right)V_{HV}\right]L_k+\left(2D_\varphi+1\right)\left(nV_{LV}-V_{HV}\right)n^2L_e}{4f_sL_k\left(L_k+n^2L_e\right)}$
$i_{ac1}(t_1)$	$\frac{\left[\left(4D_\varphi-1\right)V_{HV}+nV_{LV}\right]L_k+\left(2D_\varphi-1\right)\left(V_{HV}-nV_{LV}\right)n^2L_e}{4f_sL_k\left(L_k+n^2L_s\right)}$	$\frac{\left[\left(1+4D_\varphi\right)nV_{LV}-V_{HV}\right]L_k+\left(2D_\varphi+1\right)\left(nV_{LV}-V_{HV}\right)n^2L_e}{4f_sL_k\left(L_k+n^2L_e\right)}$
$i_{ac1}(t_2)$	$\frac{\left[\left(4D_\varphi-1\right)nV_{LV}+V_{HV}\right]L_k-\left(1-2D_\varphi\right)\left(nV_{LV}-V_{HV}\right)n^2L_e}{4f_sL_k\left(L_k+n^2L_e\right)}$	$\frac{\left[\left(4D_\varphi+1\right)V_{HV}-nV_{LV}\right]L_k-\left(2D_\varphi+1\right)\left(nV_{LV}-V_{HV}\right)n^2L_e}{4f_sL_k\left(L_k+n^2L_e\right)}$
$i_{ac1}(t_3)$	$\frac{\left[\left(1-4D_\varphi\right)V_{HV}-nV_{LV}\right]L_k-\left(2D_\varphi-1\right)\left(V_{HV}-nV_{LV}\right)n^2L_e}{4f_sL_k\left(L_k+n^2L_e\right)}$	$\frac{\left[V_{HV}-\left(1+4D_\varphi\right)nV_{LV}\right]L_k-\left(2D_\varphi+1\right)\left(nV_{LV}-V_{HV}\right)n^2L_e}{4f_sL_k\left(L_k+n^2L_e\right)}$
P	$\frac{V_{HV}D_\varphi\left(1-2D_\varphi\right)\left[nV_{LV}\left(2L_k+n^2L_s\right)-V_{HV}n^2L_e\right]}{2f_sL_k\left(L_k+n^2L_e\right)}$	$\frac{V_{HV}D_\varphi\left(1+2D_\varphi\right)\left[nV_{LV}\left(2L_k+n^2L_s\right)-V_{HV}n^2L_e\right]}{2f_sL_k\left(L_k+n^2L_e\right)}$

HV side, and by battery at LV terminal 28V side. With the developed model from the previous section, in this section, we will introduce the implementation of MDCS-MPC for the studied DAB. Although we focus on the operation conditions where the power is flowing from HV to LV side, similar analysis can be used for the scenarios when the power is transferred from LV to HV side conveniently.

A. Output Current Modelling

The average model of the DAB converter is presented in Fig. 6. In steady state, the current I_c flowing into the capacitor C_{LV} is zero, thus, the output current at the LV terminal is defined as [14]:

$$I_o = I_{LV} = \frac{2}{T_s}\int_0^{T_s/2} i_{ac2}(t)\,dt \tag{12}$$

Using Table II (scenario $0 \le D_\varphi \le 0.25$), the output currents at the LV terminals can thus be derived using (13) as:

$$I_o = \frac{V_{HV}D_\varphi\left(1-2D_\varphi\right)\left[nV_{LV}\left(2L_k+n^2L_e\right)-V_{HV}n^2L_e\right]}{2V_{LV}f_sL_k\left(L_k+n^2L_e\right)} \tag{13}$$

It can be noticed that (13) is much more detailed capturing the impact of the interlinking inductance L_e compared with the conventional model as:

$$I_o = \frac{nV_{HV}D_\varphi\left(1-2D_\varphi\right)}{f_sL_k}. \tag{14}$$

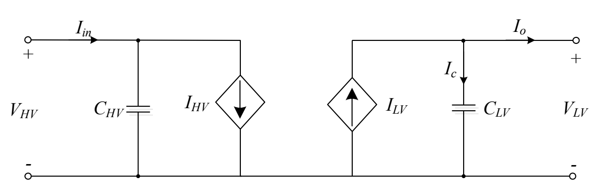


Fig. 6. Average model of the DAB converter.

B. Proportional Integral Controller Design

In comparison with the following proposed MDCS-MPC controller, a PI controller is designed in this Section, in order to illustrate the response time of the traditional linear control method. The dynamic equation of the output current is shown in (13). In order to derive the related small-signal model, small perturbations are superimposed on the equilibrium point D_φ. As a result, the transfer function of the converter is given by (15), where the equilibrium point is indicated by the notation with a bar ($\bar{X}$):

$$G_{sps}(s) = \frac{nV_{HV}\left(1-4\overline{D_\varphi}\right)\left[nV_{LV}\left(2L_k+n^2L_e\right)-V_{HV}n^2L_e\right]}{2V_{LV}f_sL_k\left(L_k+n^2L_e\right)} \tag{15}$$

As it can be noticed from (15) that, there are no dynamics to control rather than a gain. For the above designed PI controller, the main purpose is to eliminate the steady-state error.

The control block diagram is depicted in Fig. 7, where the small signal of the phase shift D_φ is modified according to the error between I_o and its reference value I_{o_ref}. A PI compensator $G_c(s)$ is utilized to minimize the steady state error, which is defined in (16). It worth noting that the control parameters of the PI controller are closely related to the transient response speed. To ensure a fairness of the comparison between the proposed control approaches, the PI controller is designed to achieve the fastest response speed, considering the practical response delay of the digital PWM.

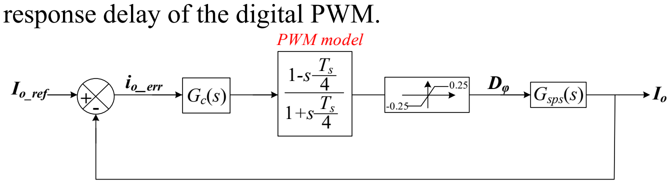


Fig. 7. Control block diagram of the PI controller.

In this paper, a digital PWM model (see Fig. 7) [21] is considered during the design stage of the PI controller. The natural frequency of the designed PI controller is influenced by the switching frequency of the PWM signals. As a result, the fastest dynamic response speed can be achieved. The key parameters k_p, k_i are determined according to the Infineon design guidance shown in [20], and the related parameters are chosen as: damping factor $\xi = 0.707$, natural frequency $\omega_0 = 6280$ rad/s. As a result, the PI parameters are set as $k_p = 0.009$ and $k_i = 911.95$.

$$G_c(s) = k_p + \frac{k_i}{s} \tag{16}$$

C. MDCS-MPC Control Design

The developed control scheme is to control the DAB output current I_o is following its demand I_{o_ref}. In order to fit the operating principle of the proposed MDCS-MPC, discretized model for the output current I_o is essentially needed. By applying the Euler backward discretization, dynamic equation shown in (13) is developed into:

$$I_o[k+1] = \lambda D_\varphi[k+1](1 - 2D_\varphi[k+1]) \tag{17}$$

where

$$\lambda = \frac{V_{HV}\left[nV_{LV}\left(2L_k + n^2 L_e\right) - V_{HV} n^2 L_e\right]}{2V_{LV} f_s L_k \left(L_k + n^2 L_e\right)} \tag{18}$$

where $I_o[k+1]$ is the predicted output current at time instant $k+1$, and $D_\varphi[k+1]$ is the selected optimal phase shift value at time instant $k+1$.

It is worth mentioning that a digital implementation delay has to be considered in the practical application. At time instant k, the sensors will measure data $X(k)$ and the microprocessor will calculate the control parameters, in our case phase shift $D_\varphi(k)$. However, the control parameter $D_\varphi(k)$ can only be implemented at $k+1$ instant and the resulted controller parameter can only be measured at $k+2$ time instant. To account for the digital control delay, an additional step needs to be added, resulting in the two-step predictive model. From (17), we have the current I_o at $k+2$ time instant as

$$I_o[k+2] = \lambda D_\varphi[k+1](1 - 2D_\varphi[k+1]) \tag{19}$$

where λ follows the same definition shown in (18), and $I_o[k+2]$ is the predicted output current at time instant $k+2$. The developed discretized model shown in (19) will be used at the estimation and prediction stages of the proposed MDCS-MPC controller, detailed analysis is proposed as follows.

The principle of moving discretized control set model predictive control (MDCS-MPC) scheme is as follows:

1. It is known that the output current I_o is a function of the phase shift D_φ as indicated in Table II. To regulate I_o to follow I_{o_ref} is effectively to find the optimal phase shift D_φ.

2. The phase shift at time instant $k+1$, $D_\varphi(k+1)$, can essentially be seen as adding or minus an increment to that used in the time instant k, i.e., $D_\varphi(k+1) = D_\varphi(k)+\Delta D_\varphi$.

3. Controlling the output current I_o is effectively to identify an optimal $D_\varphi(k+1)$ at each time instant k.

Bering this in mind, we can thus firstly divide or discretize the entire phase shift range [-0.25,0.25] to be a series of phase shifts with small equal interval Δ_f as

$$D_\varphi \in \{-0.25, \ldots, -2\Delta_f, -\Delta_f, 0, \Delta_f, 2\Delta_f, \ldots, 0.25\} \tag{20}$$

where Δ_f is defined as $\Delta_f = f_s/f_c$. f_s is the switching frequency of the converter, and f_c is the peripheral clock frequency of the applied digital control platform [12].

The total number of these intervals μ_m can thus be defined as

$$\mu_m = \frac{0.5}{\Delta_f} + 1 \tag{21}$$

The maximum number μ_m represents the finest points that can be achieved in the chosen commercial digital control platform. However, in order to avoid the heavy computational burden issue, only a small number of points μ ($\mu \le \mu_m$) centred at the previous working point will be assessed in each sampling period. At each time instant k when the phase shift $D_\varphi[k]=m$, the controller may search the optimal $D_\varphi[k+1]$ only around m. Considering the computation burden, at time instant k, the D_φ search range (defined as discretized control set (DCS)) will be limited to μ=3 points in total , i.e., the DCS is defined as $\{m-\Delta_f, m, m+\Delta_f\}$.

The phase shift within this DCS which gives the minimum error between the current I_o and its reference I_{o_ref} will be selected as the optimal as $D_\varphi[k+1]$. The error between the current I_o and its reference I_{o_ref} is referred to as the cost function (CF in the equation) and defined as

$$CF = (I_{o\_ref} - I_o[k+2])^2 \tag{22}$$

It is worth mentioning that (22) is not the finalized cost function, but a simplified one to help illustrate the operating principle of the proposed MDCS-MPC control strategy.

The calculation process of the proposed multi-dimensional MDCS-MPC is illustrated in Fig. 8, where μ=3 points are chosen and assessed in each sampling cycle. The square voltage waveforms of HV and LV H-bridges are presented in the two tops figures, where the duty cycles of the HV and LV side square voltage waveforms v_{ac1} and v_{ac2} are fixed to 0.5. The present working point is assumed to be $D_\varphi[k]=m$, therefore, the present discretized control set (DCS) for D_φ is defined as $\{m-\Delta_f, m, m+\Delta_f\}$. At time instant $k+1$, different $D_\varphi[k+1] \in \{m-\Delta_f, m, m+\Delta_f\}$ will be used for $I_o[k+2]$ calculation, resulted in different output currents $I_o^{(1)}[k+2]$, $I_o^{(2)}[k+2]$, $I_o^{(3)}[k+2]$ respectively. The smallest cost function will be identified (in this case it is $I_o^{(3)}[k+2]$ and its corresponding phase shift is $m+\Delta_f$). Therefore, $D_\varphi[k+1] = m+\Delta_f$ is assumed and used for implementation. For the control period $k+1$ to $k+2$, the DCS changes to $\{m, m+\Delta_f, m+2\Delta_f\}$. At time instant $k+2$, $I_o^{(1)}[k+3]$ results in the smallest cost function, thus the related phase shift value $D_\varphi[k+2] = m$ is applied at the time instant $k+2$. Consequently, the DCS now changes to $\{m-\Delta_f, m, m+\Delta_f\}$. This process continues.

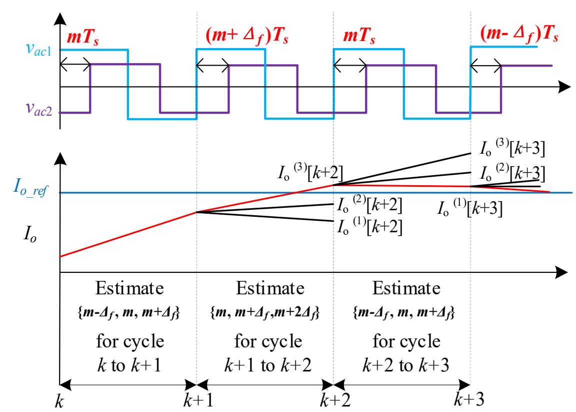


Fig. 8. Operating principle of the proposed MDCS-MPC for the DAB. μ is set to be 3 in this evaluation.

D. *Further Discussion on Cost Function*

The cost function in (22) makes sure that the output current I_o is following its reference I_{o_ref}. However, there is no constraint on the transient performance for the MDCS-MPC. To address such as issue, another term will have to be introduced into the cost function as

$$CF = \alpha_1 G_1 + \alpha_2 G_2 \tag{23}$$

where

$$\begin{cases} G_1 = \left(I_o[k+2] - I_{o\_ref}\right)^2 \\ G_2 = \left(I_o[k+2] - I_o[k+1]\right)^2 \end{cases} \tag{24}$$

where α_1 and α_2 are the two weighting factors.

In (24), G_1 is responsible for regulating the output current I_o to its reference value I_{o_ref}. Meanwhile, G_2, which represents the difference between the two nearby predicted output currents $I_o[k+2]$ and $I_o[k+1]$, is used to improve the transient response of the control system. When the predicted I_o is far from its reference value I_{o_ref}, the dominant role is taken by the term G_1. On the other hand, when I_o is regulated closely to its reference value, the cost function is strongly influenced by G_2. In this case, the transient performance can be improved.

Based on the design procedures presented in previous sections, a high-level diagram of the MDCS-MPC is shown in Fig. 9, where V_{HV}, V_{LV} are the voltage obtained from HV and LV DC buses, and I_o is the output current measured from the current sensor. μ points are evaluated and utilized in each sampling period at the estimation and prediction procedures. At the final stage, the optimal element $D_\varphi[k+1]$ which leads to the minimal cost function is regarded as the instant output of the MDCS-MPC controller to drive the DAB converter.

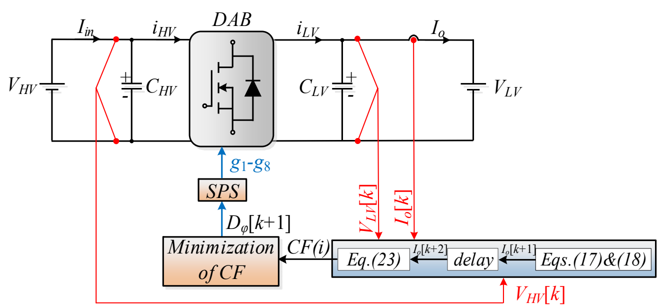


Fig. 9. A high-level diagram of the proposed MDCS-MPC strategy.

E. Robustness Evaluation Against Parameter Variations

To evaluate the robustness of the designed MDCS-MPC method against parameter variations, the effects of key parameters including V_{HV}, V_{LV}, L_e, and L_k are investigated based on the local control expression of I_o given in (13). The variation of V_{HV} and V_{LV} follows the typical aircraft electrical power specification [32]: $V_{HV} \in$ [250V, 280V] and $V_{LV} \in$ [22V, 29V]. Four representative cases are constructed to cover all boundary scenarios: Case 1: V_{HV} =250V, V_{LV} =22V; Case 2: V_{HV} =250V, V_{LV} =29V; Case 3: V_{HV} =280V, V_{LV} =22V and Case 4: V_{HV} =280V, V_{LV} =29V. The nominal operating condition is set at V_{HV} =270V and V_{LV} =28V as a reference group.

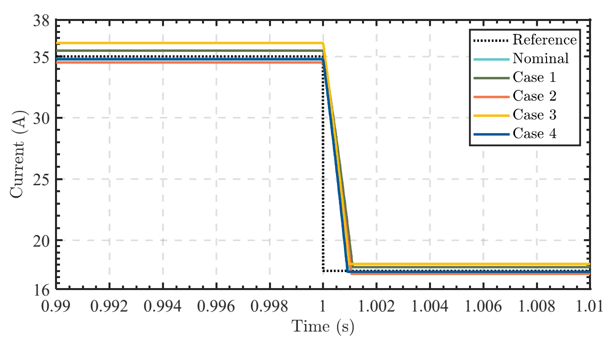


Fig. 10. Simulation results under the varying two dc bus voltages. Nominal: V_{HV} =270V, V_{LV} =28V; Case 1: V_{HV} =250V, V_{LV} =22V; Case 2: V_{HV} =250V, V_{LV} =29V; Case 3: V_{HV} =280V, V_{LV} =22V and Case 4: V_{HV} =280V, V_{LV} =29V.

As shown in Fig. 10, the reference current is stepped from 35A to 17.5A at t=1s to evaluate the dynamic performance of the controller under varying load conditions. Among the four cases, the largest steady-state error, approximately 1A, occurs in Case 3. This steady-state deviation is primarily attributed to variations in the converter's operating conditions, which in turn result in a voltage mismatch across the transformer.

The interlinking inductance L_e is also varied across four cases, ranging from −20% to +20% of its nominal value: Case A: 77.68nH (-20%); Case B: 87.39nH (-10%); Case C: 106.81nH (10%) and Case D: 116.52nH (20%). The corresponding simulation results are shown in Fig. 11, where the maximum steady-state error remains within 0.2 A for all Cases. Similar behavior is observed in Fig. 12, where the leakage inductance L_k is varied from −20% to +20% of its nominal value. The maximum steady-state error of 0.3A generated in Case II indicates that variations in L_k have a relatively minor impact compared to variations in V_{HV} and V_{LV}.

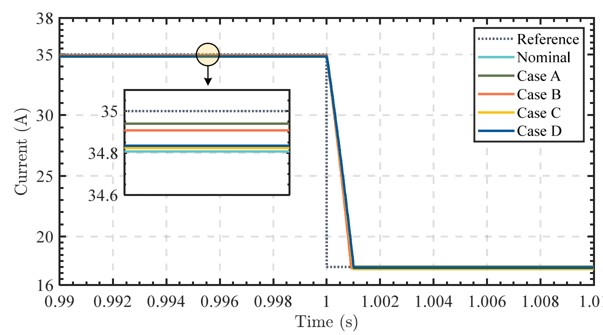


Fig. 11. Simulation results under the varying interlinking inductance L_e. Nominal: L_e =97.1n*H*; Case A: L_e =77.68nH; Case B: L_e =87.39nH; Case C: L_e =106.81nH and Case D: L_e =116.52nH.

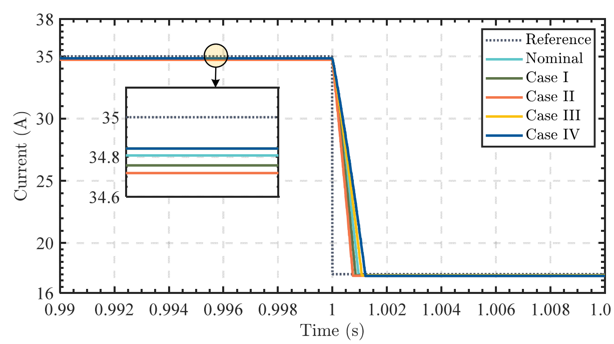


Fig. 12. Simulation results under the varying leakage inductance L_k. Nominal: L_k =46μH; Case I: L_k =41.1μH; Case II: L_k =36.8μH; Case III: L_k =50.6μH and Case IV: L_k =55.2μH.

Based on the above simulation results, it can be concluded that the designed MDCS-MPC method with V_{drop} consideration demonstrates strong robustness, particularly against variations in internal parameters of the DAB converter, such as the leakage inductance L_k and the interlinking inductance L_e. Although variations in external parameters, such as bus voltage fluctuations, may introduce some steady-state error, the controller consistently maintains a fast transient response speed.

IV. Experimental Verification

The experiment on the LV side voltage drop was conducted using a 1kW, 100 kHz, 270V/28V laboratory prototype of the DAB converter. Extensive experiments have been carried out on this DAB converter, with the corresponding parameters

TABLE III
PARAMETERS OF THE TEST SYSTEM (SEE FIG. 9)

Description	Value	Unit
Switching frequency f_s	100	kHz
Dead time t_d	80	ns
Transformer turns ratio n	10:1	/
Transformer magnetizing inductance L_m	12	mH
Transformer leakage inductance L_k	46.0	μH
Total interlinking inductance L_e	97.1	nH
LV side DC capacitor C_{LV}	65.8	μF
HV side DC capacitor C_{HV}	17.3	μF
Rated power P	1	kW
HV DC bus voltage V_{HV}	270	V
LV DC bus voltage V_{LV}	28	V
Sampling time t_s	10	μs

listed in Table III. The proposed MDCS-MPC control algorithm was verified on the experimental DAB test platform shown in Fig. 13**Fig. *13*.** Experiment DAB test.. The power stage consists of two Delta Elektronika SM500-CP-90 DC power supplies, and a TMS320F2837xD evaluation board from Texas Instruments is used as the digital control platform and communication interface with a host computer.

The experiment DAB test corresponds to the high-level diagram shown in Fig. 9, with parameters provided in Table III. GaN devices GS66516T are used for the HV full-bridge switches, with a hardware deadtime of 80ns. GaN MOSFET devices EPC2021, also with an 80ns hardware deadtime, are used for the LV H-bridge switches. The integrated leakage inductance in the high-frequency transformer is responsible for power transfer, has a value of 46 μH at the rated power. It is worth noting that the weighting factors α_1 and α_2 are chosen as 1 and 0.001, respectively.

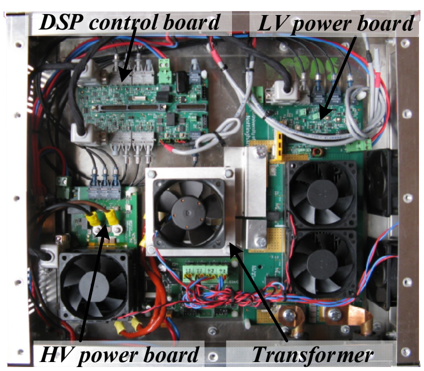


Fig. 13. Experiment DAB test.

A. LV Voltage Drop

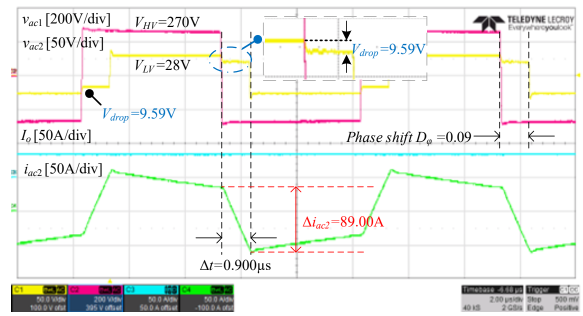
Firstly, experiments are carried out to verify the characteristics of the proposed LV side voltage drop model. Fig. 14 shows experimental results when the DAB converter is transferring 1kW power between HV and LV sides. The phase shift ratio D_φ is set between 0.09 to -0.09 to achieve forward and backward power transmission. It has been demonstrated as shown in Fig. 14 (*a*) and (*b*) that the LV side voltage drops are the same in both forward and backward power flow situations (with a voltage drop of 9.59 V in both directions). This result is in line with the theorical analysis in Section II-D. The calculated LV side voltage drop based on the system parameters presented in Table III is:

$$V_{drop} = \frac{(V_{HV} + nV_{LV})nL_e}{L_k + n^2 L_e} = 9.578 \text{ V} \tag{25}$$

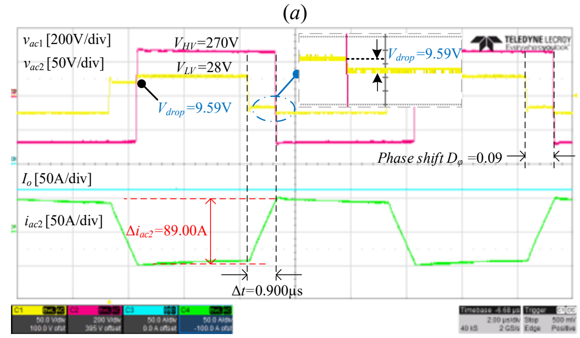
Similarly, the voltage drop located on the LV side can be calculated using the expression in (1), as

$$V_{drop} = L_e \frac{\Delta i_{ac2}}{\Delta t} = \frac{88.97 \text{ A}}{0.9 \text{ μs}} = 9.59 \text{ V} \tag{26}$$

The same voltage drops 9.59 V in Fig. 14 (*a*) and (*b*) validate that the value of the LV side voltage drop has no relationship with the power transfer directions.

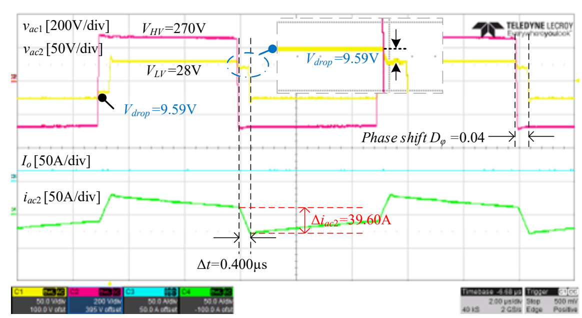


(*a*)

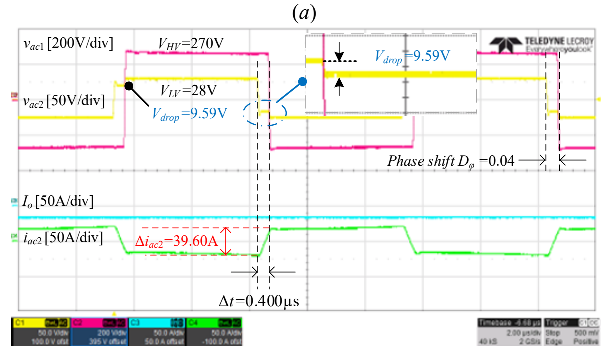


(*b*)

Fig. 14. Experiment waveforms of the DAB converter operating under 1000W. (*a*) Power is transferred from HV side to LV side. (*b*) Power is transferred from LV side to HV side.



(*a*)



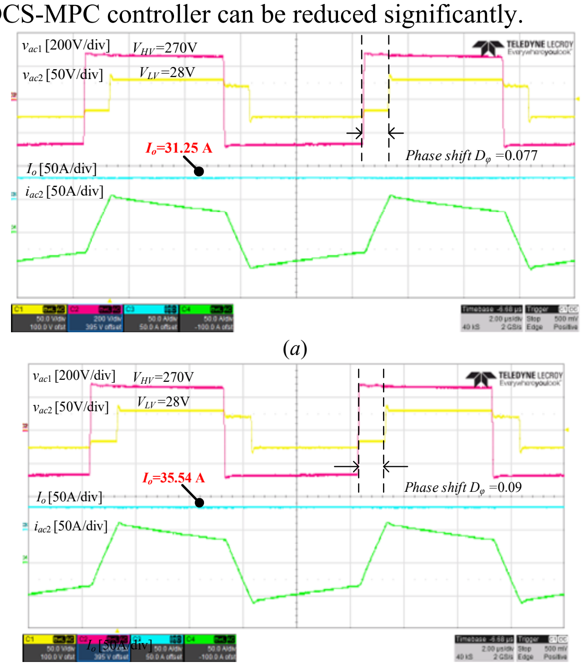
(*b*)

Fig. 15. Experiment waveforms of the DAB converter operating under 500W. (*a*) Power is transferred from HV side to LV side. (*b*) Power is transferred from LV side to HV side.

Additionally, as shown in Fig. 15 (*a*) and (*b*), the DAB converter operates at 500W for both forward and backward power flow directions. The phase shift ratio D_φ is set between 0.04 to -0.04 to achieve forward and backward power transfer. Consequently, the LV side voltage drop 9.59 V remains the same as that observed at 1kW. This validates that the LV side voltage drop is independent of the amount of power transferred.

B. *The Proposed MDCS-MPC*

The impact of the interlinking inductance L_e on the current control performance of the MDCS-MPC method is demonstrated in Fig. 16. The same current references 35A are setup for the models with and without drop considerations simultaneously to transfer 1kW power from the HV side to the LV side. The experimental results of the MDCS-MPC controller without LV voltage drop consideration are shown in Fig. 16 (a). It can be seen that the output current is regulated to 31.25A rather than the reference value of 35 A, resulting in a steady-state error of 4.45A attributable to model mismatch. Besides, the phase shift D_φ can only reach to 0.077 under this situation. However, when the LV side voltage drop model is implemented, the output current can be controlled to 35.54A using a 0.09 phase shift, with a steady state error of 0.54A as shown in Fig. 16 (*b*). In other words, for the same setup power transmission of 1kW, over 120W power cannot transfer to the LV side because of the interlinking inductance L_e. These phenomena are also evident in (13) and (14), the added interlinking inductance modifies the expression of the controlled current, thereby further affecting the control performance. Hence, it can be concluded that by including the LV side voltage drop model, the steady-state error of the MDCS-MPC controller can be reduced significantly.



(*b*)

Fig. 16. MDCS-MPC current regulation steady state performance. (*a*) Without the LV voltage drop model in (14). (*b*) With the LV voltage drop model in (13).

C. *Comparison with other control methods*

A comparative study of the transient control performance for output current regulation between PI, hybrid, VDPC and MDCS-MPC control methods is presented in Fig. 17. As it can be observed from Fig. 17 (*a*) that, the response time of traditional PI controller is the significantly long, as 900 μs. The transient control performance of the proposed two feedforward control strategies, hybrid control and VDPC, is shown in Fig. 17 (*b*) and (*c*). These feedforward controls use the load current information to calculate the phase shift ratio close to its steady state value. As a result, by incorporating the feedforward structure, the response time is reduced to 495 μs and 230 μs respectively. However, when the size of the discretized control set is chosen to be only 3, the transient response time of the proposed MDCS-MPC is 150 μs, as shown in Fig. 17 (*d*). Moreover, increasing the size of the discretized control set (μ) per sampling period can further improve the transient response of the proposed MDCS-MPC, as long as the computational load remains manageable. The transient experimental results show that the MDCS-MPC method achieves nearly six times faster response than conventional PI control. Moreover, benefiting from its ability to predict future system behavior, it also outperforms the two feedforward control methods in transient performance. It worth noting that the proposed modified mathematical model considering the LV side voltage drop was implemented into the MDCS-MPC controller, as a small steady-state error is achieved (within 0.5A). Thus, it is verified that the MDCS-MPC considering the impact of converter LV side interlinking inductance can provide stiff current regulation with a significant decrease in response time.

V. CONCLUSION

In this paper, a modified mathematical model of the DAB converter including LV side voltage drop is developed for the dc distribution system in MEA applications. Consequently, an MDCS-MPC control strategy is employed to regulate the output current on the LV dc bus based on the developed model. Based on the results obtained: (1) it is found that the LV side voltage drop has no relationship with how much power is delivered by the DAB converter, (2) the MDCS-MPC control method can achieve fast transient response speed and can significantly reduce the steady-state errors of the control performance in the regulation of the output current on the LV dc bus compared to the traditional SPS modulation-based model. This is a big gain as it ensures efficient and accurate operation of the DAB converter employed in the MEA applications, as compensation for the impact of the interlinking inductance has been achieved. Furthermore, these findings can be developed to fit advanced modulation methods, such as dual-phase shift (DPS) modulation, and triple-phase shift (TPS) modulation.

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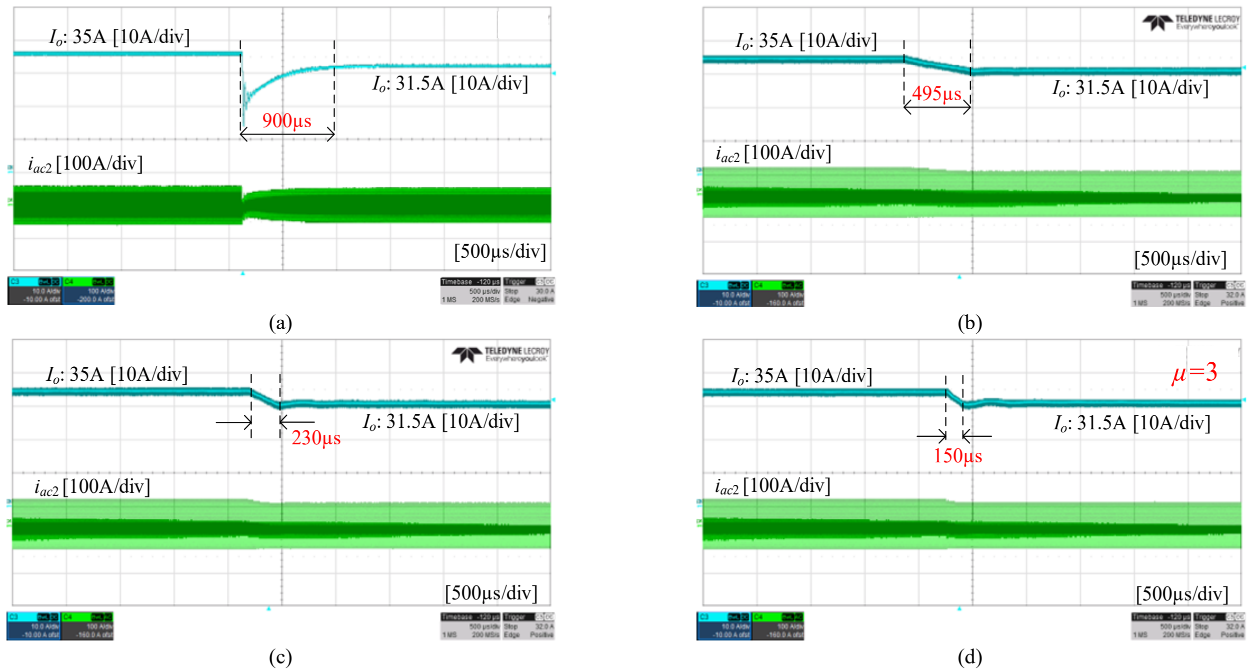

Fig. 17 Output current regulation transient control performance comparison between (*a*) PI control. (*b*) Hybrid control. (*c*) VDPC. (*d*) MDCS-MPC with the proposed modified mathematical model in (14).

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