Conducted Emission Mitigation for Solid-State Transformer using Modulation and Multiple Configuration Techniques

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***Index Terms*—Solid-State Transformer, Modulation strategy, EMC/EMI, common-mode current, dV/dt.**

***Abstract*—Solid-state transformers have several advantages over conventional 50 Hz transformers. However, the high switching speed of power electronic devices generates electromagnetic interference (EMI) that can cause malfunction. Conducted emission mitigation techniques for solid-state transformers using appropriate modulations and configurations in the QSPICE simulator are analysed in time and frequency domains. Common-mode (CM) emission and reactive power can be improved using proper modulation and configuration techniques for single and multiple solid-state transformers. The single-phase shift modulation has the lowest CM emission and the highest reactive power. In contrast, the triple-phase shift modulation demonstrates the highest CM emission and the lowest reactive power among the various modulation strategies. The CM emission of single and multiple solid-state transformers with dV/dt cancellation capability is below the IEC 62041-2020 standard limits.**

I. INTRODUCTION

The plan to make Europe the first climate-neutral continent by 2050 will be achieved by electrifying the main CO2 emission sectors such as transportation using renewable energy sources. Solid-state transformers (SST) are potential solutions for integrating several renewable energy sources and energy storages with more flexible control and the ability to link asynchronous systems [1]. However, the high dV/dt of the switching devices, the switching frequency and the parasitic capacitances in the transformer windings and the switching devices cause EMI [2], [3], which can affect the sensitive devices in the complex and dynamic railway system.

Most of the research done on SST focuses on modulation techniques to eliminate reactive power [4], [5] and extend the range of operation of zero voltage switching (ZVS) [6]–[8]. An analytical model-based CM voltage proposed in [9] considering several modulation techniques for the dual active bridge (DAB) converter. However, the analysis did not consider the transformer's intra-winding parasitic capacitances. In addition, the current through the transformer interwinding capacitance at each switching event was not explained. CM current analysis considering dV/dt cancellation, including part-to-part skew compensation, using parallel DAB and modulation techniques, is presented in [10]. PWM strategy proposed by [11] to cancel the CM noise generated by multicell DC–AC converter while [12] used symmetrical coupled phase-shifted inductors and modulation techniques to suppress the CM voltage of a three-level DAB. Most of the previous work focuses on reactive power improvement without considering CM noise and few on CM noise reduction by excluding reactive power.

This paper clearly shows how each modulation technique of SST can produce unwanted current in the transformer winding parasitic capacitances during the switching event and their impact on the reactive power. Additionally, the common-mode (CM) emission measurement is performed using a line impedance stabilization network (LISN). An analysis is conducted in both the time and frequency domains while considering conducted emission limits. The remaining sections are organised as follows: section II explains the detailed SST model and modulation strategies, section III describes multiple SST configuration options for better EMI reduction, section IV presents the results and discussions, and section V concludes.

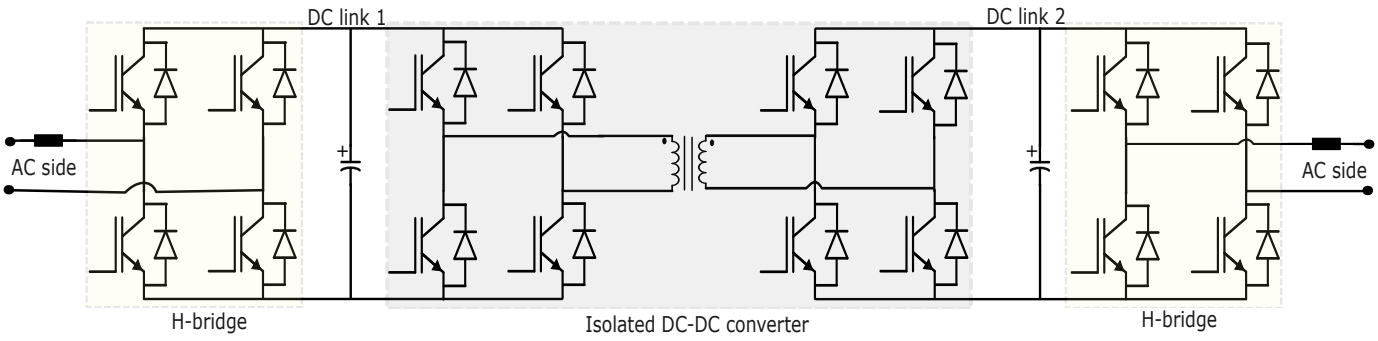


Fig. 1: UNIFLEX-PM single AC/DC/DC/DC/AC module [13].

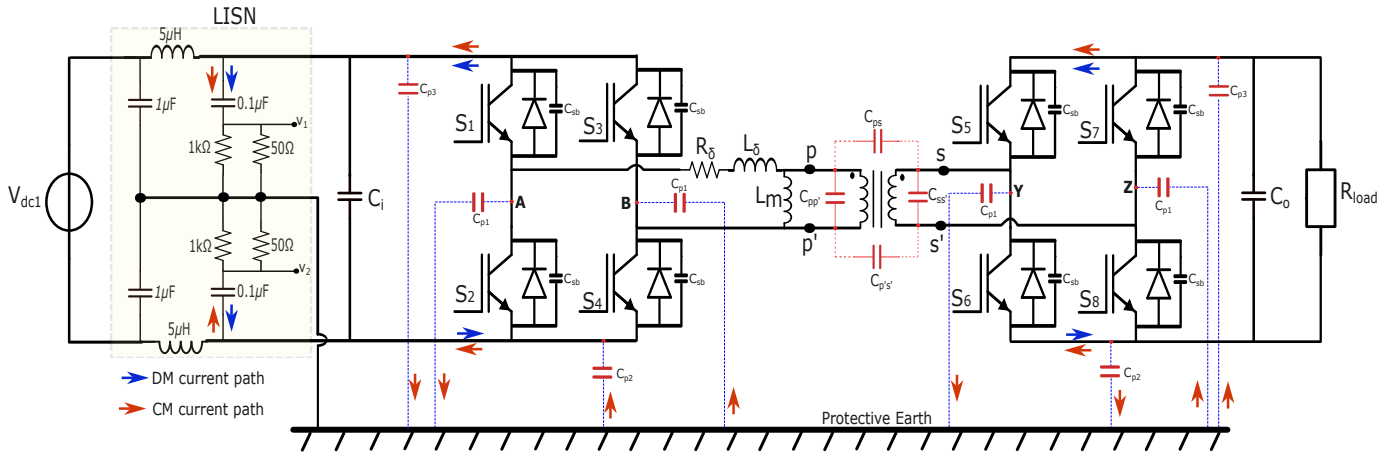


Fig. 2: Solid state transformer including parasitics, snubber capacitor, and LISN.

II. Solid-state transformer model and modulation strategies

A. Solid-state transformer model

This work is based on the solid-state transformer shown in Fig. 1. The two AC side H-bridges are switching at 150 Hz and have a very low impact on the conducted emission generation compared to the isolated DC-DC converter switching at 2 kHz. In addition to the switching frequency, the common-mode current is dominant on the isolated DC-DC converter due to the parasitic capacitance of the transformer. Therefore, this system is simplified to Fig. 2 to analyse the conducted emissions.

The main sources of conducted emissions in SST must be identified and considered in the system model to analyse (measure) the emissions being conducted. The dominant sources of EMI are the parasitic capacitances from the switching device to the chassis and the transformer windings. The simplified SST circuit model shown in Fig. 2 is used to analyse the impact of the modulation techniques on the conducted emissions. CISPR band B LISN (150 kHz - 30 MHz) is used to measure the CM and differential mode (DM) emissions to compare the results with the emission limits of the IEC 62041-2020 standard. A similar model with CISPR band A LISN (9 kHz - 150 kHz), is presented in [14].

DM noise is not the main source of EMI because the current path through the positive and neutral lines has the same magnitude but opposite direction (blue arrow in Fig. 2), which will cancel each other out. However, the CM current flows (red arrow in Fig. 2), in the same direction in the positive and neutral lines of the same magnitude, which will be added together to generate more EMI. DM and CM voltages are obtained using (1) and (2), respectively. Similarly, the CM and DM currents through the LISN are measured in the 50 Ω resistances of the positive and neutral lines.

$$V_{\mathrm{DM}} = \frac{V_1 - V_2}{2} \tag{1}$$

$$V_{\mathrm{CM}} = \frac{V_1 + V_2}{2} \tag{2}$$

V_1 and V_2 are the noise voltages across the positive and neutral lines, respectively.

The snubber capacitor, C_{sb}, in Fig. 2 is designed to operate the DC-DC converter in a soft-switching

mode [15]. This soft-switching technique helps to reduce switching losses and creates a smooth transition during the switching states of the IGBT. The impact of soft-switching on conducted emission is explained in [14].

B. Solid-state transformer modulation techniques and their impact on conducted emission

The four commonly used modulation techniques for SST are single phase shift, SPS, (no inner phase shift on both sides, $\phi 1 = \phi 2 = 0$, Fig. 3a), extended phase shift, EPS, (only one inner phase shift, either $\phi 1 = 0$ or $\phi 2 = 0$, Fig. 3b), double phase shift, DPS, (the two inner phase shifts are equal, $\phi 1 = \phi 2 \neq 0$, Fig. 3c), and triple phase shift, TPS, (the two inner phase shifts are not equal, $\phi 1 \neq \phi 2 \neq 0$, Fig. 3d). A phase shift, ϕ, is applied between the left and right side half-bridges of the isolated DC-DC converter to have bidirectional power transfer in the SST.

Let us now analyse the impact of each modulation strategy on conducted emissions. This work focuses on CM emission analysis and mitigation because the main aim is to analyse the effect of dV/dt at each switching state for all modulation techniques.

Fig. 3a, shows the switching state of the upper switches of the primary-side (s_1, s_3) and the secondary-side (s_5, s_7) half-bridges for SPS modulation. The waveforms for lower switches are not shown here for simplicity because they complement the upper switches. Since there is no inner phase shift between the upper switches of the half-bridges, the diagonal switches will be conducted at a time. That is, s_1 and s_4 or s_3 and s_2 for the half-bridge of the primary side and s_5 and s_8 or s_7 and s_6 for the half-bridge of the secondary side. The voltage across legs A and B, V_{AB}, and legs Y and Z, V_{YZ}, are square waves with three voltage levels.

Fig. 3b, shows the switching state of the upper switches and the voltages across the legs of the half-bridges for EPS modulation. SPS is extended to the EPS by adding an inner phase shift between the upper switches of the half-bridge to control the circulating current. The inner phase shift is applied only to one side of the transformer with higher voltage.

Fig. 3c and Fig. 3d, show the switching state of the upper switches and the voltages across the legs of the half-bridges for DPS and TPS modulations. The inner phase shift is applied on both sides of the transformer to reduce the circulating currents. Instead of having the same ϕ_1 and ϕ_2 as DPS, TPS have different inner-phase shifts. TPS has more degrees of freedom because the power transfer can be controlled by independently varying the inner and outer phase shifts of the primary

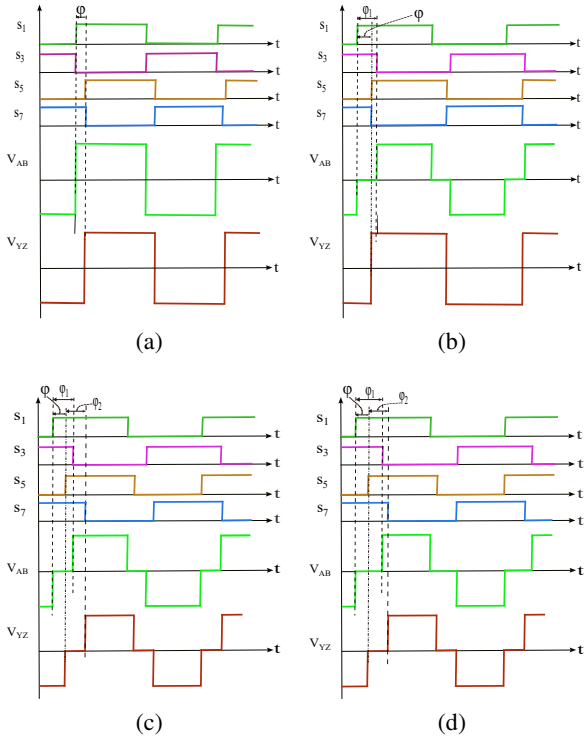


Fig. 3: SST modulation techniques: (a). SPS, (b). EPS, (c). DPS, (d). TPS.

and secondary side half-bridges. This degree of freedom helps to reduce (eliminate) the circulating current which reduces the reactive power to improve the system's efficiency [16].

One of the main sources of common-mode emission for SST is the switching devices' high dV/dt value. Therefore, this work focuses on dV/dt reduction analyses using modulation and multiple SST configuration techniques. The current paths of the SST primary side converter and the switching state using SPS modulation are shown in Fig. 4. There are four switching sequences for SPS modulation [17]. Only two switching sequences are shown in Fig. 4, MFT stands for medium frequency transformer. The diagonal switches with complementary dV/dt will be conducted together; see Fig. 3a. Hence, the common-mode current through C_{p1} of leg A and B will be zero (ideally), if both parasitic capacitances are equal and if there is no part-to-part skew difference between the diagonal switches during switching. However, it's impossible to have perfect dV/dt cancellation due to the mismatch between parasitic capacitances and gate drive part-to-part skew differences.

Unlike SPS, the diagonal switches with complementary dV/dt will not be conducting together for the other modulation techniques (EPS, DPS, TPS) due to the inner phase shift between the conducting switches. Therefore,

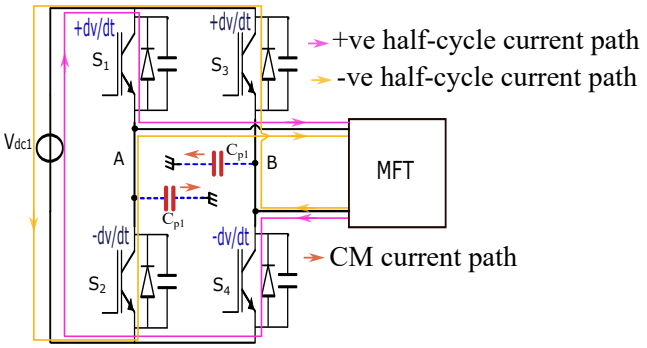


Fig. 4: Current paths for the SST primary side converter using SPS modulation.

there is no dV/dt cancellation during switching. By introducing an internal phase shift, two upper or lower switches operate simultaneously to eliminate reactive power, as illustrated in Fig. 3b - EPS, Fig. 3c - DPS and Fig. 3d - TPS. The results and discussion section explains the analysis of the current flowing through the transformer interwinding parasitic capacitances and the common-mode emissions measured by the LISN.

III. Multiple SST configuration techniques for better EMI reduction

As described in the previous section, only SPS modulation provides dV/dt cancellation. SPS gives the lowest common-mode emission with the highest reactive power, and TPS gives the highest common-mode emission and the lowest reactive power. We now extend this principle to reduce the common-mode emission by adjusting the configuration of multiple SSTs to have a dV/dt cancellation ability and to reduce the reactive power using TPS modulation. The best way to reduce the CM noise for any configuration is to use SPS modulation but with the highest reactive power. Therefore, it is a trade-off between CM emission and efficiency. Since the application of this work is for a railway that is sensitive to EMI due to complexity and dynamic systems, a method with better EMI reduction and less efficiency is preferred over a noisy efficient system. Depending on the configurations of the multiple converters, the CM noise will be different [18].

Two cases are shown in Fig. 5a and Fig. 5c. The first configuration aims to connect two SSTs in parallel using TPS modulation to eliminate reactive power. In addition, the second SST is shifted by half of the switching period to produce complementary switching with the first SST and cancel the dV/dt of the system. The voltages across legs A and B for the first SST and between legs A' and B' for the second SST are shown in Fig. 5b. The waveforms of V_{AB} and $V_{A'B'}$ have a complementary dV/dt during

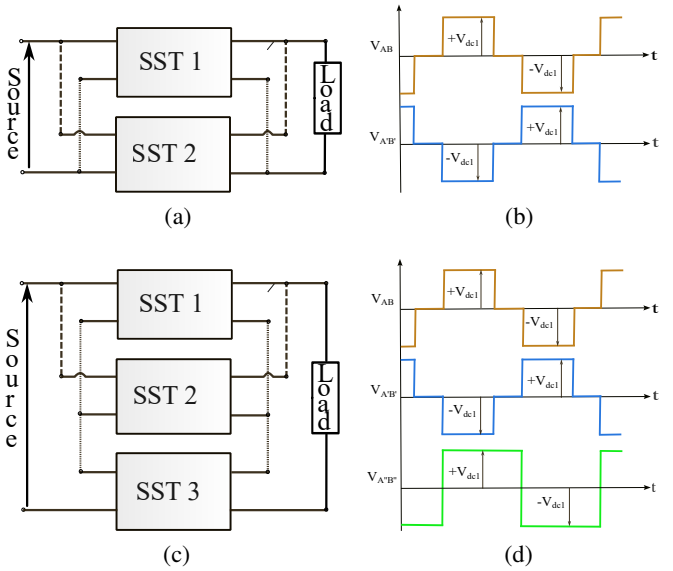


Fig. 5: Multiple SST configuration and modulation options: (a). Two SSTs connected in parallel. (b). TPS modulation for both SSTs of (a). (c). Two SSTs are connected in parallel and one SST is in series. (d). Two SSTs connected in parallel using TPS modulation and one SST in series with SPS modulation for (c).

switching. Therefore, the overall common-mode current will be small due to the dV/dt cancellation. Depending on the application, it is possible to connect several SST pairs with dV/dt cancellation ability in parallel and then in series with the other pairs to increase the voltage or connect all of them in parallel to increase the current if there are even numbers of SSTs.

If there are an odd number of SSTs, Fig. 5c, common mode emissions and reactive power can be reduced by connecting the pairs in parallel to have dV/dt cancellation with TPS modulation and the other SST in series or parallel with SPS modulation. Using this strategy, it is possible to reduce the CM emission and improve the efficiency of the system. The complement of dV/dt during switching for SST 1 and SST 2 is shown in the transformer voltage waveforms in Fig. 5d. Where $V_{A''B''}$ is the voltage between legs A and B of the third SST. The impact of these configurations on conducted emissions is presented in the results and discussion section.

The design parameters for the SST circuit, Fig. 2, are given in Table I taken from [13] except the parasitic capacitances of the transformer. The parasitic capacitances of the transformer are obtained by measuring the setup of [13] using Keysight Agilent E4990a Impedance Analyzer.

TABLE I: Design parameters.

Parameters	Value	Unit
Voltage source, V_{dc1}	1100	V
Switching frequency	2	kHz
Transformer rated power	25	kVA
Leakage inductance, L_δ	0.48	mH
Winding resistance, R_δ	150	mΩ
Transformer ratio	76:76	
Load resistance, R_{load}	48	Ω
Phase shift angle (ϕ)	7.54	degree
Dead time	2.5	μs
Duty cycle	50	%
DC-link capacitors, C_i = C_o	3.1	mF
Snubber capacitor, C_{sb}	4.7	nF
Capacitance, C_{p1}, C_{p2}, C_{p3}	70, 120, 20	pF
Capacitance, $C_{pp'}$, $C_{ss'}$	1.2, 0.9	nF
Inter-winding capacitance, C_{ps}	0.316	nF

IV. Results and Discussion

To analyse the impact of the modulations on the conducted emission: an inner phase shift, $\phi_1 = 5^\circ$ is applied on the primary side of the SST for EPS, on both sides of the SST for DPS, $\phi_1 = \phi_2 = 5^\circ$, and TPS, $\phi_1 = 9^\circ$, $\phi_2 = 5^\circ$ and simulated using the Qorvo QSPICE simulator. The simulation results for the transformer voltages and the current through the transformer interwinding parasitic capacitances are shown in Fig. 6.

As shown in Fig. 6a, both the primary (V_p) and secondary (V_s) side voltages have four for SPS and six for EPS switching events in a single period. Due to the dV/dt at each switching event, unwanted current flows through the transformer inter-winding parasitic capacitor, Fig. 6b. Similarly for DPS and TPS which have eight switching events, Fig. 6c, and the unwanted current that flows through the transformer inter-winding parasitic capacitor is shown in Fig. 6d. As shown in Fig. 6b and Fig. 6d, current flows through the transformer inter-winding capacitor only during the switching event. Therefore, this unwanted current can be reduced by using a dV/dt cancellation technique during switching.

The total CM current (voltage) and DM current (voltage) are measured using LISNs in the CISPR band A and B frequency ranges. The results in the next section are measured using the CISPR band B because there is no EMC standard for power transformers in the CISPR band A frequency range. The CM current (I_{cm}), in time domain, measured by LISN is shown in Fig. 7. The common-mode current is almost zero for SPS because it provides a dV/dt cancellation. Due to parasitic capacitance mismatches and part-to-part skew of gate-drives, there is no perfect dV/dt cancellation. The other modulation techniques have a high common-mode

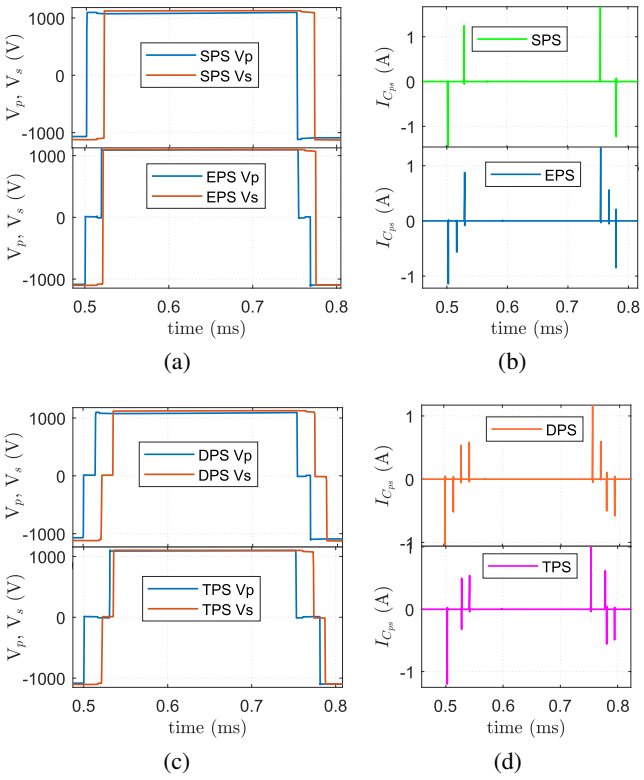


Fig. 6: Transformer voltages and inter-winding current: (a). Voltage for SPS and EPS, (b). Current for SPS and EPS, (c). Voltage for DPS and TPS, (d). Current for DPS and TPS

current because they do not have dV/dt cancellation capability.

The EMC requirements for emission and immunity within the frequency range 0 Hz to 400 GHz for power transformers, power supply units, reactors, and similar products are given by IEC 62041: 2020 and IEC 61000-6-4-2019. The SST is categorised under the power transformers and must have an emission level below the limits given in these standards to be implemented in a railway traction supply system. The emission limits in Table II are used to compare the conducted emissions of the SST for each modulation technique.

TABLE II: IEC 62041:2020 conducted emission limits.

Frequency band (MHz)	Emission limits dB(μV)
0.15 – 0.5	89, quasi-peak 76, average
0.5 – 30	83, quasi-peak 70, average

The CM voltage measured by the LISN, in the frequency domain, is shown in Fig. 8a for each modulation strategy. This figure shows that the CM emission is below the limits only for SPS because of the dV/dt

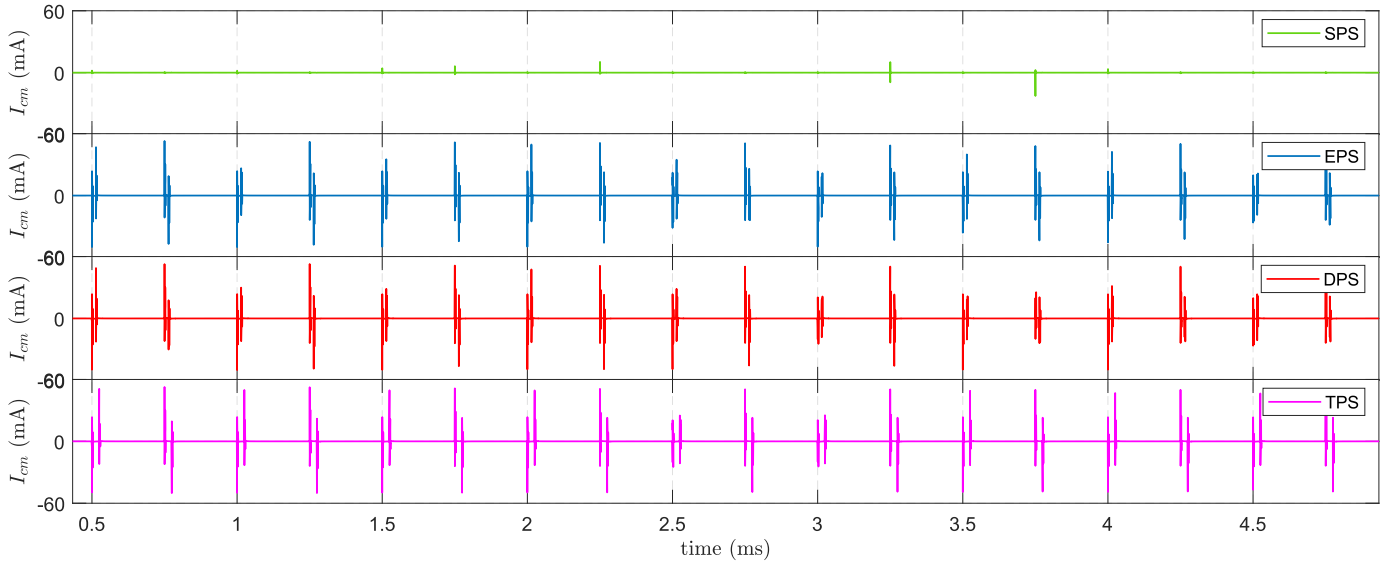
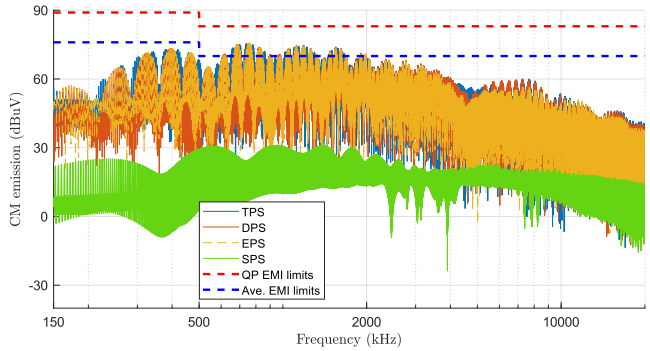
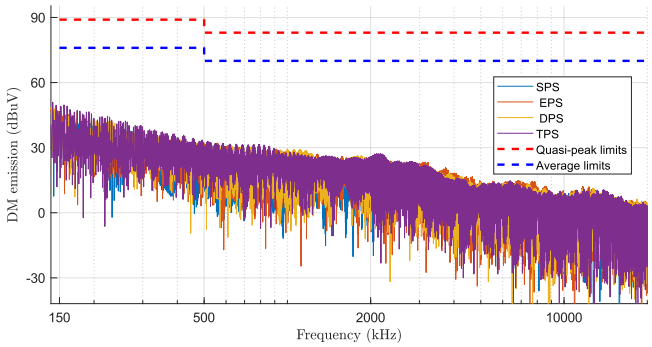


Fig. 7: CM current measured by LISN for single SST.



(a) CM



(b) DM

Fig. 8: Conducted emissions measured by LISN for single SST.

cancellation. The other modulations generate a CM emission above the limits. Therefore, it is possible to reduce the CM emission below the limits using SPS without adding a filter. Meanwhile, an additional CM mitigation technique must be applied for the other modulation techniques to reduce emissions below the limits.

The DM voltage measured by the LISN shown in Fig. 8b for each modulation strategy is below the limits specified in the standard. This is because the DM current through the positive and neutral lines has the same magnitude but flows in opposite directions. This is why it is important to focus on mitigating CM emission instead of DM.

The total power transfer using SPS and TPS modulation techniques for 10 Ω load is given in Fig. 9. Due to the circulating current, the SPS has high reactive power while it is possible to minimize this reactive power by adjusting the inner and outer phase shifts of the TPS modulation.

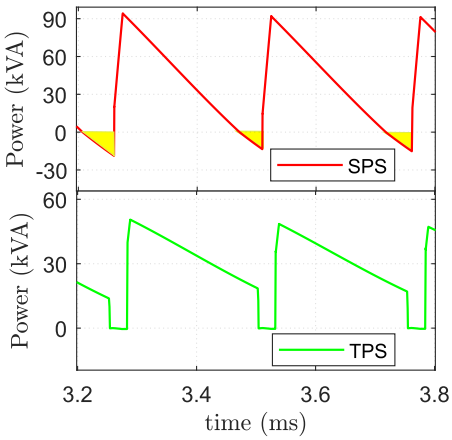


Fig. 9: Total power transfer using SPS and TPS modulations.

The comparison of CM and DM voltages measured by CISPR band B LISN for single and multiple SSTs with different configurations and modulation techniques are shown in Fig. 10 and Fig. 11. The CM emission

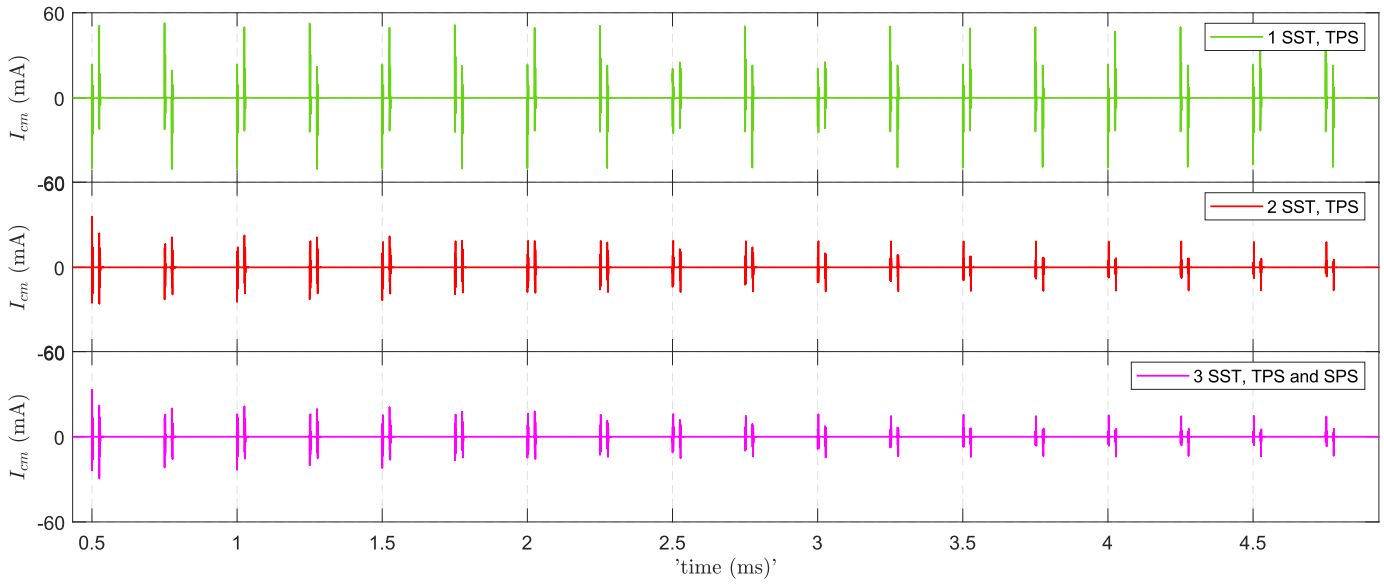
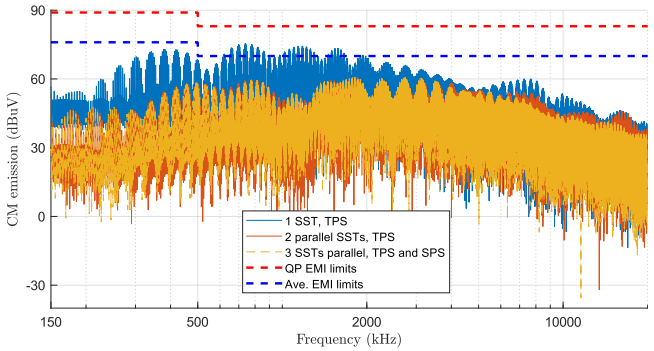
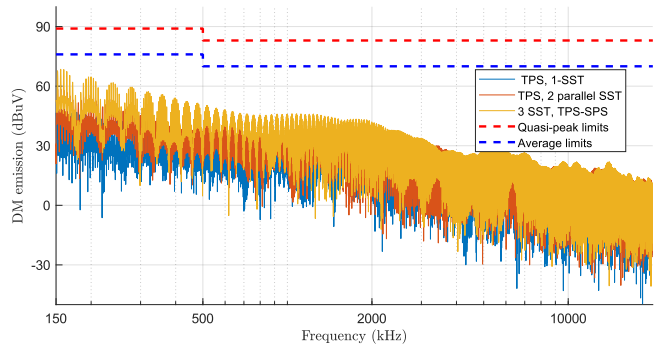


Fig. 10: CM current measured by LISN for multiple SST.



(a) CM



(b) DM

Fig. 11: Conducted emissions measured by LISN for multiple SST

for the configurations given in Fig. 5a and Fig. 5c is shown in Fig. 10, time domain, and Fig. 11a, Fast Fourier Transform (FFT). The CM emissions for such configurations are below the limits whereas, the single SST with TPS modulation produces CM emissions above the limits. DM emission for all types of SST configurations is below the emission limits of the standard, as shown in Fig. 11b. Therefore, the main component of the conducted emission is the common mode.

The common-mode current measured by the LISN in the time domain for multiple SSTs is shown in Fig. 10. The common-mode current of multiple SSTs with dV/dt cancellation capability is very low compared with the single SST with the same modulation technique. The conclusion is that both CM emission and reactive power can be improved using proper configurations and modulation techniques. In this way, there is no need to have additional external components for EMI mitigation such as EMI filters.

The experimental setup is shown in Fig. 12. The three SSTs and LISNs are connected to a common ground plane. Copper brackets are used in place of wires to connect the LISNs to the ground plane to minimize the equivalent series inductance. The time and frequency domains are measured using an oscilloscope and an EMI test receiver.

V. Conclusion

This paper explains the impact of different solid-state transformer modulations and multiple configuration techniques on the conducted emission. The selection of modulation technique is a trade-off between improving the conducted emission and the reactive power of the SST because each modulation can not improve both the EMI and the reactive power simultaneously. The SPS modulation has the lowest CM emission and highest reactive power while TPs have the worst CM emission and

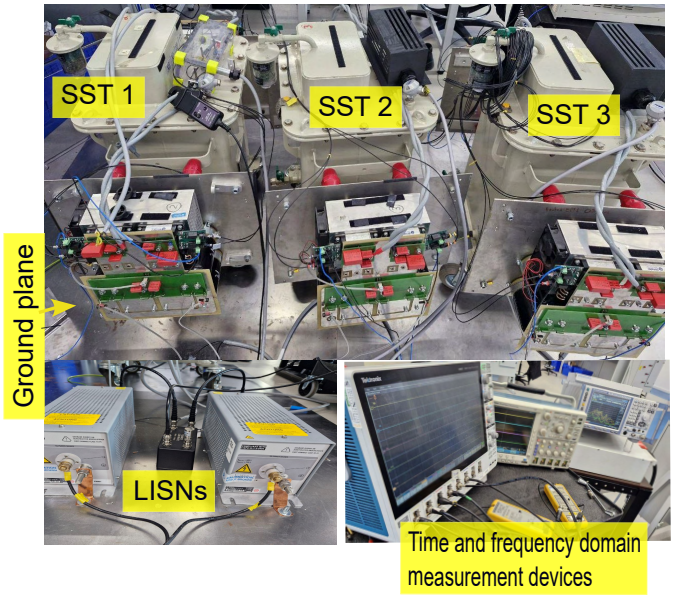


Fig. 12: Experimental setup.

lowest reactive power compared to the other modulation strategies. While EPS, DPS and TPS have a CM emission above the IEC 62041:2020 conducted emission limits, SPS generates CM emission below the limits.

The CM emission and reactive power can be improved by configuring two SSTs in parallel with dV/dt cancellation capability using TPS, for an even number of SSTs, and then series or parallel connection with SPS, for an odd number of SSTs. The design and analysis of CM choke for the mitigation of conducted EMI in a multicell SST will be the future work of this study.

REFERENCES

[1] F. Iov, F. Blaabjerg, J. Clare, P. Wheeler, A. Rufer, and A. Hyde, "Uniflex-pm–a key-enabling technology for future european electricity networks," *Epe Journal*, vol. 19, no. 4, pp. 6–16, 2009.

[2] D. Han, S. Li, Y. Wu, W. Choi, and B. Sarlioglu, "Comparative analysis on conducted cm emi emission of motor drives: Wbg versus si devices," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8353–8363, 2017.

[3] C. W. Mclyman, "Winding capacitance and leakage inductance," 2011.

[4] H. Wen, W. Xiao, and B. Su, "Nonactive power loss minimization in a bidirectional isolated dc–dc converter for distributed power systems," *iEEE Transactions on industrial Electronics*, vol. 61, no. 12, pp. 6822–6831, 2014.

[5] S. Shao, M. Jiang, W. Ye, Y. Li, J. Zhang, and K. Sheng, "Optimal phase-shift control to minimize reactive power for a dual active bridge dc–dc converter," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 10 193–10 205, 2019.

[6] Z. Guo, "Modulation scheme of dual active bridge converter for seamless transitions in multiworking modes compromising zvs and conduction loss," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 9, pp. 7399–7409, 2019.

[7] G. Xu, L. Li, X. Chen, Y. Liu, Y. Sun, and M. Su, "Optimized eps control to achieve full load range zvs with seamless transition for dual active bridge converters," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 9, pp. 8379–8390, 2020.

[8] G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation strategy to operate the dual active bridge dc-dc converter under soft switching in the whole operating range," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1228–1236, 2010.

[9] Y. Yan, Y. Huang, R. Chen, and H. Bai, "Building common-mode analytical model for dual active bridge incorporating with different modulation strategies," *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12 608–12 619, 2021.

[10] S. Kumar, S. K. Voruganti, B. Akin, and G. Gohil, "Common-mode current analysis and cancellation technique for dual active bridge converter based dc system," *IEEE Transactions on Industry Applications*, vol. 58, no. 4, pp. 4955–4966, 2022.

[11] F. Salomez, H. Pichon, Y. Lembeye, and J.-C. Crébier, "Pwm strategy for the cancellation of the common mode noise generated in a multi-cell dc-ac converter," *IEEE Transactions on Power Electronics*, 2024.

[12] X. Zhao, Z. Wang, D. Jiang, and Z. Liu, "Common-mode voltage analysis and suppression strategy for three-level dual-active-bridge converter," *IEEE Transactions on Power Electronics*, 2024.

[13] A. J. Watson, G. Mondal, H. Dang, P. W. Wheeler, and J. C. Clare, "Construction and testing of the 3.3 kv, 300 kva uniflex-pm prototype," *EPE Journal*, vol. 19, no. 4, pp. 59–64, 2009.

[14] H. H. Adhena, A. J. Watson, S. Greedy, N. Moonen, and F. Leferink, "Analysis of conducted emi for dual active bridge dc-dc converter in an electric traction application," in *13th International Conference on Power Electronics, Machines and Drives (PEMD 2024)*. IET, 2024, pp. 423 – 429.

[15] D. Siemaszko, F. Zurkinden, L. Fleischli, I. Villar, Y. R. De Novaes, and A. Rufer, "Description and efficiency comparison of two 25 kva dc/ac isolation modules," *EPE Journal*, vol. 19, no. 4, pp. 17–24, 2009.

[16] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional dc–dc converter for high-frequency-link power-conversion system," *IEEE Transactions on power electronics*, vol. 29, no. 8, pp. 4091–4106, 2013.

[17] H. Ramakrishnan, "Bi-directional, dual active bridge reference design for level 3 electric vehicle charging stations," *Syst. Eng. Texas Instruments, India*, 2019.

[18] C. E. Feloups, H. H. Adhena, N. Moonen, D. Thomas, and F. Leferink, "Investigating the cm noise generated by different configurations of multiple forward converters," in *2023 International Symposium on Electromagnetic Compatibility–EMC Europe*. IEEE, 2023, pp. 1–6.