Second-Carrier Harmonic Cancellation for a DC Bus Fed by Multiple Dual Active Bridges in More Electric Aircraft Applications

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***Abstract*—This paper develops a mechanism to suppress second carrier harmonics on a common DC bus fed by multiple dual-active bridge (DAB) converters. A mathematical model of dc-link current harmonic components of a DAB is derived. Using this model, it is found that the magnitude and the phase angle of the second carrier harmonic are mainly determined by the phase shift ratio of the DAB converter. Based on this conclusion, a harmonic suppression control scheme has been developed to manage the phase shifts in carrier waves of the two converters. To mitigate the impacts of differences in leakage inductances, voltage source types and levels, an enhanced harmonic cancellation scheme has been developed using an extra control loop to coordinate the duty cycles between DABs to achieve entire harmonic cancellation in general cases. The proposed method demonstrates a significant reduction of second carrier harmonics and has been validated in both simulation and experiment results.**

***Index Terms*—Dual active bridge converter, cancellation method, capacitors, second carrier harmonic.**

I. INTRODUCTION

THE dual-active bridge (DAB) is an appealing topology that has gained significant attention in recent years[1], [2], [3], [4]. It has been widely used in various transportation applications, such as more-electric aircraft (MEA) or all-electric aircraft (AEA), etc. It serves as an interface for power transfer between different power sources and loads with a high voltage conversion gain and galvanic isolation. With the increased power demands on aircraft, multiple converters are connected in series or parallel as a new system. For MEA applications, a typical output parallel-connected system is shown in Fig. 1, where multiple DABs are connected to independent batteries to achieve the required power and redundancy requirements. Although it increases the power rating of the system, the power quality of the DC bus might be of concern. The power switches in the converter turn on and off periodically and produce current ripples on the DC-link bus [5]. In order to suppress the dc-link harmonics, one of the most widely used methods is adding a large dc-link capacitor. However, capacitors are bulky and expensive, which means the overall system compromises in terms of weight, volume, and cost[6], [7]. Aircraft applications are sensitive to this. Apart from that, the harmonics in dc-link transferred from the capacitor to other passive components, causing more power loss and reducing the lifetime of capacitors [8]. Minimizing the harmonics of DC-bus currents can potentially reduce the size of the capacitor. The suppression of harmonics can further improve the ripple performance and power quality. Meanwhile, another benefit gained from harmonic suppression is increased capacitor lifetime, which is important to system reliability.

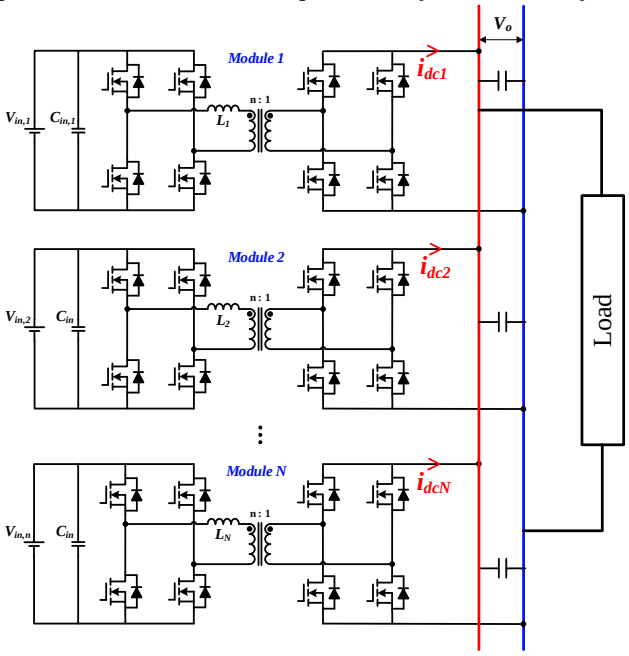


Fig. 1. Multi-source output parallel DAB converter system

There are many methods proposed to reduce the dc-link harmonics. Papers [9] and [10] mainly focus on harmonics produced by a three three-phase voltage source converter. [11], [12], [13] mainly focus on harmonics produced by inverter. [14] and [15] mainly focus on harmonic suppression in motor drive systems. For the DAB converter system, many researchers have investigated these problems. In [16], a dual-inductor connected DAB converter is proposed to reduce the current harmonics. This topology is a current source type DAB converter with inductors (current filters) connected to both the input and output ports to reduce the current harmonic. However, additional

magnetic components will increase the system's volume, weight, and cost. Meanwhile, it mainly focuses on the working principle and control scheme but there is less analysis on harmonic active suppression. In [17], an active suppression of DC harmonics for the DAB converter method is proposed. The idea is to introduce an internal phase shift at the primary and secondary bridges. A detailed current harmonic calculation in the inductor and input port is analysed in this paper. However, the suppression of particular harmonics can constrain the power transfer capability and do not include multi-converter systems. In [18], the multi-level structure of the DAB converter is proposed. This method is based on the modular multilevel converter (MMC) to increase the voltage level of the bridge. The output current harmonic is suppressed by reducing the voltage harmonics in high-frequency AC links. However, this method focuses on the topology analysis and the control scheme since they are very complicated. In [19], [20], an interleaved structure of DAB converter is proposed to reduce the harmonic. Compared to the multi-level converter, the interleaved structure is simpler. However, the interleaved angle of each converter in these papers is directly given as a constant and there is no output current harmonic analysis. And the performance of these methods is limited when facing the problems of parameter mismatch.

In [21] and [22], a new harmonic suppression method in MEA application is proposed. A buck-boost converter is used to balance the harmonics produced by a three-phase PWM converter for the MEA power system in [21], and two three-phase PWM converters are implemented to eliminate harmonic in [22]. The main idea is to use another converter to compensate for the harmonic of each other. Since the harmonic components can't be eliminated through modifying topology and modulation, this idea is a better solution to address this problem.

Inspired by this, a harmonic suppression method for second carrier harmonics on the capacitor in a two-DAB converter system is developed in this article. The proposed method does not modify the basic working principle for a DAB converter and is based on the interleaved structure. This approach offers a range of improvements and introduces fresh perspectives, outlined below:

1) A detailed analysis of the output current harmonics of the DAB converter is proposed in the paper, which gives a clear view of the characteristics of the harmonics.
2) Based on the mathematical model of harmonics, the phase angle between different converters is actively changed according to the environment. This scheme has a better performance when facing the problems of parameter mismatch. In addition, this scheme can also be applied to other DC converters in the bus.

To better show the performance of the different methods, a comparison table is summarized as shown in Table I. The symbol "+" represents the degree of each assessment. The proposed method has good performance without increasing the system's complexity and has a wide range of applications.

TABLE I
COMPARISON BETWEEN DIFFERENT METHODS

	Complexity	Performance	Range of applications
[16]	+++	+++	+
[17]	++	++	+++
[18]	++++	++++	+
[19],[20]	+	+++	+++
Proposed	++	++++	++++

The rest of the paper is organized as follows: the basic principles for DAB converter and DC harmonic analysis are introduced in Section II. The calculation process of DC-link harmonic current is detailed. With the proposed harmonic model, a new method to minimize the second carrier harmonic is proposed in Section III. With the proposed method, a significant minimization in second carrier harmonic can be achieved in different power sharing ratios. Finally, the proposed method has been validated by simulation and experiments in Section IV.

II. SPS MODULATION FOR DAB CONVERTERS

A. Leakage inductor current i_L for DABs with SPS Control

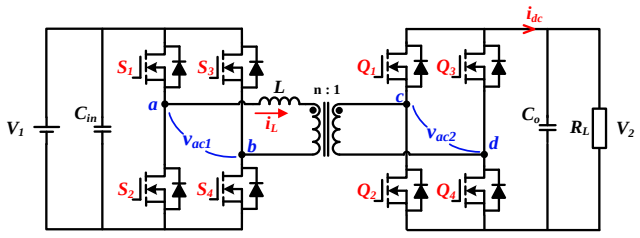


Fig. 2. Topology of a DAB converter

In order to develop a mechanism to suppress harmonics at the DC bus, it is essential to analyse the details of current harmonics within one DAB. The topology of a commonly used DAB converter is shown in Fig. 2. It is composed of two symmetrical H-bridges. They are connected through a high-frequency transformer. The transformer can be regarded as an ideal transformer and a leakage inductance L. The transformer turns ratio is defined as n. Each bridge consists of four power switches (S_1-S_4 and Q_1-Q_4). The input DC voltage is noted as V_1, and the output voltage is noted as V_2. The output voltage of the primary bridge is noted as v_{ac1}, and the second bridge is noted as v_{ac2}. Furthermore, two bridges are connected through a high-frequency transformer. The output current before the output capacitor is noted as i_{dc}.

For a single DAB converter, phase-shift modulation techniques are commonly used for its power flow control. Among these phase shift modulation methods, the single-phase shift (SPS) stands as the most widely used one [23]. In this paper, we thus only focus on DABs using SPS modulation

techniques. The basic operation modes in SPS are shown in Fig. 3, where D refers to the phase shift ratio between the primary side and secondary side AC voltages (i.e. v_{ac1} and v_{ac2}, it is also equal to the phase angle between switching functions of S_1 and Q_1). We also define that the maximum phase shift is $T_s/2$ and the range of phase shift ratio D is of a range [0, 1]. The phase shift angle θ_c (carrier phase angle) is defined as the phase shift of the rising edge of S_1&S_4 with the reference t = 0 axis as shown in Fig. 3.

Assuming that the DAB converter in Fig. 2 is ideal, the current across the transformer leakage inductance L can be expressed as

$$\frac{di_L(t)}{dt} = \frac{v_{ac1}(t) - nv_{ac2}(t)}{L} \tag{1}$$

where $v_{ac1}(t)$ represents the terminal voltage at the primary side of the transformer, $v_{ac2}(t)$ represents the terminal voltage of the secondary side.

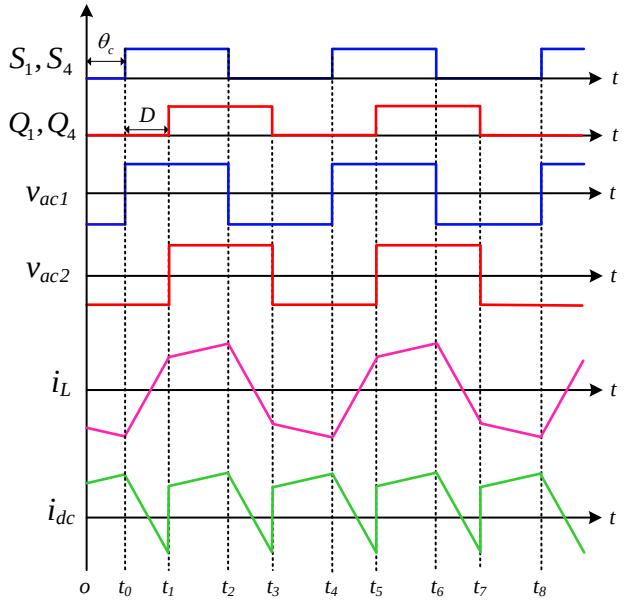


Fig. 3. Switching status, current, and voltage waveforms in SPS control.

Suppose that the inductor current at t_0 is $i_L(t_0)$, the current at time instant t_1, t_2, t_3 and t_4, shown in Fig. 3 can be written as

$$i_L(t_1) = i_L(t_0) + \frac{V_1 + nV_2}{L} \cdot \frac{D}{2f} \tag{2}$$

$$i_L(t_2) = i_L(t_1) + \frac{V_1 - nV_2}{L} \cdot \frac{(1-D)}{2f} \tag{3}$$

$$i_L(t_3) = -i_L(t_1) \tag{4}$$

$$i_L(t_4) = i_L(t_0) = -i_L(t_2) \tag{5}$$

where f is the switching frequency. Solving equations (2) to (5), the inductor current at the time t_0 and t_1 can be derived as

$$i_L(t_0) = \frac{1}{4fL} \cdot \left[-V_1 + (1-2D)nV_2\right] \tag{6}$$

$$i_L(t_1) = \frac{1}{4fL} \cdot \left[(2D-1)V_1 + nV_2\right] \tag{7}$$

Thus, the inductor current at any time instant in one switching cycle is defined and can be given as

$$i_L(t) = \begin{cases} \frac{1}{4fL} \cdot \left[-V_1 + (1-2D)nV_2\right] + \frac{(V_1 + nV_2)}{L} \cdot t, 0 < t < \frac{D}{2f} \\ \frac{1}{4fL} \cdot \left[-V_1 + (1+2D)nV_2\right] + \frac{(V_1 - nV_2)}{L} \cdot t, \frac{D}{2f} < t < \frac{1}{2f} \\ \frac{1}{4fL} \cdot \left[3V_1 + (2D+1)nV_2\right] + \frac{(-V_1 - nV_2)}{L} t, \frac{1}{2f} < t < \frac{1+D}{2f} \\ \frac{1}{4fL} \cdot \left[3V_1 + (-3-2D)nV_2\right] + \frac{(-V_1 + nV_2)}{L} \cdot t, \frac{1+D}{2f} < t < \frac{1}{f} \end{cases} \tag{8}$$

B. Mathematical Analysis of DC Current Harmonic of DAB converter

With the derived explicit expression of $i_L(t)$, we can identify the DC current i_{dc} using the relationship between the leakage inductance current i_L and the dc-link current i_{dc}. This can be derived from the inductor current and the switching states on the secondary side.

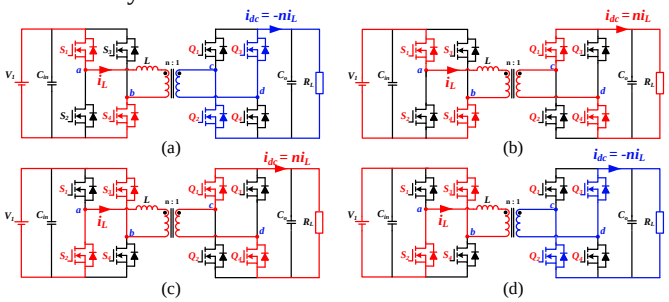


Fig. 4 The relationship between inductor current and DC bus current. (a) time interval [t_0, t_1], (b) time interval [t_1, t_2], (c) time interval [t_2, t_3], (a) time interval [t_3, t_4]

At interval $t_0 \sim t_1$, from Fig. 3, the primary switch S_1, S_4, and the secondary switch Q_2, Q_3 are closed. The output current direction is opposite to that of the inductor current as shown in Fig. 4(a), thus the current $i_{dc} = -ni_L$. Similar analysis can be done for the other time intervals as shown in Fig. 4(a) ~ Fig. 4(d) and is summarised in Table II. Based on this analysis, the

TABLE II RELATION BETWEEN CURRENT I_{DC} AND I_L AT DIFFERENT TIME INTERVALS

Time interval	Switching status	DC current i_{dc}
[t_0, t_1]	S_1, S_4, Q_2, Q_3 on	$i_{dc} = -n\ i_L$
[t_1, t_2]	S_1, S_4, Q_1, Q_4 on	$i_{dc} = n\ i_L$
[t_2, t_3]	S_2, S_3, Q_1, Q_4 on	$i_{dc} = n\ i_L$
[t_3, t_4]	S_2, S_3, Q_2, Q_3 on	$i_{dc} = -n\ i_L$

the direction of the output current i_{dc} and i_L will be in the same direction when Q_1 and Q_4 are open. These two currents will be in opposite directions when Q_2 and Q_3 are open. From Fig. 3, it can be seen that the frequency of output current i_{dc} is twice the switching frequency. To simplify the analysis of the phase of the harmonic, the start of one cycle of output current is defined as t_1 and the end of one cycle is defined as t_3. Then, the current $i_{dc}(t)$ in one cycle is given as

$$i_{dc}(t)=\begin{cases}\dfrac{1}{4fL}\cdot\left[(2D-1)V_1+nV_2\right]+\dfrac{(V_1-nV_2)}{L}\cdot t, 0<t<\dfrac{(1-D)}{2f}\\ \dfrac{1}{4fL}\cdot\left[(3-2D)V_1+nV_2\right]+\dfrac{(-V_1-nV_2)}{L}\cdot t, \dfrac{(1-D)}{2f}<t<\dfrac{1}{2f}\end{cases} \quad (9)$$

Using Fourier expansion, the current $i_{dc}(t)$ can be expressed as

$$i_{dc}(t)=I_0+\sum_{k=1}^{\infty}I_k\cos[2k\pi(2f)t+\varphi_k]\ ,\ k=1,2,...,\infty \quad (10)$$

where I_0 is the DC component of the output current. φ_k is the phase angle of the k-th order DC-bus harmonics. The magnitude expression is

$$I_k=\sqrt{a_k{}^2+b_k{}^2} \quad (11)$$

$$a_k=\frac{1}{\pi}\int_0^{\frac{T_s}{2}}i_{dc}(t)\cdot\cos 4k\pi ftdt \quad (12)$$

$$b_k=\frac{1}{\pi}\int_0^{\frac{T_s}{2}}i_{dc}(t)\cdot\sin 4k\pi ftdt \quad (13)$$

Substituting (9) into (12) and (13), the closed-form of Fourier coefficients are

$$\begin{aligned}a_k=&\frac{1}{\pi}\int_0^{(2-2\pi)}\frac{1}{4fL}\cdot\left[(2D-1)V_1+nV_2\right]\cos(kx)+\frac{(V_1-nV_2)}{L}\cdot x\cos(kx)dx\\&+\frac{1}{\pi}\int_{(2-2\pi)}^{2\pi}\frac{1}{4fL}\cdot\left[(3-2D)V_1+nV_2\right]\cos(kx)+\frac{(-V_1-nV_2)}{L}\cdot x\cos(kx)dx\end{aligned} \quad (14)$$

$$\begin{aligned}b_k=&\frac{1}{\pi}\int_0^{(2-2\pi)}\frac{1}{4fL}\cdot\left[(2D-1)V_1+nV_2\right]\sin(kx)+\frac{(V_1-nV_2)}{L}\cdot x\sin(kx)dx\\&+\frac{1}{\pi}\int_{(2-2\pi)}^{2\pi}\frac{1}{4fL}\cdot\left[(3-2D)V_1+nV_2\right]\sin(kx)+\frac{(-V_1-nV_2)}{L}\cdot x\sin(kx)dx\end{aligned} \quad (15)$$

Simplify equation (14) and (15), we have

$$\begin{aligned}a_k=&\frac{1}{k\pi fL}\cdot\left[(D-1)V_1\right]\cdot\sin k(2-2D)\pi-\frac{V_1}{k^2 2\pi^2 fL}\\&+\frac{V_1}{k^2 2\pi^2 fL}\left[\cos k(2-2D)\pi+k(2-2D)\pi\sin k(2-2D)\pi\right]\end{aligned} \quad (16)$$

$$\begin{aligned}b_k=&\frac{1}{k\pi fL}\cdot\left[(1-D)V_1\right]\cdot[\cos k(2-2D)\pi-1]+\frac{(V_1+nV_2)}{2k\pi fL}\\&+\frac{V_1}{2\pi^2k^2fL}\left[\sin k(2-2D)\pi-k(2-2D)\pi\cos k(2-2D)\pi\right]\end{aligned} \quad (17)$$

Based on (16) and (17), the angle of different harmonic of i_{dc} can be calculated. It is noted that the phase angle φ_k is not only determined by the harmonic, but also determined by carrier phase angle θ_c and phase shift D. Thus, the phase angle of the k-th order harmonic is expressed by

$$\varphi_k=2Dk\pi+2k\theta_c+\alpha_k \quad (18)$$

$$\alpha_k=\text{atan2}(-b_k,a_k) \quad (19)$$

For the harmonics phase angle φ_k in (18), the term $2Dk\pi$ means that the phase difference is affected by the phase shift D and the phase of switching signal θ_c. Equation (19) represents the harmonic phase angle with respect to equation (9). Using equations (10) to (19), the magnitude and phase angle of $i_{dc}(t)$ harmonic components can be calculated explicitly. Assuming a DAB is working under the conditions in Table III, different harmonic components within the current $i_{dc}(t)$ can be derived from (10) to (19). The harmonic component magnitudes up to 200kHz with different phase shift D are shown in Fig. 5. As can be seen, the second carrier harmonic of a frequency of $2f$ (40kHz) has the maximum magnitude compared to other harmonic components. Especially when the phase shift closes to 0.5 (maximum power transfer), the magnitude grows quickly and is even larger than the DC component. Thus, in this paper, we will mainly focus on $2f$ harmonic studies.

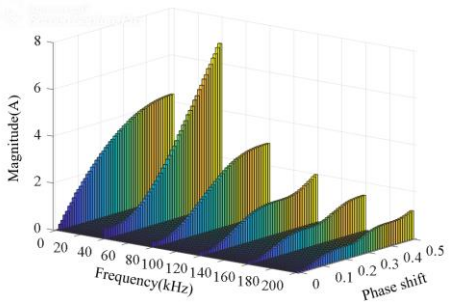


Fig. 5 Relationships of magnitude, frequency, and phase shift.

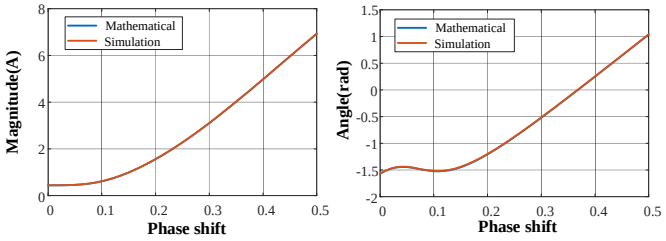
TABLE III CIRCUIT PARAMETERS

Parameters	Value
Input voltage V_1	250 V
Output voltage V_2	270 V
Leakage inductance	L = 360 μH
Switching frequency f	20kHz
Transformer ratio n	1:1

C. Comparison Between Mathematical Model and Circuit Model

To validate the accuracy of our models from equation (10) to (19), a DAB circuit using parameters in Table III has been simulated in a MATLAB/PLECS environment with different phase shifts D implemented. After each simulation, the DC bus current i_{dc} is captured and analysed using the FFT toolbox in MATLAB. Results are compared to our mathematical model (10)-(19) in Fig. 6. As can be seen, the second carrier harmonics results from the mathematical model and the circuit model match very well in both the magnitude and phase of the second

carrier harmonics. Through the above analysis, it can be concluded that the mathematical model is highly accurate to be used to calculate harmonics within the DC bus current i_{dc} in our further studies.



(a) (b)

Fig. 6 Comparison of second carrier harmonic for mathematical model and simulation with increased phase shift. (a)Magnitude, (b) Phase angle.

III. Harmonics Cancellation Scheme Development

In this section, we aim to develop the second carrier harmonic cancellation scheme using a two-parallel DAB system as an example.

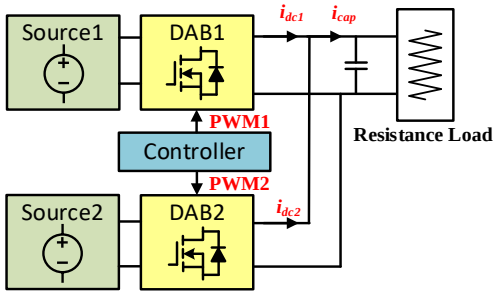


Fig. 7 System diagram.

A. Second carrier harmonic suppression scheme

For harmonic suppression, the technique developed in the paper considers the fact that when two sinusoidal currents flow into one node and these two currents are of the same amplitude and frequency, these two currents will cancel each other (i.e. sum up to zero) if they are of 180° phase shift. From this, to cancel the second harmonics with the same magnitude and frequency from two DABs discussed so far, the phase angle difference of harmonic of the two DABs should be with 180° phase shift. Thus, it requires

$$\varphi_1^{[1]} - \varphi_1^{[2]} = \pi \tag{20}$$

Considering a parallel connected DAB system as shown in Fig. 7 and assuming the two DABs are of the same parameters, i.e. $L_1 = L_2 = L$ and input DC power supplies are of the same voltage level. We also consider that two DABs share the same phase shift $D_1 = D_2 = D$. According to (10) to (17), the magnitude of the harmonic of the two converters is perfectly matched. Based on power equation (21) below, the two DABs also share the same power, which is the most ideal condition.

$$P_o = \frac{nV_{in}V_o}{2Lf} D(1-D) \tag{21}$$

Under this condition, we also have $\alpha_1^{[1]} = \alpha_1^{[2]}$ from (18). Thus, the requirement in (20) becomes

$$\theta_c^{[1]} - \theta_c^{[2]} = \frac{\pi}{2} \tag{22}$$

Equation (22) indicates that, for two identical DABs which are under the same operation conditions, the second carrier harmonics can be eliminated when the modulation signals are in π/2 phase shift.

In practice, the phase shift D of DABs may not always be equal especially when DABs are connected to different types of resources (batteries and fuel cells) or the leakage inductances are not equal. In these cases, the phase shift D of the two DABs may be different to produce the required power. Under these conditions, from (10) to (19), we know that the magnitudes of two converter's harmonic may not be equal in these cases. Thus, the second carrier harmonic will be suppressed but cannot be entirely cancelled. However, using (20) together with (18) and (19), these components can still be suppressed when the two carrier signal phase angles related with

$$\theta_c^{[1]} - \theta_c^{[2]} = (D_2 - D_1 + 0.5)\pi + \frac{\alpha_1^{[2]} - \alpha_1^{[1]}}{2} \tag{23}$$

Equation (23) indicates a way to suppress the second carrier harmonics in a general case when two DAB converters are connected in parallel with different phase shifts. The control loop design for the second carrier harmonic can thus be developed using (16) to (23) as shown in Fig. 8. The outer control loop is for output voltage control, where V_{ref} is the reference voltage, and V_2 is the output voltage. An additional carrier phase angle controller is added to the conventional power control loop for harmonic suppression. The phase shifts can be calculated using (21) with power demand P^* from the PI controller. The power sharing between the two DABs is controlled by the two coefficients K_1 and K_2 with $K_1 + K_2 = 1$. When $K_1 = K_2 = 0.5$, the two DABs share the power requirements equally.

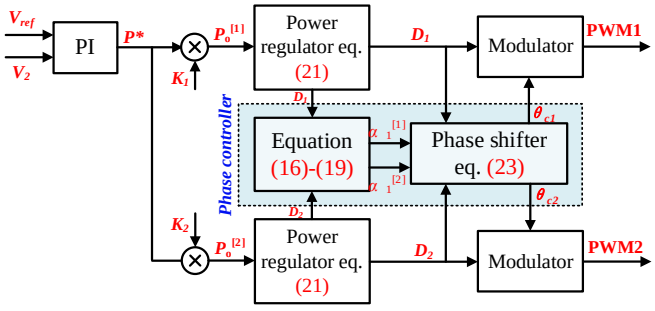


Fig. 8 General second carrier harmonic cancellation method.

To better understand how the proposed method is working, the switching waveform and output current waveform are shown in Fig. 9. S_{11} and S_{41} represent the switches S_1 and S_4 of converter 1. Q_{11} and Q_{41} represent the switches Q_1 and Q_4 of converter 1. S_{12}, S_{42}, Q_{12} and Q_{42} represent the switches S_1, S_4, Q_1 and Q_4 of converter 2, respectively. D_1 and D_2 represent the phase shift of each converter. $\Delta\theta_c$ is the carrier signal phase shift angle, which corresponds to the equation (23). i_{dc1}, i_{dc2} and i_{cap} represent the output current of converter 1, converter 2 and capacitor current, respectively. It can be seen that there is a phase shift between the switching signal of converter 1 and converter 2. The sum of them, the capacitor current, is also different to the original waveform. The capacitor waveform is positive, meaning there is less reactive power in the capacitor. The current ripple of the output current is smaller than the sum of i_{dc1} and i_{dc2}. The frequency of the output current is higher. Thus, the harmonics and voltage ripple are reduced.

The proposed method can be applied in reverse power flow conditions. The working principle of the DAB converter is symmetric. The relationships between phase angle, magnitude and phase shift are the same as normal power flow. The only difference is that the signals of switches S_1-S_4 in this paper are regarded as the base signals switch in normal power flow. The reference of the other switch signals is determined by the base signal. In reverse power flow, the signals of switches Q_1-Q_4 are regarded as the base signals. The other process is the same as normal power flow.

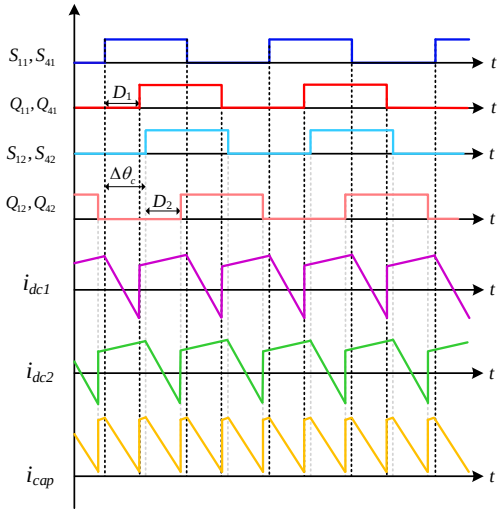


Fig. 9. Critical waveforms of the proposed method.

B. Enhanced second carrier harmonic cancellation scheme

Although (23) gives the way to suppress the second carrier harmonics, to fully cancel such a harmonic in general cases (different power sharing, voltage levels, transformer leakage inductances etc), an advanced adaptive power sharing control scheme needs to be developed. Assuming the power sharing ratio of two converters is K_1 and $(1-K_1)$, the power transferred by one DAB (converter 1, delivers K_1 percent of total required power) and the other (converter 2, delivers $1-K_1$ percent of total required power) can be given as

$$P_o^{[1]} = \frac{nV_1V_2}{2L_1 f} D_1(1-D_1) = K_1 P_o \tag{24}$$

$$P_o^{[2]} = \frac{nV_1V_2}{2L_2 f} D_2(1-D_2) = (1-K_1) P_o \tag{25}$$

where P_o is the total required output power. In order to minimize the second carrier harmonic, the magnitude of the two converters should be equal with a phase angle difference of 180°. Thus, to make the second harmonic magnitude equal between two DABs, we need

$$I_1^{[1]}(D_1, L_1) = I_1^{[2]}(D_2, L_2) \tag{26}$$

where $I_1^{[n]}(D, L)$ is the magnitude function of the n-th converter of second carrier harmonics from (11) to (17). For a two-DAB system, n=1, 2. Substituting (24) and (25) into (26) would help us find out the power sharing ratio. However, the magnitude equation in (26) is complicated to solve with a closed-form solution. To address this issue, an extra control loop is developed as shown in Fig. 10. Firstly, the second carrier harmonic magnitude of each DAB $I_1^{[1]}$ and $I_1^{[2]}$ is calculated using (11) to (17) with inputs D_1 and D_2 of the two DABs. The difference of $I_1^{[1]}$ and $I_1^{[2]}$ is then fed to a PI controller to regulate the harmonic magnitude with the parameter K_1. The philosophy of such a controller is explained as follows. When $I_1^{[1]}$ is different from $I_1^{[2]}$, the controller will take action and tune the K_1 to make sure that there is no difference between $I_1^{[1]}$ and $I_1^{[2]}$. With this extra controller, the second carrier harmonic magnitude from two DABs will be controlled to be the same. By applying both magnitude and phase control as shown in Fig. 10, the second carrier harmonic can be entirely cancelled at the common DC bus.

It is mentioned that the proposed method relies on the phase shift of different carrier waves. It is important to synchronize the clock of each converter. For the system controlled by different controllers, synchronization can be realized by the peripherals of the controller. Hence, the proposed method can be applied to a multi-controller scheme.

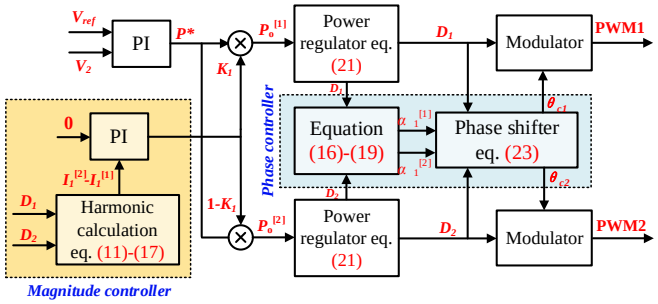


Fig. 10 Enhanced second carrier harmonic cancellation scheme.

C. Three or multi-module scheme

In the condition of three or more converters, a similar scheme can be applied. If all converters in the systems share the same parameters, the phase angle of each converter is:

$$\Delta\theta_{c,n} = \frac{n\pi}{N}, n = 1, 2, ..., N \tag{27}$$

where $\Delta\theta_{c,n}$ is the phase angle of the n-th converter, N is the total number of converters. If the converter parameters are mismatched, the magnitude of each converter is different. This means that the phase angle in (27) is not suitable in these conditions. To solve this issue, each phase angle should be modified to achieve better performance. The following analysis is based on a three-converter system.

Firstly, the base phase angle is calculated based on the magnitude of each converter. If the phase shift ratio of each converter is different, the magnitude of harmonics in each module is different. Supposed that the magnitude of harmonics of each converter are $I_{[1]}$, $I_{[2]}$, $I_{[3]}$ based on equations (11) to (17) in the paper, we have:

$$\Delta\theta_{12} = \frac{1}{2}\arccos\frac{I_{[3]}^{\ 2} - (I_{[1]}^{\ 2} + I_{[2]}^{\ 2})}{-2I_{[1]}I_{[2]}} \tag{28}$$

$$\Delta\theta_{13} = \frac{1}{2}\arccos\frac{I_{[2]}^{\ 2} - (I_{[1]}^{\ 2} + I_{[3]}^{\ 2})}{-2I_{[1]}I_{[3]}} \tag{29}$$

where $\Delta\theta_{12}$ is the phase difference between converter 1 and converter 2, and $\Delta\theta_{13}$ is the phase difference between converter 1 and converter 3.

According to equations (11) to (19) in the paper, the phase shift ratio can not only affect the magnitude but also the phase angle of harmonics. Hence, compensation is applied to (28) and (29):

$$\Delta\theta_{12} = \frac{1}{2}\arccos\frac{I_{[3]}^{\ 2} - (I_{[1]}^{\ 2} + I_{[2]}^{\ 2})}{-2I_{[1]}I_{[2]}} - \frac{1}{2}(\varphi_{[2]} - \varphi_{[1]}) \tag{30}$$

$$\Delta\theta_{13} = \frac{1}{2}\arccos\frac{I_{[2]}^{\ 2} - (I_{[1]}^{\ 2} + I_{[3]}^{\ 2})}{-2I_{[1]}I_{[3]}} - \frac{1}{2}(\varphi_{[3]} - \varphi_{[1]}) \tag{31}$$

where $\varphi_{[1]}$, $\varphi_{[2]}$, $\varphi_{[3]}$ are the harmonic angles of each converter and are calculated based on equations (16) to (19) in the paper. Based on the phase difference between each converter, the controller generates the different signal waveforms for each converter, as shown in Fig. 11. For a system with more than three converters, the system can be regarded as a combination of two or three converters. Hence, the proposed scheme can be applied to a multi-converter system.

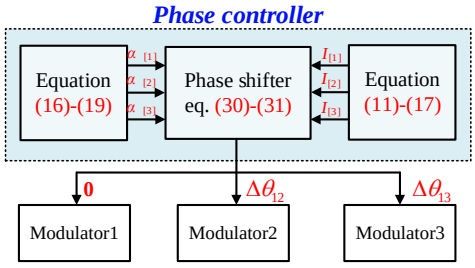


Fig. 11. Three-module scheme.

D. Capacitance evaluation

To better show the effectiveness of the proposed method, capacitance reduction is analysed. According to the relationships of capacitor voltage and current, we have:

$$C\sum_{k=1}^{\infty}\frac{dV_k}{dt_k} = \sum_{k=1}^{\infty} i_k(t) \tag{32}$$

where $i_k(t)$ represents the functions of the k-th harmonic. Since the voltage ripple is caused by the harmonics, the overall voltage ripple is the sum of them. The harmonic functions are all trigonometric functions. Hence, the function of voltage ripple is:

$$C\sum_{k=1}^{\infty}\Delta V_k = \sum_{k=1}^{\infty}\int i_k(t) \tag{33}$$

$$\sum_{k=1}^{\infty}\Delta V_k = \sum_{k=1}^{\infty}\int_{-T_k/4}^{T_k/4} I_k\cos(2\pi f_k t)dt\frac{1}{C} = \frac{1}{C}\sum_{k=1}^{\infty}\frac{I_k}{\pi f_k} \tag{34}$$

where I_k represents the magnitude of the k-th harmonic. ΔV_k represents the ripple voltage caused by the k-th harmonic. C is the capacitance. If the conventional method and proposed methods have the same voltage ripple, the capacitance relationships are:

$$\sum_{k_1=1}^{\infty}\frac{I_{k_1}}{f_{k_1}}\frac{1}{C_1} = \sum_{k_2=1}^{\infty}\frac{I_{k_2}}{f_{k_2}}\frac{1}{C_2} \tag{35}$$

where C_1 is the capacitance in the conventional method, while C_2 is the capacitance in the proposed method. In the proposed method, suppose that the second-carrier harmonics (k = 1) are eliminated only, we have:

$$\frac{C_2}{C_1} = \frac{\sum_{k=2}^{\infty}\frac{I_k}{k}}{\sum_{k=1}^{\infty}\frac{I_k}{k}} \tag{36}$$

Based on equations (11) to (17), the ratio of C_2 and C_1 is about 0.46. This means that the capacitance in the proposed method is 46 % of the conventional method. Suppose that the capacitor is ideal and shares the same structures and dielectric, the volume reduction of capacitor is about 54 % theoretically.

IV. Simulation and Experiment Results

A. Simulation results

The simulation is implemented on Matlab/Simulink with PLECS Blockset. The control loop is implemented in Simulink and the circuit model is implemented in PLECS. The parameters used for simulation are shown in Table IV. The

input voltage is 250 V. The output voltage is assumed to be 270 V. The switching frequency of power modules is set at 20 kHz. The transformer has a ratio of 1:1 with two different leakage inductances 360 μH and 400 μH.

The simulation is divided into two parts. The first simulation indicates the difference when harmonic suppression is applied compared to a traditional parallel system. The results are shown in Fig. 12. The whole process is conducted on the same power sharing ratio. In the first section, before the time 30 ms, the two converters switching signal has the same phase angle. The two converters both generate second carrier harmonics ($2f$) to dc-link current (i_{dc1} and i_{dc2}). These components are summed up on the capacitor current (i_{cap}). As shown in the spectrum diagram of the first section. The magnitude of the second carrier harmonic is 7.62 A.

TABLE IV SIMULATION ENVIRONMENT

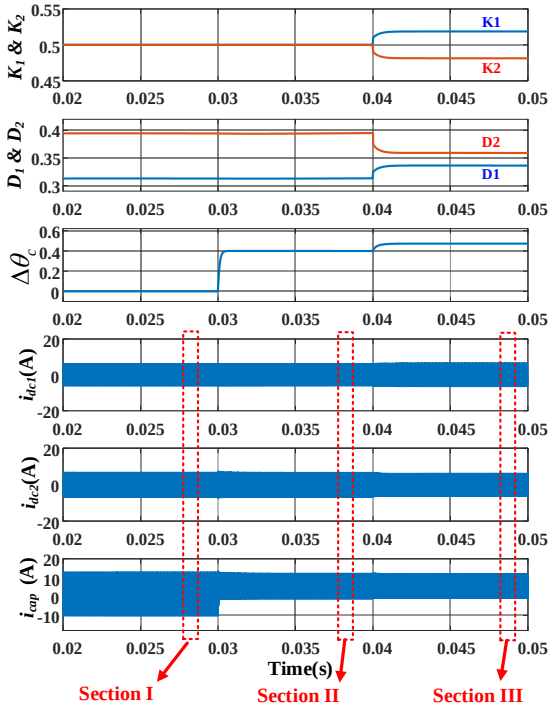
Parameters	Value
Input voltage V_1	250 V
Output voltage V_2	270 V
Output power P_o	2 kW
Leakage inductance	L_1 = 360 μH, L_2 = 400 μH
Switching frequency f	20 kHz
Transformer ratio n	1:1

The proposed normal harmonic suppression scheme is applied in the second section at 30ms. The switching signal phase ratio ($\Delta\theta_c/\pi$) of second converter delays with respect to the first converter increases from 0 to around $\pi/2$. It can be obviously seen from Fig. 12 (a) that the reverse current in i_{cap} is almost disappeared. Apart from that, the harmonic at 120 kHz is also reduced. In the zoom-in view, when the output current in one of the two converters is decreased, the other converter provides a positive current and balances the capacitor current. This significantly reduced reactive power in the system. Thus, a suppressed second harmonic on the DC-link current is achieved. As can be seen from the spectrum of the second section, the second carrier harmonic is reduced from 7.62 A to 1.37 A (82% reduction).

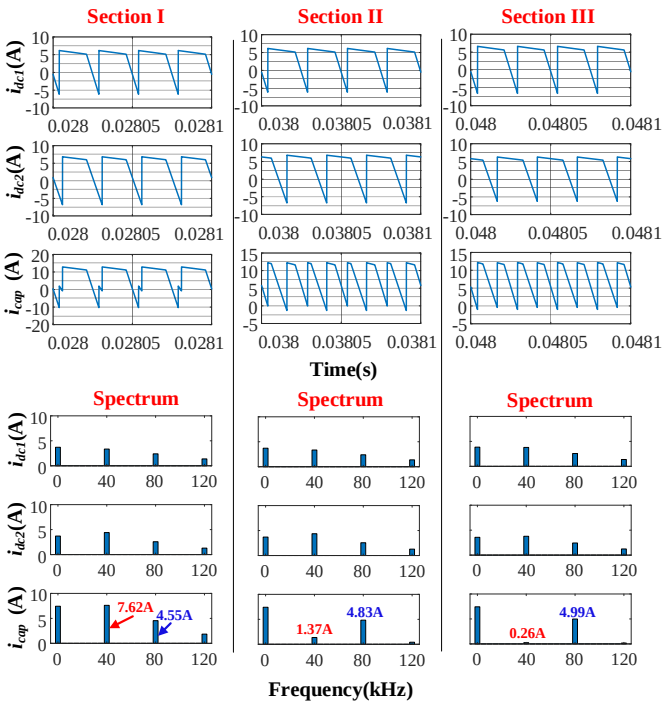
The second part is to verify the enhanced harmonic suppression scheme. The result is shown in the third section of Fig. 12 (a). The power sharing ratio is 1:1 before time 30 ms. It can be seen from the spectrum of the second section that the second carrier harmonic has been partially eliminated before enhanced harmonic control is applied. Due to the same power sharing ratio, even if the harmonic phase angle is opposite, the magnitude in the two converters is different. The proposed enhanced harmonic scheme is applied at the time of 40 ms. The power sharing ratio begins to change. The converter with a smaller leakage inductance generates a higher phase shift in the converter. And the magnitude is higher than another converter. Thus, to achieve the same harmonic magnitude, the converter with a larger leakage inductance should provide higher power. As shown in Fig. 12 (a), K_1 increases and K_2 decreases.

In the zoom-in view, the i_{cap} peak current in each cycle tends to be equal and uniform after the proposed scheme is applied, as shown in the subfigure in Fig. 12 (b). The difference of i_{dc1} and i_{dc2} between the three sections is the phase and magnitude. In section II and section III, there is a phase shift in the carrier wave. In section III, i_{dc1} is higher than in section II, and i_{dc2} is slightly smaller than in section II. Compared to the conventional method without phase shift, the current ripple is significantly reduced when the harmonic suppression scheme is applied. As can be seen from the spectrum, the second-carrier harmonic is reduced from 7.62 A to 0.26 A. It is a 97% reduction compared to the non-suppression method. Compared to the proposed normal suppression method in Section II, the second-carrier harmonic is reduced from 1.37 A to 0.26 A. If the parameter mismatch is higher, the enhanced scheme performance is better. It can be seen that the current ripple in section III is slightly smaller than in section II. Although the current ripples are very close between the normal scheme and the enhanced scheme, the waveform in the enhanced method is more consistent and the frequency is higher, which is closer to 80 kHz. This can be seen from the spectrum, the harmonic of section III in 80 kHz is higher than section II. Thus, the harmonic is further eliminated.

The simulation results of the three-converter system are shown in Fig. 13. The voltage level, switching frequency and transformer ratio are the same as in Table IV. The inductances of the three converters are L_1 = 360 μH, L_2 = 400 μH and L_3 = 400 μH respectively. And the output power is 2500 W. It can be seen that the second-carrier harmonic is significantly reduced and close to zero compared to the result without the proposed method. In addition, the harmonics at 80 kHz are also reduced, and the performance of a three-converter system is better than a two-converter system.

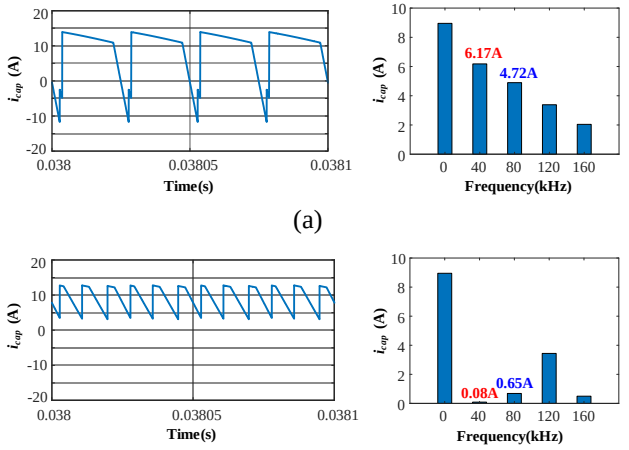


(a)



(b)

Fig. 12 Simulation result comparison when harmonic suppression is applied. (a) Overall waveforms, (b) amplified waveforms and spectrum.



(a)

(b)

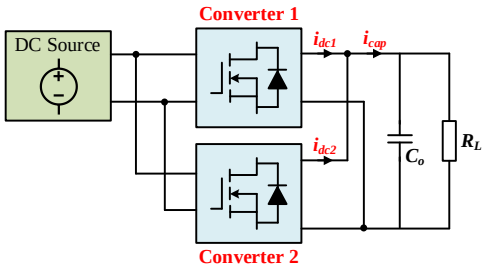
Fig. 13. The waveforms (left) and the spectrum (right) of capacitor current in a three-converter system. (a) the conventional method, (b) the proposed method.

B. Experiment results

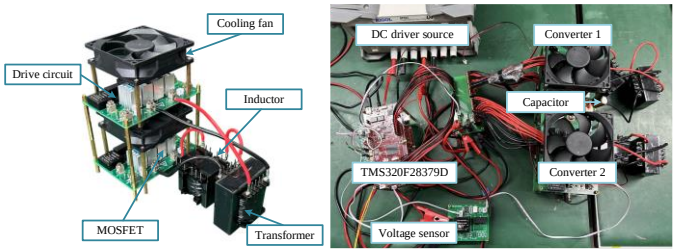
In the experiment, a DC converter system composed of two DAB converters is used to verify our proposed harmonics suppression scheme. The DAB converter system is fed by one source to represent two independent DC sources with the same input voltage. The experiment setup is shown in Fig. 14. Fig. 14(a) shows the system schematic drawing. Fig. 14(b) is the picture of a single DAB converter. The overall experimental platform is shown in Fig. 14(c). PWM signals are generated from the TMS320F28379D controller. The parameters of the experiment are shown in Table V. The switching frequency is 20 kHz. The leakage inductance of the two converters is 360 μH and 400 μH, respectively. The input voltage is 90 V. The output voltage is 100 V and the load is 200 W.

TABLE V EXPERIMENT PARAMETERS

Parameters	Value
Input voltage V_1	90 V
Output voltage V_2	100 V
Output power P_o	250 W
Leakage inductance	L_1 = 360 μH, L_2 = 400 μH
Switching frequency f	20 kHz
Output capacitor C_o	47 uF
Transformer ratio n	1:1

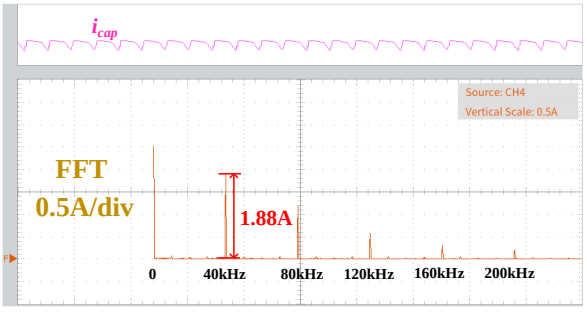


(a)



(b) (c)

Fig. 14 Experimental setup. (a) Schematic drawing. (b) Single converter. (c) Overall platform.



(a)

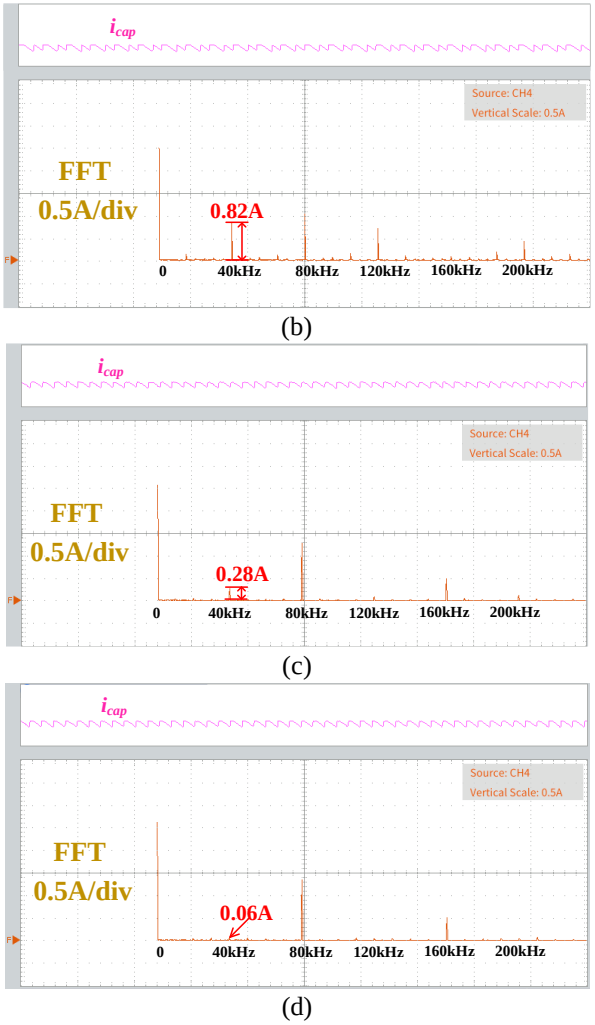
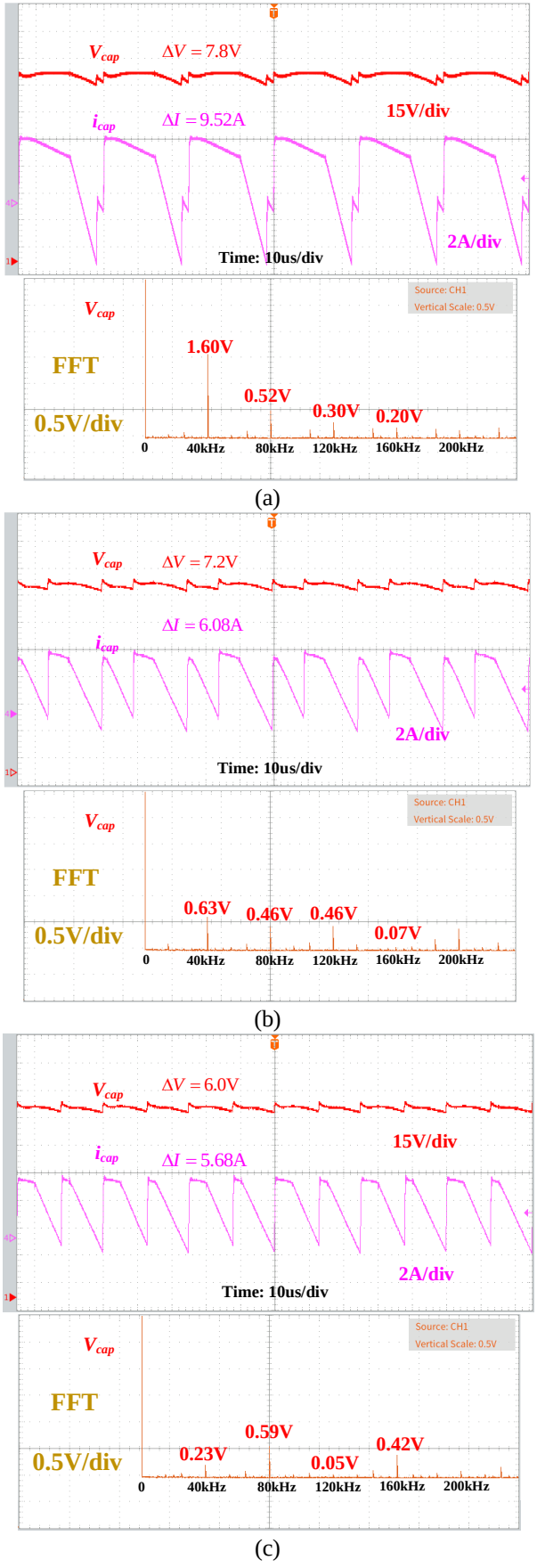
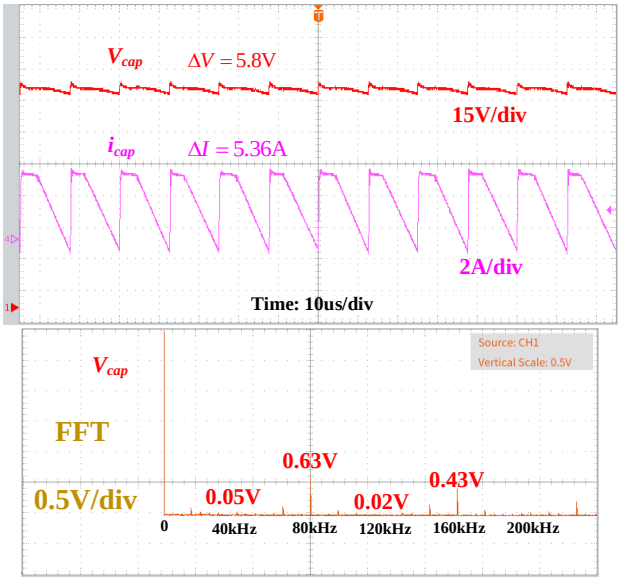


Fig. 15. Capacitor currents and their spectrum when (a) Harmonic suppression scheme is not applied. (b) Interleaved scheme. (c) Proposed normal scheme. (d) Enhanced suppression scheme.

Fig. 15 (a) shows the capacitor current (i_{cap}) spectrum in the normal control method without harmonic suppression, where the second-carrier harmonics is 1.88 A. Fig. 15 (b) shows the capacitor current spectrum of a normal interleaved scheme. The second-carrier harmonics is 0.82 A. Fig. 15 (c) shows the performance of the proposed normal suppression scheme. The second-carrier harmonic is suppressed from 1.88 A to 0.28 A, and about 85% of the second-carrier harmonic is eliminated. The second carrier harmonic cannot be fully cancelled from the control scheme in Fig. 8 due to the different leakage inductances. Using the enhanced harmonics cancellation scheme as shown in Fig. 10, the magnitude of the second carrier harmonic can be further suppressed to 0.06 A (97% reduction) as shown in Fig. 15 (d). Compared to the conventional interleaved method, the proposed method has a better performance when the parameters are mismatched.





(d)

Fig. 16 Capacitor voltage and current waveforms and voltage spectrum when: (a) Harmonic suppression scheme is not applied. (b) Interleaved scheme. (c) Proposed normal suppression scheme. (d) Enhanced suppression scheme

Fig. 16 (a)-(d) shows the amplified capacitor current waveforms and capacitor voltage spectrum in different situations. The capacitor voltage is measured and its voltage is effectively the voltage on the DC bus. The current waveforms are similar to the simulation. Fig. 16 (a) represents the result without the provided method. The current ripple is 9.52 A. The frequency of the current is lower and the current ripple is very large. This results in harmonic voltage in the capacitor, as can be seen from the spectrum. Fig. 16 (b) represents the result of the conventional interleaved method. The current ripple is 6.08 A. It can be seen that the interleaved method has some improvement in the capacitor current ripple but still has limited performance when facing the parameter mismatch. Even though the current ripple is reduced by applying a constant phase angle, the waveform still contains many second carrier components. The voltage ripple is not significantly reduced. In Fig. 16 (c), the phase shift angle is calculated by the harmonic model. The voltage and current ripple are further reduced compared to Fig. 16 (b). In Fig. 16 (d), the magnitude of harmonics is regulated and the current waveforms are more regular and the frequency is close to 80 kHz. The second-carrier components are further reduced. The voltage and current ripple are the smallest. It can be seen that, with the implementation of the enhanced cancellation scheme, the voltage ripple of the capacitor is reduced from 7.8 V to 5.8 V using the enhanced cancellation scheme (38% reduction). This means that the proposed method can apply a smaller capacitor to keep the same voltage ripple.

V. Conclusion

In this paper, the mathematical model of the second-carrier harmonic in DAB converter was investigated. The model indicates that the magnitude and the phase are dependent on the phase shift ratio.

Based on the model, a second carrier harmonic elimination method is proposed. By shifting a certain phase angle of the carrier wave, the reduction in the second carrier harmonic is achieved in a two-DAB converter system. The model derived in SPS modulation and the cancellation method is basic research of harmonic elimination. It gives a potential approach of harmonic cancellation in not only dual DAB converter systems, but also other multi-converter systems, such as microgrid or other DC converters. Meanwhile, harmonics in multi-phase shift modulation can also be further investigated.

Finally, simulation and experiment were implemented to verify the validity of the proposed second carrier harmonic model and cancellation method. According to the results, the proposed method could significantly reduce the second-carrier harmonics.

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