

Optimized Carrier Disposition Based Discontinuous Pulse-width Modulation Method for three-level NPC Converters

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Abstract—Three level neutral-point-clamped (3L-NPC) converter is a multilevel topology that is well-suited solution in high voltage, high frequency applications such as flexible AC transmission systems and electric vehicle drive systems. This paper is focused on a silicon carbon (SiC) based 3L-NPC for high frequency application which presents a higher switching loss and aging mismatch. In this paper, a new improved approach of the discontinuous pulse width modulation (DPWM) of 3L-NPC based on carrier disposition is presented. Based on the relationship between switching loss and power factor angle, an optimized DPWM method with minimum switching loss is proposed. The simulation and experimental results show how the optimized carrier disposition based discontinuous pulse-width modulation (OCD-DPWM) is achieved whereas the switching loss is reduced and the system efficiency is improved.

Keywords—3L-NPC, DPWM, modulation method, switching loss, efficiency

I. INTRODUCTION

As the energy crisis intensifies, there is an urgent need to improve the power electronics conversion efficiency to reduce the unnecessary waste. The improvement has become a research hotspot of many scholars. Comparing to the conventional two-level converters, three level neutral-point-clamped topology which could generate three level step shaped phase voltage and five level shaped phase voltage could provide an effective way to reduce the harmonics of output voltage and current. Moreover, it also has the advantage of the reduction of emitter-collector voltage (V_{CE}), which means smaller voltage capacity devices could be selected for the same power application. Due to the low stress to switching devices, switching noise and switching

loss are reduced [1]. Therefore, 3-L NPC is widely used for high voltage, high frequency applications such as high speed machine control [2-5] and electric vehicle drive systems [6-8]. Since the converter is always used for medium or high power applications, a PWM scheme which minimizes the losses of the converter is necessary for highly efficient power transmission. Additionally, as the switching frequency of the power devices is becoming higher, the minimization of the switching loss becomes a more relevant issue.

The losses of power converters are mainly divided into two categories: the conduction loss and the switching loss. Some scholars devote to the analysis of the conduction loss and the relationship of duty ration of the PWM and the conduction loss has been concluded in [9]. Meanwhile, in order to minimize the switching loss, some improved modulation schemes have been proposed [6, 10-14]. Discontinuous pulse width modulation (DPWM) is one of these which provide a novel direction to save the energy. In addition, DPWM also bring other advantages to the conversion system, [9] uses DPWM to solve the neutral-point voltage unbalancing issue which is an inheritance problem of three-level NPC inverter due to the split dc-link capacitors. The effectiveness of the proposed DPWM method is verified by using the simulation and the experimental results. However, these strategies do not guarantee the minimum switching loss of the converter which operates in all the ranges of the phase angle.

In this paper, a carrier disposition based DPWM method is proposed and compared with the space vector based DPWM method. Meanwhile, the switching losses for various PWM schemes are also summarized. From these results, an optimized DPWM strategy which is based on carrier disposition PWM is developed in order to minimize the loss

This work was supported by the Ningbo Science & Technology Bureau under Grants 2017D10029 and 2017D10031. This work was also supported by the Zhejiang Provincial Department of Human Resources and Social Security under Grant QJD1803013

of a voltage-fed three-phase PWM rectifier in all the ranges of the phase angle. To verify the effectiveness of the proposed OCD-DPWM method, a 3L-NPC experimental prototype is designed using silicon carbon devices. The simulation and experimental results show a good performance of the proposed PWM method.

II. 3L-NPC TOPOLOGY AND DPWM METHODS

In Fig. 1, a typical topology of the three-level neutral point clamped converters is presented. It can be seen, the output voltage of each phase has three states ($-V_{DC}/2$, 0, $+V_{DC}/2$) [15].

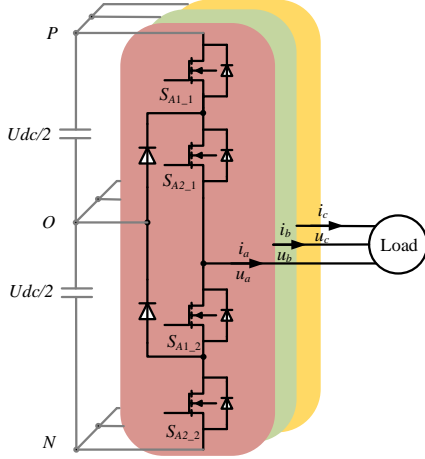


Fig. 1. 3L-NPC topology

In order to reduce the switching losses, the inverter outputs are alternately connected to the top or bottom of the dc-link for a time. By locking the switch state to ON or OFF in specific intervals, it can reduce the number of switching operation of the switches under large current. By increasing the number of switching operation under low current, switching loss could be minimized, so that the system efficiency of the three-level NPC inverter could be increased.

Conventional 60° DPWM methods can be described by using an unified expression. The desired three phase voltage reference of the converter is shown as follow:

$$\begin{cases} u_a^* = M \sin(\omega t) \\ u_b^* = M \sin(\omega t - 120^\circ) \\ u_c^* = M \sin(\omega t + 120^\circ) \end{cases} \quad (1)$$

Where $M = \sqrt{3}U_m/U_{dc}$ is the modulation index, which is less than 1.154, ω is the angular frequency of reference voltage.

In order to improve the modulation index of the converter, The common mode voltage (CMV), as shown in (2), is injected to the original voltage reference.

$$u_z = -kU_{\max} - (1-k)U_{\min} + (2k-1) \quad (2)$$

Where $U_{\max} = \text{Max}(u_a^*, u_b^*, u_c^*)$, $U_{\min} = \text{Min}(u_a^*, u_b^*, u_c^*)$, and k ($0 \in 1$) is defined as the proportional allocation factor. Different DPWM method can be realized by using different k value. Then the new reference of A, B and C can be obtained as follow:

$$\begin{cases} u_{az}^* = u_a^* + u_z = M \sin(\omega t) + u_z \\ u_{bz}^* = u_b^* + u_z = M \sin(\omega t - 120^\circ) + u_z \\ u_{cz}^* = u_c^* + u_z = M \sin(\omega t + 120^\circ) + u_z \end{cases} \quad (3)$$

A. Space Vector Based Discontinuous Pulse Width Modulation Method

For space vector based discontinuous pulse width modulation method, the operating status of the switch and the pole voltage in the NPC inverter can be represented by the switching states shown in Table I. k VALUE OF EACH INTERVAL OF DPWMx

DPWMx	Interval number											
	1	2	3	4	5	6	7	8	9	10	11	12
DPWMMAX	1	1	1	1	1	1	1	1	1	1	1	1
DPWMMIN	0	0	0	0	0	0	0	0	0	0	0	0
DPWM0	0	1	1	0	0	1	1	0	0	1	1	0
DPWM1	0	0	1	1	0	0	1	1	0	0	1	1
DPWM2	1	0	0	1	1	0	0	1	1	0	0	1
DPWM3	1	1	0	0	1	1	0	0	1	1	0	0

When the three-level NPC inverter generates three phase voltage and current, the 3L-NPC inverter has 27 combinations of switching states. These combinations are possible to indicate a switching state with a space vector and it can be confirmed in Fig. 2. In accordance with the magnitude of the vector, the space voltage vectors can be classified into four categories: large, medium, small, and zero. There are several conventional DPWM methods, which can be classified into 30° , 60° , and 120° DPWM methods. The main difference is the number of intervals of one voltage cycle. Among these method, 60° DPWM method is the most common one. By dividing one cycle of voltage into twelve equal intervals, named 1~12. As shown in Table 1, each of the intervals is periodically taken as 0 or 1 to generate six DPWM modes (fig. 3).

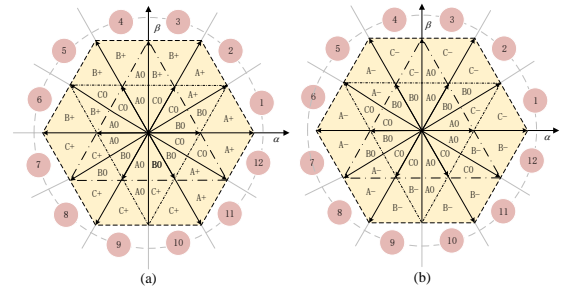


Fig. 2. SV-DPWM method (a) $k=1$; (b) $k=0$

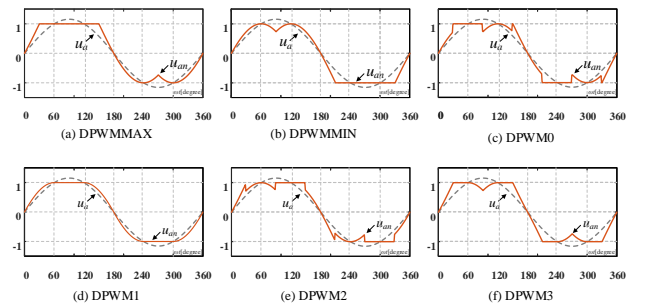


Fig. 3. DPWMx modulation waveform

B. Carrier Disposition Based Discontinuous Pulse Width Modulation Method

Differing from the SV-DPWM, carrier disposition based discontinuous pulse width modulation method is no longer relying the switch states but referring to the modulated wave which can be calculated from the reference utility voltage. There are two kind of carrier-based modulation method, one is the carrier phase shift (CPS) which is suitable for most kind of multi-level converters, the other one is the carrier disposition (CD) based modulation method which is the desired method for 3L-NPC converter. According to the carrier wave of switches in the same lag, CD PWM can be divided into two categories: PD-carrier disposition and POD-carrier disposition. Considering the degree of control freedom, a DPWM method combining with the carrier disposition based modulation is selected in this paper (shown in figure 4).

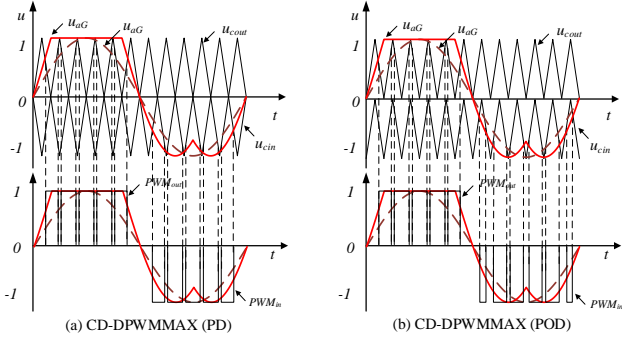


Fig. 4. CD-DPWM modulation method

C. Switching Loss Analysis of DPWMx

Switching loss of discontinuous PWM schemes, which have been well analyzed in some papers, is summarized in this section and compared with the one of continuous PWM schemes.

For the calculation of the switching loss, the linear dependency of a switching energy loss on the switched current is assumed from the measurement results. Therefore, when a high switching frequency is implied, the switching loss is as follows for the continuous PWM schemes:

$$P_{sw(continuous)} = \frac{1}{2\pi} \int_{\frac{\pi}{2}+\phi}^{\frac{\pi}{2}} E_{TD} i f_{sw} d\theta = \frac{E_{TD} I f_{sw}}{\pi} \quad (4)$$

Where $P_{sw(continuous)}$ is the switching loss of continuous PWM modulation method, E_{TD} is the equivalent DC voltage, f_{sw} is the switching frequency and i is the load current. In the case of the DPWMx, according to the symmetry of pole voltage, the following properties can be obtained:

$$\begin{aligned} P_{sw}(-\phi) &= P_{sw}(\phi) \\ P_{sw}(\phi) &= P_{sw}(\pi - \phi) \end{aligned} \quad (5)$$

Where ϕ is the power factor angle which is between 0 and 180°. Therefore, it is sufficient to consider the range of $0 < \phi < \pi/2$ for the discontinuous PWM schemes as follow:

$$P_{sw(DPWM1)}(\phi) = \begin{cases} P_{sw(continuous)} \cdot \left(1 - \frac{1}{2} \cos \phi\right), & 0 < \phi < \frac{\pi}{3} \\ P_{sw(continuous)} \cdot \frac{\sqrt{3}}{2} \cos \phi, & \frac{\pi}{3} < \phi < \frac{\pi}{2} \end{cases} \quad (6)$$

$$P_{sw(DPWM0)}(\phi) = P_{sw(continuous)} \cdot \left(\phi - \frac{\pi}{6}\right) \quad (7)$$

$$P_{sw(DPWM2)}(\phi) = P_{sw(continuous)} \cdot \left(\phi + \frac{\pi}{6}\right) \quad (8)$$

$$P_{sw(DPWM3)}(\phi) = \begin{cases} P_{sw(continuous)} \cdot \left(1 - \frac{\sqrt{3}-1}{2} \cos \phi\right), & 0 < \phi < \frac{\pi}{6} \\ P_{sw(continuous)} \cdot \frac{\sin \phi + \cos \phi}{2}, & \frac{\pi}{6} < \phi < \frac{\pi}{3} \\ P_{sw(continuous)} \cdot \left(1 - \frac{\sqrt{3}-1}{2} \sin \phi\right), & \frac{\pi}{3} < \phi < \frac{\pi}{2} \end{cases} \quad (9)$$

$$P_{sw(DPWMMAX)}(\phi) = \begin{cases} P_{sw(continuous)} \cdot \left(1 - \frac{\sqrt{3}}{4} \cos \phi\right), & 0 < \phi < \frac{\pi}{6} \\ P_{sw(continuous)} \cdot \left(\frac{1}{2} + \frac{\sin \phi}{4}\right), & \frac{\pi}{6} < \phi < \frac{\pi}{2} \end{cases} \quad (10)$$

From the equation (6) to equation (10), it can be seen, the switching loss of different modulation schemes mainly relevant to the power factor angle of the converter. In order to analysis the losses effectively, a relative switching loss function (RSLF) which is suitable for all kinds DPWMx is deduced as follow:

$$RSLF = \frac{P_{sw(DPWMx)}}{P_{sw(continuous)}} = \frac{1}{4} \int_0^{2\pi} f(\theta) d\theta \quad (11)$$

According to the function of RSLF, the ratios of switching losses of discontinuous PWM schemes compared with continuous PWM schemes can be obtained (shown in fig. 5). It can be seen, the switching loss is reduced by 33% on the average and there is a wide difference of switching loss among DPWM schemes depending on the phase angle.

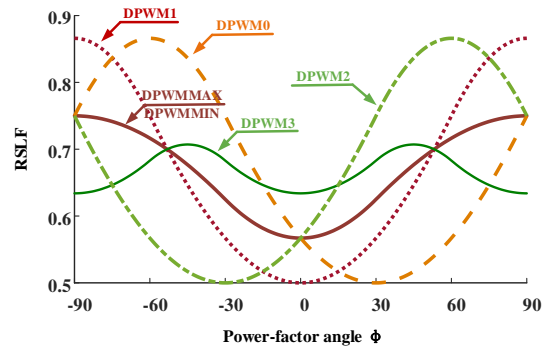


Fig. 5. RSLF- ϕ waveform of DPWMx

III. OPTIMIZED CARRIER DISPOSITION BASED PULSE WIDTH MODULATION METHOD

As shown in Fig. 5, the RSLF changes greatly along with the power factor angle. Since the modulation index is normally higher than 0.9, unit power-factor control is no longer suitable in this case because the saturation of PWM converters. It will become more serious when the DC-link

voltage getting lower or the output voltage becomes higher. Hence, the power factor angle is reasonable to be considered as a control factor to minimize the switching loss. In this section, an optimized CD-DPWM (OCD-DPWM) method is proposed based on the analysis of switching loss and power factor angle.

A. Proposed OCD-DPWM Method

The voltage equation of converter in d-q frame is:

$$\begin{aligned} 0 &= pL_d i_d - \omega L_q i_q + V_d \\ E &= pL_q i_q + \omega L_d i_d + V_q \end{aligned} \quad (12)$$

Where p is the derivative operator, E is the magnitude of the output voltage. When the modulation index is lower and no saturation occurs, the unit power-factor control is much desirable to regulate d -axis current to zero like SV-PWM control method. However, when the dc voltage of the converter cannot meet the requirement of the output voltage, the dynamic response is getting poorer. Especially when the q -axis current change from positive to negative abruptly to meet the output requirement of the converter phase voltage.

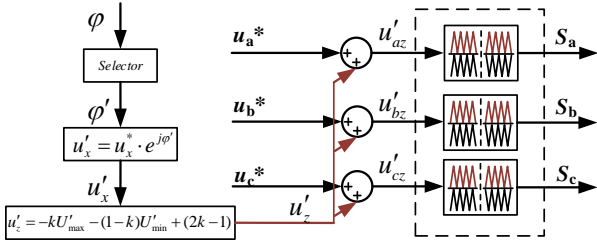


Fig. 6. Modulation strategy of OCD-DPWM

In this case, the phase angle at the output side is changed from 0 to 180° depending on the operation condition. The modulation strategy is illustrated in Fig. 6 and the RSLF of this optimized CD-DPWM is calculated according to equation (11). One power factor angle selector is used before the calculated voltage reference is implemented. According to the feedback current and voltage, the power factor angle can be obtained. At this time, a power factor angle selector will be used to find out the minimum loss. The RSLF- ϕ waveform of it is illustrated in Fig. 7. It can be seen, the switching loss of optimized CD-DPWM is conspicuously reduced by 46% on the average, which means 20% off to previous six DPWMx methods on the average.

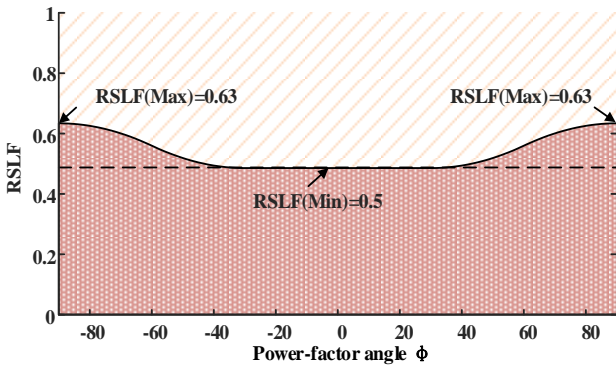


Fig. 7. RSLF- ϕ waveform of OCD-DPWM

B. Efficiency Analysis

TABLE I. PARAMETERS OF SWITCH AND DIODE

$(P_n=3300\text{kW}, I_n=5\text{A}, M=0.86) 175^\circ\text{C}$		
Switch	E_{on}	330 $\mu\text{J/pulse}$
	E_{off}	85 $\mu\text{J/pulse}$
	V_{CE}	1.7V
Diode	E_{rr}	22.1 $\mu\text{J/pulse}$
	V_F	2.3V/pulse

In order to identify the efficiency improvement of the proposed CD-DPWM method, an experimental prototype is designed based on SiC MOSFET (shown in Fig. 8). The parameters of switches and diodes is illustrated in table II. The conduction loss ($P_{s,con}$) and switching loss ($P_{s,sw}$) of a switch are calculated as:

$$P_{s,con} = V_{CE} \cdot I_C \cdot D_{sw} \quad (1)$$

$$P_{s,sw} = \frac{f_{sw} \cdot (E_{on} + E_{off}) \cdot I_{sw}}{I_{nom}} \quad (6)$$

Where V_{GS} is the gate threshold voltage, I_{GSS} is the gate-source leakage current, D_{sw} is the duty ratio, f_{sw} is the switching frequency, and E_{on} and E_{off} are turn-on and turn-off energy losses. The conduction loss ($P_{d,con}$) and switching loss ($P_{d,sw}$) of a diode are calculated as:

$$P_{d,con} = V_F \cdot I_D \cdot (1 - D_{sw}) \quad (7)$$

$$P_{d,sw} = f_{sw} \cdot E_{rr} \quad (8)$$

Where V_d is the diode voltage drop, I_D is the diode forward current, and E_{rr} is reverse recovery energy loss. The losses of switches and diodes are calculated by using the parameters listed in Table I. The efficiency of CPWM and CDB-DPWM is compared as shown in Fig. 7. It can be seen, when the frequency become higher, the efficiency will drop quickly and the DPWMx can effectively promote the system efficiency.

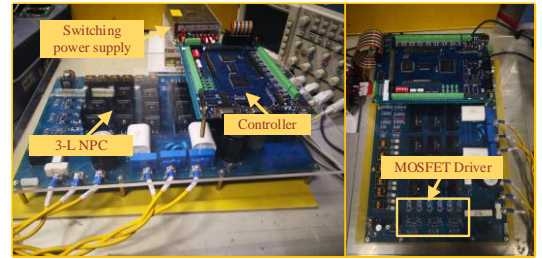


Fig. 8. Experimental prototype of 3L-NPC converter

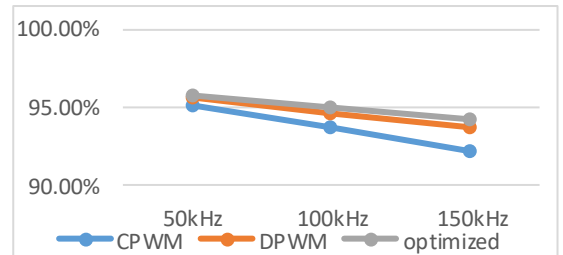


Fig. 9. System efficiency comparison among CPWM, DPWMx and OCD-DPWM

IV. CONCLUSION

In this paper, the carrier disposition based DPWM method for 3-level NPC inverters is proposed and the relationship between SV-DPWM and CD-DPWM is analyzed. According to the working principle, six DPWM mode is generated which shows 33% reduce of switching loss on the average than continuous PWM method. Based on the relationship between switching loss and power factor angle, an optimized CD-DPWM is proposed, which can reduce 46% switching loss of 3L-NPC inverters. For further research, the analysis among different modulation methods will be done in more detail, and the THD of different methods will be compared and verified in experiments.

ACKNOWLEDGMENT

This work was supported by the Ningbo Science & Technology Bureau under Grants 2017D10029 and 2017D10031. This work was also supported by the Zhejiang Provincial Department of Human Resources and Social Security under Grant QJD1803013

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