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RESEARCH ARTICLE

Design Analysis of SiC-MOSFET Based Bidirectional SSPC for Aircraft High Voltage DC Distribution Network

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ABSTRACT Research on electric power systems (EPSs) for the aviation industry has recently grown significantly due to the need to reduce global CO2 emissions from transportation. To fulfill the power requirements of a more electric aircraft (MEA), DC power distribution has emerged as a potential solution. However, the progress of DC distribution faces significant difficulties related to system protection. Solid-state power controllers (SSPCs) are being considered in these applications due to their ability to provide fast-tripping mechanisms for system protection. Although SSPCs have been successfully implemented in low voltage DC 28V aircraft networks, their application in high voltage systems (270 V, ±270 V, or higher) presents challenges, such as over-voltage and excessive power loss, particularly for high-power applications. This paper focuses on the development of SSPCs for a 270 V DC system with a current rating of 125 A / 250 A. The paper presents designs for over-voltage suppression and thermal management of the SSPCs. The study also includes a comparative analysis of using a different number of SiC MOSFET modules connected in series and parallel and their effect on the cooling requirements and circuit temperature to assess power losses, power density, weight, and cooling requirements for the SSPCs. A prototype of the proposed SSPC has been built for experimental validation. Results show effective over-voltage suppression to 480 V and quick interruption capabilities with trip currents of 250 A and 375A within time intervals of 160 μs and 300 μs, respectively, for line inductance of 105 μH. The circuit withstands energy up to 22.5 J for a breaking current of 375 A.

INDEX TERMS Electric power systems, more electric aircraft, solid-state power controllers SSPCs, thermal design, SiC MOSFET, dc distribution, cooling requirements.

I. INTRODUCTION

The shift in the aviation industry towards more electric aircraft (MEA) technology necessitates substituting conventional aircraft equipment with their electrical counterparts, such as power sources, converters, and protection devices [1], [2], [3], [4], [5], [6]. The main aim of this transformation is to reduce the carbon footprint of the aviation sector while concurrently increasing efficiency and reducing the weight of new aircraft [7]. Additionally, MEA technology presents advantages such as decreased noise and vibration, and improved reliability relative to existing systems [8], [9].

The existing electric power systems (EPS) found in more electric aircraft are discussed in [2]. The conventional system relies on an AC configuration, as seen in aircraft such as B737 which uses constant frequency based electrical system (115 V, 400 Hz). However, this configuration suffers from low power density [10]. To improve the power density and efficiency, the MEA has started incorporating a high DC voltage alongside the AC system, creating a hybrid configuration that combines both AC and DC systems [2], [9]. A 115 V/320-800 Hz AC and 270 V DC system has been used

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recently in F35 from Lockheed Martin [11], aiming to reduce the weight of the overall aircraft cables. Moreover, 230 V / 320-800 Hz AC and a 540V (±270 V) DC system, which is used in B787, has been employed to further decrease current, resulting in reduced system weight and improved cooling requirements [10]. The choice between 270 V and 540 V depends on the aircraft's AC voltage network, which is either 115 V or 230 V. Detailed information about these two hybrid scenarios can be found in [2]. The using of a purely DC-based EPS is seen as a promising architecture for MEA, with proposal for a ±270 V system emerging in various projects [9], [10]. However, it is worth noting that the partly or all DC based EPSs encounter challenges related to high fault current caused by large DC-link capacitors and low fault impedance. Furthermore, the absence of zero-crossing points in the DC load current poses a challenge for traditional protection methods. Mechanical circuit-breakers (MCB), commonly used in AC systems, rely on zero-crossing points to interrupt the current flow effectively [12], [13], [14]. However, in a DC based EPS, an alternative protection technology that can interrupt the current without relying on zero-crossing points is required. The emerging technology of solid-state power controllers (SSPCs) can provide faster protection times compared to MCB, typically in the range of tens or hundreds of microseconds. Therefore, SSPCs have been considered for MEA applications [15], [16]. SSPC offers advantages such as faster response, precise current limiting, and the ability to interrupt fault currents. They can be designed to detect fault conditions and quickly turn-off the current [17].

SSPCs are typically composed of one or more semiconductor devices connected in series or/and parallel. However, they suffer significantly higher conduction loss compared to MCBs. In contrast, the hybrid power controller (HPC) combines the strengths of both MCB and SSPCs [18]. However, a high-speed mechanical switch is required to achieve fast turn-off time and avoid oversizing the solid-state part in the HPC. Designing and operating the HPC is complex and costly when compared to the SSPCs and MCB, while aiming for the same functionalities [19].

The literature review presented in [20] examined various aspects related to SSPCs, which included power semiconductor technologies, circuit configurations, overvoltage clamping circuits, gate drivers, and fault detection methods [14], [20], [21], [22], [23], [24], [25], [26]. Different semiconductor technologies were discussed, each with their advantages and limitations. For aircraft applications, Si IGBT could be a suitable option for high current and high voltage applications [27], but it is challenged by high conduction loss (which is the main loss in the SSPC), leading to lower efficiency. In contrast, Wide Band Gap (WBG) devices such as GaN and SiC MOSFETs got attention due to their low ON-state resistance, resulting in reduced conduction losses. However, GaN was considered more suitable for low current applications due to its no high current limited availability in the market. A study implemented the SSPC using GaN devices, which was successfully developed and tested for a DC system voltage of 300 V and a turn-off current of 45 A [28]. For low and medium current applications, SiC MOSFETs emerged as a good choice. In [15], the design of the SSPC utilizing SiC MOSFETs was presented and experimentally validated for 600 V, 60 A, and a turn-off of 180 A. In [29], the SSPC based on SiC MOSFETs was described, offering a 540 V and 100 A capacity, with a turn-off test capability of 150 A. However, despite the comprehensive review, there is a lack of existing research that specifically investigates and provides a design analysis of SSPCs utilizing different semiconductor devices. The SSPC functions as a semiconductor switch that remains in an ON state, allowing continuous current flow. It is capable of handling breaking currents that are between 2× to 12× of the nominal current [29], [30], [31]. For a 270 V DC system, the nominal current is in the order of tens/hundreds of amperes. Consequently, the semiconductor components utilized in the SSPC must be capable of withstanding nominal, overcurrent levels and short circuit currents.

This paper presents novel findings from an in-depth investigation of SSPC utilizing varying numbers of semiconductor components to manage losses, which has not been previously explored by other researchers. To handle high current levels, parallel SiC MOSFET modules can be used [20]. By connecting additional devices in parallel, the resistive behaviour of SiC MOSFETs results in reduced losses. The study takes into account the trade-off between the number of parallel SiC MOSFETs and the cooling system requirements. The research investigates a comprehensive analysis of how the number of series and parallel components impacts thermal capability, cooling demands, weight, and power density during normal and overload current conditions. The design is for a 270 V, 125 A SSPC capable of withstanding overcurrent of 250 A for 2 minutes, providing protection between the 270 V DC bus and load.

The paper is structured in the following manner: In Section II, the SSPC design specifications and topology selection for SSPC are outlined. Section III presents the selection of the semiconductor device, estimation of conduction loss, the necessary cooling, thermal evaluation, and simulation tests from thermal aspect. A detailed explanation of the overvoltage protection mechanism can be found in Section IV. Section V contains the test circuits and experimental results. Lastly, Section VI provides the conclusions of the study.

II. SSPC DESIGN REQUIREMENTS AND TOPOLOGY SELECTION

The design requirements of the SSPC considered in this paper are listed in Table 1, outlining the required functions. The SSPC is designed for 270 V DC system which can be formed as unipolar 270 V (or bipolar ±135 V). The design faces challenges due to the need for high efficiency, specific overcurrent characteristics, and natural convection cooling. The SSPCs are intended to operate at a nominal current I_{nom} of 125 A in 85 °C ambient temperature. Additionally, the

SSPC should be appropriately rated to handle overload and short-circuit current conditions, as specified in Table 1. It is expected that the SSPC can handle 150% I_{nom} (187.5 A) for 10 mins, 200% I_{nom} (250 A) for 2mins, and 300% I_{nom} (375 A) for 1msec, while maintaining a temperature below the specified limit.

In [20], various commonly employed topologies for SSPCs have been discussed. One of these topologies, shown in Fig. 1, consists of a power semiconductor switch combined with an overvoltage protection device that acts as an energy absorption unit. The reason for choosing this topology is its advantages, including reliability, simplicity, and minimal component requirements. To illustrate that, Fig. 1 shows a bidirectional SSPC based on SiC MOSFETs, where two semiconductor devices are required to be connected in an anti-series configuration. When both MOSFETs are simultaneously turned on, the current flows through the MOSFETs' channels instead of the body diode. This behavior is due to the bidirectional characteristic of the MOSFET body. In scenarios where the current demand exceeds the capacity of an individual branch/channel, multiple channels of the SSPC can be connected in parallel. This arrangement effectively minimizes conduction loss due to the resistance ON-state characteristic of the MOSFET.

TABLE 1. Specifications of SSPC.

Type	Bidirectional
Nominal voltage	270 V
Nominal current	125 A
Overload current conditions	1.5 × I_{nom} for 10 mins
	2 × I_{nom} for 2 mins
	3 × I_{nom} for 1 ms
	≥ 4 of I_{nom} for instant trip
	Short circuit current 1250 A
Protection functions	Over current and short circuit
Measured signals	Voltage, current and the temperature signals
Cooling	Natural convection

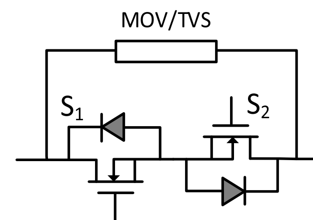

FIGURE 1. Bidirectional SSPC.

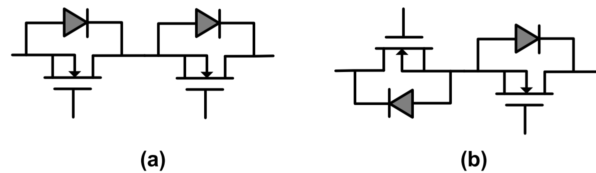

FIGURE 2. Module configurations, a) half-bridge and b) dual-common source.

III. SEMICONDUCTOR DEVICES SELECTION, LOSS ESTIMATION, AND COOLING REQUIREMENTS

The main objective of this section is to describe the specific requirement for achieving high efficiency by carefully choosing the main semiconductor devices and providing the cooling requirements. Additionally, this section emphasizes how the utilization of parallel and series semiconductor devices affects the conduction loss, efficiency and power density.

A. SEMICONDUCTOR DEVICES SELECTION

The performance of the SSPC is greatly influenced by the selection of the semiconductor components, as the power loss is mainly determined by the conduction and switching characteristics of the semiconductor. SiC MOSFET modules with high power capabilities have advantageous characteristics such as low ON-state resistance, minimized conduction loss, and a higher maximum junction temperature [32]. The choice of these modules depends on their ON-state resistance and current rating. SiC discrete devices, on the other hand, are only available for low current ratings up to 125 A. Consequently, a number of parallel discrete devices must be used, leading to increased design complexity. Power modules, which offer high current ratings, are a preferable option in such cases. A survey was conducted on SiC manufacturers, including ROHM, On Semi, Cree, Infineon, Microchip, IXYS, and GeneSic. The commercial devices from these manufacturers have voltage ratings ranging from 650 V to 1.7 kV. The devices selected for this study were from Cree and Microchip due to their high current rating availability. The commonly available structure of these modules is in the form of half-bridge configurations, requiring two anti-series devices to obtain the SSPC shown in Fig. 1. Microchip also provides dual-common source modules, which can be connected as two anti-series switches, thus requiring only one module for the SSPC. Fig. 2 provides the module configurations, half-bridge and dual-common source. Table 2 gives the main specifications of the selected modules.

It is important to note that the semiconductor devices of SSPCs are normally ON during normal operation. Therefore, the predominant loss of the SSPC is the conduction loss. Since the device is only turned on or off when inserting/removing the SSPC from the circuit, the switching loss becomes negligible and can be disregarded.

B. LOSS CALCULATIONS

To determine the conduction loss of a SiC MOSFET, it is necessary to take into account the current flow and the conditions of the gate drive signal. The MOSFET can carry current in both forward and reverse directions when the gate signal is forward bias. Conversely, when the gate signal is reverse biased, only the body diode is able to conduct reverse

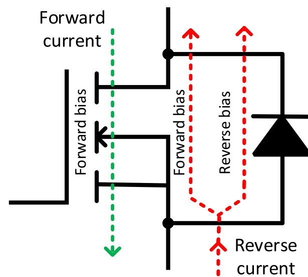

FIGURE 3. Current directions in MOSFET and its body diode.

current [33]. The current direction in the MOSFET is illustrated Fig. 3, when the gate signal is forward bias, the forward current flows through the MOSFET (as illustrated by green color), while the reverse current can flow through two paths (as illustrated by red color). At lower levels of current, the current passes through the MOSFET channel exclusively, while at higher current levels, it becomes distributed between the MOSFET channel and the body diode. The diode starts to conduct current when the voltage drop across the MOSFET goes higher than the diode threshold voltage. Normally, the reverse current does not flow through the body diode due to its relatively high threshold voltage, which typically falls within the range of 1.5 V to 3 V. As a result, the point at which current sharing (between the MOSFET channel and body diode) shifts towards higher current levels. The sharing of the reverse current I_R between the MOSFET I_{DS} and the diode I_f can be expressed by:

$$\begin{aligned} V_{DS} &= I_{DS} R_{DS-on} \\ V_{DS} &= V_{fo} + I_f R_f \\ I_R &= I_{DS} + I_f \end{aligned} \tag{1}$$

where V_{DS} is the voltage drop across the MOSFET during turn on condition. V_{fo}, and R_f donate the device threshold voltage, and ON-state resistance of the diode, respectively. R_{DS-on} represents the MOSFET ON-state resistance. The parameters V_{fo}, R_f, and R_{DS-on} can be calculated from the device datasheet according to their corresponding curves. The MOSFET generates a voltage drop V_{DS} on R_{DS-on} as the current I_{DS} passes through it, as shown in (1). Initially, the current I_f remains at zero until the voltage V_{DS} exceeds V_{fo} as the current I_R reaches a certain level, it splits between the MOSFET and the diode, with the distribution dependent on the values of V_{fo}, R_f, and R_{DS-on}. It is worth mentioning that the current will mainly go through the MOSFET rather than the diode due to high voltage drop of the diode for all selected modules in Table 2. The ON-state resistance for the MOSEFT is considered the same in both forward and the reverse conduction when calculating the conduction loss. The ON-state loss can be calculated for one switch by (2), where I_{Line} is the line current passing through the SSPC. The total conduction loss is given by (3) for n parallel channels of MOSFETs with two anti-series MOSFETs per channel. It can be seen that the total conduction loss for the MOSFET based SSPCs decrease as the number of parallel channels (n) increases.

$$P_{on} = R_{DS-on} \times (I_{Line}/n)^2 \tag{2}$$

$$P_{loss-total} = 2 \times \text{n} \times P_{on} = 2 \times R_{DS-on} \times I_{Line}^2/n \tag{3}$$

C. COOLING REQUIREMENTS

To ensure that the design keeps the junction temperature of the semiconductor devices under the maximum limit, a thermal model is needed. The junction-case thermal impedance R_{th-jc}, which is an inherent parameter specific to each device and provided in Table 2, cannot be changed. Heatsinks are typically employed to facilitate effective heat transfer from the semiconductor devices to the surrounding environment. The design, shape, and material of the heatsink naturally impact the heat transfer process. By varying the thermal impedance of the heatsink, denoted as R_{th}, the heat transfer, and the junction temperature can be regulated.

In this design, as the cooling requirements are limited to natural convection, the weight of the SSPC unit will be significant, resulting in a low power density. However, it is widely acknowledged that incorporating liquid-cooled plates or fans-based cooling can significantly reduce weight and enhance power density.

First, consider that the SSPC is designed with one channel, and assume that the SSPC modules are placed on a single heatsink, in the case of using half-bridge configuration, two modules connected in anti-series are required, resulting in the presence of four SiC MOSFETs with 4 thermal resistances, as illustrated in Fig. 4a. While in the case of using dual-common source configuration, one module is required, resulting in the presence of two SiC MOSFETs with two thermal resistances, as illustrated in Fig. 4b. Equations (4) and (5) have been used to determine the heatsink thermal impedance R_{th} and the junction temperature T_j respectively.

$$R_{th} = \frac{T_h - T_a}{P_{loss-total}} \tag{4}$$

$$T_j = P_{loss-i} \times R_{th-jc} + T_c \tag{5}$$

where $P_{loss-total}$ is the total loss of MOSFETs sharing the same heatsink unit. P_{loss-i} is the power loss of one switch. R_{th} is calculated to keep the device has T_j less than or equal to 125 °C, at 85 °C ambient temperature T_a. For simplicity, it is assumed that the heatsink temperature T_h equals case temperature T_c. Table 3 gives the calculated conduction loss; heatsink temperature and the required heatsink thermal resistance for each device for an 85 °C ambient temperature T_a. As the SSPC should handle $2\times I_{nom}$for 2 mins, the calculations given in Table 3 are based on $2\times I_{nom}$. Devices with dual-common structures have lower loss than devices with half-bridge structures due to the use of half as many series switches in the channel. Therefore, the calculated heatsink thermal resistance required for dual-common configuration is higher than that required for the devices with half-bridge

TABLE 2. The specifications of the selected modules.

Parameters	CAB450M 12XM3	MSCSM120A M042CD3AG	MSCSM70AM 025CT6LIAG	MSCSM120A M03CT6LIAG	MSCSM70DU M025AG	MSCSM70DU M017AG
Supplier	Cree	Microchip	Microchip	Microchip	Microchip	Microchip
Structure	Half-bridge	Half-bridge	Half-bridge	Half-bridge	Dual-common	Dual-common
No. Modules per branch	2	2	2	2	1	1
$R_{DS\text{-}on}$ at 25°C (mΩ)	2.6	4.2	3	2.5	2.5	1.7
$R_{DS\text{-}on}$ at 125°C (mΩ)	3.7	5.46	3.3	3.25	2.75	1.87
Current At 25°C (A)	450	495	689	805	689	454
Voltage rating V_{DS} (V)	1200	1200	700	1200	700	700
Max operating junction Temp. (°C)	150	150	150	150	150	150
Junction-case resistance $R_{th\text{-}jc}$ (°C/W)	0.13	0.074	0.08	0.047	0.08	0.055
Pulse current at Temp. of 25 °C (A)	900	990	1400	1600	1380	2000
Weight (gms)	175	350	320	320	320	320
Dimension in (mm^3)	80×53×19	62×108×14	62×108×15	62×108×16	62×108×18	62×108×19
Cost per device in (£)	740	863	812	1225	574	784

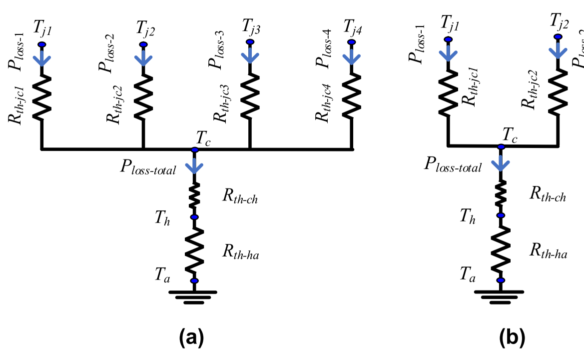

FIGURE 4. Description of thermal resistances of SSPC using half-bridge and dual-common source modules.

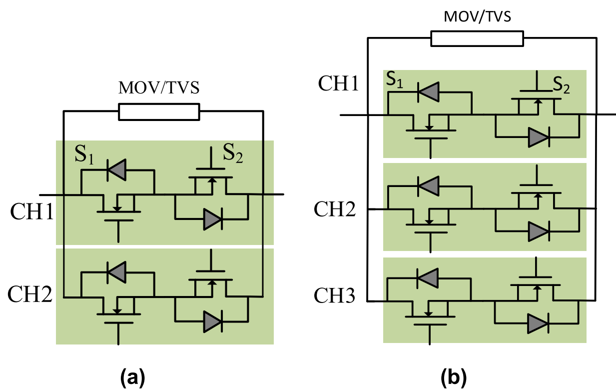

FIGURE 5. SSPC of Multiple channels, a) two channels and b) 3 channels.

configuration, which means that better cooling and reduced heatsink weight.

The results have been calculated for multiple channels, 2 and 3 channels that are illustrated in Fig. 5. From Table 3, as the number of channels increases, the power loss for each channel and the total loss decreases. As a result, the required heatsink thermal resistance will rise, resulting in a lighter heatsink. The semiconductor devices that have dual-common configuration provide the lowest conduction loss and then improved heatsink thermal resistance. The SiC dual-common MOSFET module MSCSM70DUM017AG from Microchip is considered the best choice and the dual-common MSCSM70DUM025AG is the second option.

D. HEATSINK SELECTION

In this section, the calculations were performed to determine the power loss (using (2) and (3)), heatsink temperature (using (4)), and the necessary thermal resistance of the heatsink (based on (5)) for varying configurations of SiC MOSFET modules with 1, 2, and 3 channels. Heatsink thermal resistance R_{th} is determined to keep the device has junction temperature T_j less than or equal to 125 °C, at 85 °C ambient temperature T_a. The analysis revealed that the modules featuring dual-common structures exhibit lower loss, higher thermal resistance, and lower cooling requirements compared to those with half-bridge structures. Moreover, with an increasing number of channels, the loss per channel and the overall loss both decrease, resulting in a lighter heatsink. Consequently, the dual-common SiC modules MSCSM70DUM017AG were chosen for the design of SSPC. The performance can be enhanced by adding more channels, but this improvement comes at the expense of higher costs for SiC modules and the SSPC unit. Since high current SiC modules, especially dual-common modules, are not widely available in the market, the choice of heatsink is presently limited to either 1 or 2 channels. In each scenario, the heatsink selection is based on the thermal resistance values calculated in Table 3.

Table 4 shows the product number of the selected heatsink. The approximated total weight (including heatsink and semiconductor devices weight) has been calculated for the two cases, 1 and 2 channels. For No. channel = 1, the heatsink from ABL supplier is selected, part number 177ABL with dimensions 300 × 300×83 mm^3. While for No. channel = 2, the heatsink from ABL supplier is selected, part number 180AB with dimensions 215 × 200×77 mm^3. The total

TABLE 3. The calculated power loss and heatsink requirements for different number of channels.

Parameters	CAB450M1 2XM3	MSCSM120AM04 2CD3AG	MSCSM70AM025 CT6LIAG	MSCSM120AM 03CT6LIAG	MSCSM70DU M025AG	MSCSM70DUM017 AG
$R_{DS\text{-}on}$ at 125 ºC (mΩ)	3.7	5.46	3.3	3.25	2.75	1.87
Junction to case thermal resistance $R_{th\text{-}jc}$ (ºC/W)	0.13	0.074	0.08	0.047	0.08	0.055
Num of device per module	2	2	2	2	2	2
No. modules per branch	2	2	2	2	1	1
Total number of devices per branch	4	4	4	4	2	2
Overcurrent at 2×I_{nom} (A)	250	250	250	250	250	250
Number of parallel channels = 1						
Branch power loss at I_{nom} (W)	231.3	340.6	206.3	203.1	85.9	58.4
Branch power loss at 2×I_{nom} (W)	925	1362.5	825	812.5	343.75	233.75
Total power loss at 2×I_{nom} (W)	925	1362.5	825	812.5	343.75	233.75
Heatsink Temp T_h (ºC)	94.9375	99.7938	108.5	115.4531	111.25	118.5719
Heatsink thermal resistance $R_{th\text{-}ha}$ (ºC/W)	0.0107	0.0109	0.0285	0.0375	0.0764	0.1436
Number of parallel channels = 2						
Branch power loss at I_{nom} (W)	57.8	85.2	51.6	50.8	21.5	14.6
Branch power loss at 2×I_{nom} (W)	231.25	340.625	206.25	203.125	85.9375	58.4375
Total power loss at 2×I_{nom} (W)	462.5	681.25	412.5	406.25	171.875	116.875
Heatsink Temp T_h (ºC)	117.4844	118.6984	120.875	122.6133	121.5625	123.393
Heatsink thermal resistance $R_{th\text{-}ha}$ (ºC/W)	0.0702	0.0495	0.087	0.0926	0.2127	0.3285
Number of parallel channels = 3						
Branch power loss at I_{nom} (W)	25.7	37.8	22.9	22.6	9.5	6.5
Branch power loss at 2×I_{nom} (W)	102.78	151.4	91.7	90.3	38.2	25.9
Total power loss at 2×I_{nom} (W)	308.3	454.2	275	270.8	114.6	77.9
Heatsink Temp T_h (ºC)	121.6	122.2	123.2	123.9	123.5	124.3
Heatsink thermal resistance $R_{th\text{-}ha}$ (ºC/W)	0.1189	0.0819	0.1388	0.1438	0.3358	0.5042

TABLE 4. Heatsink selection, total weight, and power density for No. Channel = 1 and 2 when using MSCSM70DUM017AG.

Parameters	Value	
No. Channel	1	2
No. Modules	1	1
Modules number	1	2
Module weight (gm)	320	320
Total module weight (gm)	320	640
Module Cost (£)	685	685
Total Modules Cost	685	1370
Calculated heatsink $R_{th\text{-}ha}$ (ºC/W)	0.143	0.326
Module dimensions (mm^3)	62×108×19	62×108×19
Supplier, product Number	ABL, 177ABL	ABL, 180ABL
Heatsink dimensions (mm^3)	300×300×83	215×200×77
Thermal resistance at natural convection (ºC/W)	0.138	0.265
Approx heatsink weight (kg)	6.76	3
Total weight (kg)	7.08	3.64
Power density (kW/kg)	4.77	9.3

weight required for number of channels = 2 is approximately 3.64 kg compared to 7.08 kg required for No. channels = 1, which considered as 48.5% weight saving.

In this work, natural convection cooling is necessary and consequently the heatsink will have a significant weight. However, if a fan or liquid cooled plate were used instead, the weight could be greatly reduced, resulting in a higher power density. For example, if we use the liquid cold plate Wakefield-Vette180-20-6C, which weighs 500 gm, this will result in a power density of over 30 kW/kg for the required power rating 33.75 kW for an SSPC with two channels. However, since the plate thermal resistance is 0.038 °C/W, the power rating would increase to 55 kW, resulting in a power density of 50 kW/kg.

E. SIMULATION RESULTS

PLECS software was used to carry out a thermal simulation of the SSPC. The objective of the simulation was to assess the thermal performance during steady-state performance of the SSPC and its behaviour when subjected to over-current conditions, specifically at 2× I_{nom} continuing for 2 mins. The schematic of the system is shown in Fig. 6. The inductance L_{DC} and resistance R_{DC} represent the inductance and resistance of the DC-bus and parasitic wiring found within the system, and R_{Load} represents a steady state load. The fault is imposed with series resistance to limit the fault current to 2× I_{nom}. The circuit parameters are given in Table 5.

In the first scenario, the simulation focused on a single module/channel with a heatsink of a thermal resistance of 0.138 °C/W (Table 4). As shown in Fig. 7, under steady-state conditions and at the nominal current, each MOSFET device exhibited a power loss of approximately 29 W, resulting in a total loss of 58 W. This caused the temperature of the heatsink

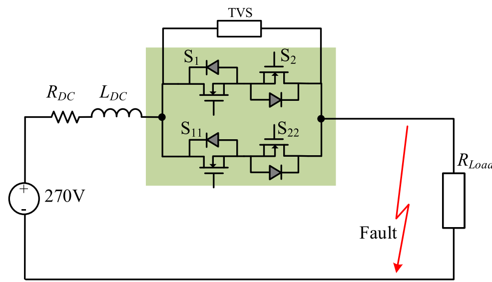

FIGURE 6. Schematic diagram of bidirectional SSPC with the 270 VDC.

TABLE 5. The simulation test parameters of SSPC.

Components	Parameters
DC voltage V_{DC}	270 V
Nominal current I_{nom}	125 A
Line inductance L_{DC}	100 µH
Line resistance R_{DC}	100 mΩ
Load resistance R_L	2.16 Ω
SiC MOSFET Module	MSCSM70DUM017AG
Junction-case thermal resistance $R_{th\text{-}jc}$	0.055 °C/W

to rise to 93 °C. When the current increases to twice the nominal value, the total power loss increases to around 240 W. Thus, the temperature of the heatsink rose to 118 °C, and the junction temperature of the device reached 123 °C. The simulation results match perfectly with those calculated in Table 3.

In the next case, two modules were connected in parallel, assuming the utilization of a heatsink assembly with a thermal resistance of 0.264 °C/W (Table 4). As shown in Fig. 8, at the nominal current, each MOSFET device experienced a power loss of approximately 7.25 W, leading to a channel loss of 14 W and a total loss of 28 W. Consequently, the temperature of the heatsink rose to 92 °C. Under over-current conditions (twice the nominal current), the total power loss increased to approximately 120 W. This resulted in a temperature rise of the heatsink to 115 °C, while the junction temperature of the device reached 118 °C.

In conclusion, by doubling the number of parallel modules, the power loss was halved, leading to improved cooling requirements. Furthermore, this will lead to a 48.5% reduction in weight (considering both the heatsink and semiconductor components), and a 55.5% decrease in volume, taking the heatsink into account. However, it is worth to note that these benefits will come at the expense of increased overall cost, as the semiconductor expenses will be doubled.

IV. OVERVOLTAGE PROTECTION SCHEME AND INRUSH CURRENT LIMITING

A. OVERVOLTAGE PROTECTION SCHEME

The function of the SSPC is to connect/disconnect the load from the 270VDC distribution bus; the simplified schematic of the system is shown in Fig. 6. The SSPC must be capable of dissipating the inductive energy during turn-off and

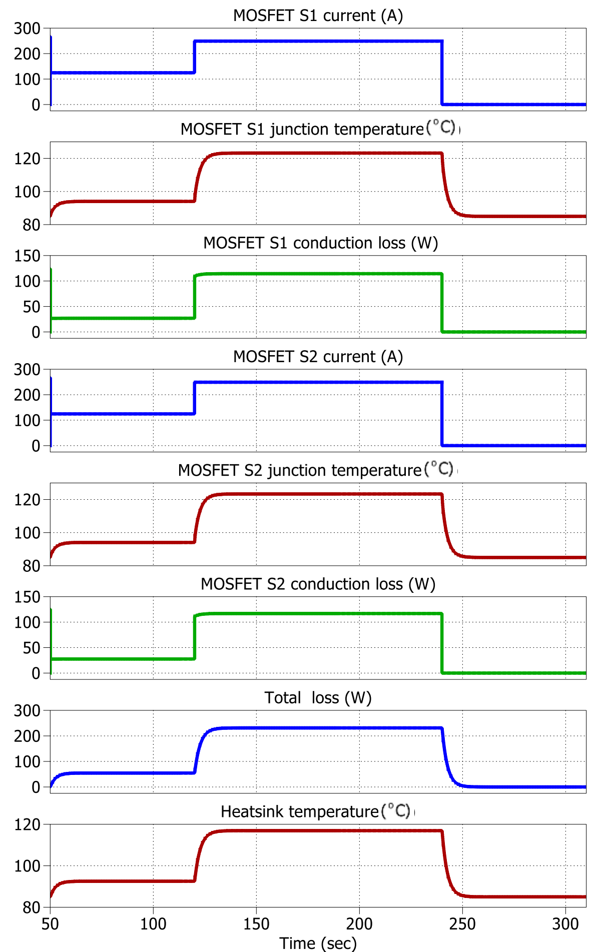

FIGURE 7. Simulation results of the junction and heatsink temperatures and loss for No. channels = 1.

over current tripping. If this voltage surge is not adequately suppressed, the SSPC may experience failure, which would subsequently impact the entire EPS. To prevent overvoltage, various protective devices can be employed. These options include transient voltage suppression (TVS) diodes, metal-oxide varistors (MOV), as well as snubber circuits such as RC, and RCD configurations.

As TVS devices are commonly used in aerospace applications due to their reliability at high operating temperatures [20], a TVS device has been selected for this design. Fig. 9 shows the SSPC current and the voltage during the fault condition. The below description explains the functioning of a SSPC with TVS diodes operating in the event of a fault.

- At time t_0, a fault occurs across the load, causing the line current (I_{Line}) to increase.
- As the fault current rises, it eventually reaches the over-current (I_{OC}, threshold current) at time t_1. This triggers the SSPC to open and disconnect the load.
- Due to the rapid change in current (di/dt) across the circuit's inductance L_{DC}, an overvoltage occurs at the SSPC terminals. The overvoltage activates the TVS

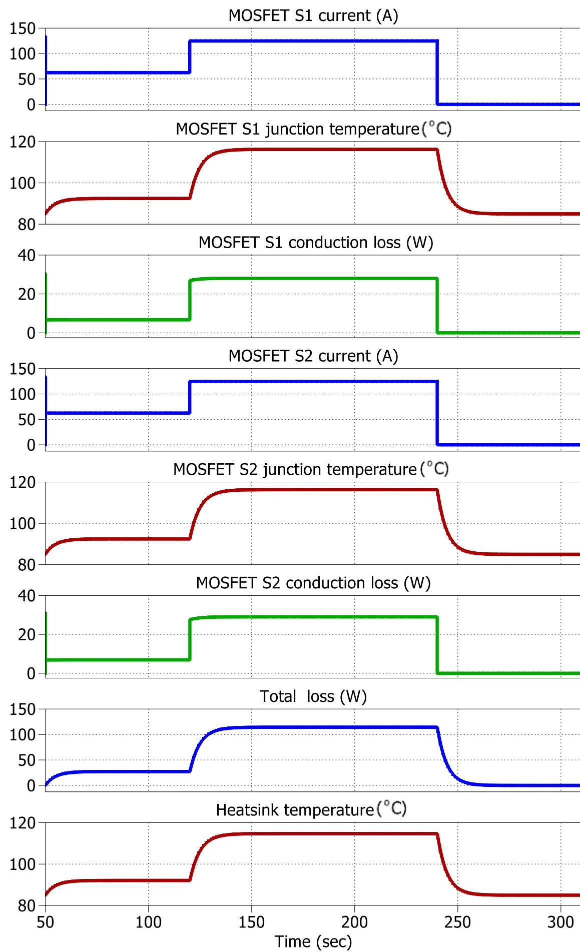

FIGURE 8. Simulation results of the junction and heatsink temperatures and loss for No. channels = 2.

diodes, causing them to enter avalanche breakdown. This limits the voltage across the SSPC. The TVS diodes remain in avalanche breakdown as the current transitions from the SiC MOSFET modules to the TVS diodes.

- The avalanche breakdown of the TVS diodes continues until the fault current reaches zero at time t_2.
- At t_2, the TVS diodes exit avalanche breakdown, and the SSPC blocks the DC voltage until the fault across the load is cleared.

Equation (6) can be used to estimate the time it takes for the fault current to reach zero (Δt):

$$\Delta t = t_2 - t_1 = \frac{L_{DC} \times I_{OC}}{V_{Cl-min} - V_{DC}} \tag{6}$$

By substituting in the appropriate values into the formula, Δt can be calculated and the time needed for the fault current to return to zero during the circuit operation determined. Increasing the clamping voltage reduces the time needed to drive I_{Line} to zero but increases the voltage stress on the MOSFETs. When selecting TVS diodes, certain design guidelines should be followed. The minimum reverse breakdown voltage of the TVS diodes should be higher than the DC voltage.

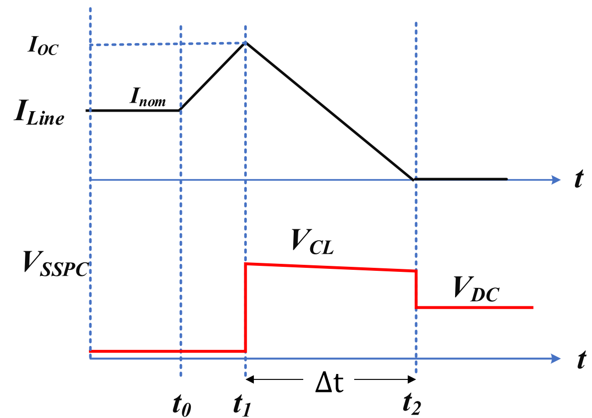

FIGURE 9. The waveforms for fault transient for SSPC using TVS diode.

The minimum clamping voltage should be greater than the nominal bus voltage but lower than the MOSFET maximum voltage rating. It should also exceed the limits of overvoltage or transient condition that may occur in the DC bus. For a 270 V bus voltage, the maximum overshot voltage is 350V according to the MIL-STD-704F standard [34]. The acceptable peak clamp voltage ranges from 1.5 - 2 times the DC bus voltage. Finally, the TVS diodes instantaneous peak power and energy should not exceed the device limits.

The Little-fuse Company offers the AK10-380C TVS bidirectional diode [35], with following specifications: 1) The TVS diode has a peak pulse current rating of 10 kA, 2) the standoff voltage is 380 V, thus the TVS diode can handle a voltage stress of 270 V when the SSPC is open, 3) the breakdown voltage (V_{br}) falls in the range of 401 V - 443 V, and 4) the maximum clamping voltage (V_{cl-max}) is 520 V at 10 kA maximum pulse current. The calculated clamping voltage range of the TVS diode is 416 V to 452 V, determined from (7) when the short circuit current I_{cl} is 1.25 kA. The maximum clamped voltage of 452 V which provides a 33% safety margin to the selected 700 V power modules.

$$V_{Cl} = \frac{V_{Cl-max} - V_{br}}{10kA} * I_{Cl} + V_{br} \tag{7}$$

The peak pulse power reaches 520 kW with a maximum current of 1.25 kA and a minimum clamping voltage of 415V. For line inductance of 20 μH, the required pulse width is calculated using (6), which is 172 μs.

TVS diode datasheet gives peak pulse power ratings based on the 8/20 μs or 10/1000 μs double exponential current waveform. However, in certain applications like SSPCs, the current waveform may be sawtooth or triangular. In the case of the double exponential curve, the withstand time is defined as the period in which the current reduces to half of its maximum value. Conversely, for the sawtooth curve, the withstand time is defined as the period in which the current decreases to zero. To address the variance between the actual sawtooth waveform and the specified exponential waveform, a normalization factor of 2.8 is used [17], [36]. The pulse power curve from TVS datasheet is redrawn considering the

factor 2.8 as shown in Fig. 10, where the actual exponential curve is represented by the blue curve and the red one represents the sawtooth curve.

When the peak pulse power reaches 520 kW, the pulse width that the device can endure is approximately 625 μs. This duration is roughly 3.6 times longer than the necessary time, indicating that the energy absorption requirement can be comfortably fulfilled. This excess energy margin permits the SSPC to operate in a different system with either 3.6 times the line inductance or 3.6 times the peak current.

B. INRUSH CURRENT LIMITING

Capacitive loads are frequently encountered in the MEA distribution system, resulting in the occurrence of inrush currents flowing through the SSPC during turn on. In such cases, it is crucial to address the issue of the inrush current that needs to be limited. To limit this inrush current, it becomes essential to implement a soft start-up scheme that regulates the rate at which the input current changes. There exist several methods to mitigate the inrush current problem as follows. These various solutions will be evaluated and considered in more detail in our extension research.

- The use of a pre-charge resistor [37], [38].
- Gradual ramping of the gate drive voltage using an RC network [39].
- Multiple switches operate in a phase-shifted sequence incorporating current limiting measures [40].

V. TEST CIRCUITS AND EXPERIMENTAL RESULTS

The SSPC has been built to verify the analysis and simulations that have been described in the previous sections. The top and side views of the SSPC prototype are illustrated in Fig. 11. The main hardware components used are presented in Table 6. The DC source is formed using the parallel connection of two 15 kW bi-directional power supplies PSI 9360-120 when needed, each with a maximum current of 120 A.

The SSPCs were evaluated for their thermal capabilities for steady state test under two different levels of current: the nominal current I_{nom} of 120 A and 2 times I_{nom} which is 240 A. To test the turning off mechanism, the SSPCs were subjected to current levels of $2\times I_{nom}$ (~240 A) and $3\times I_{nom}$ (~370 A).

To conduct a steady state test, the SSPC terminals were connected in a short-circuit configuration. A low-voltage high-current DC source is used to maintain current regulation through the SSPC, which functions in current limiting mode. Fig. 12(a) provides a diagram of the steady-state test circuit. The amount of conduction loss in the SSPC is equal to that of a 33.75 kW load and a 67.5 kW load when operating with a current of 120 A and 2 × 120 A respectively. The results have been downloaded from the 200 MHz oscilloscope as Excel files which are re-drawn using MATLAB.

The first steady-state test case involves testing the SSPC at its nominal current rating $I_{nom} = 120$ A (maximum current rating of the DC supply). This is done to ensure that the SSPC can operate reliably and safely at its designed level. Fig. 13 shows the steady state experimental result of continuous current of 120 A, including the line current, and the voltage

TABLE 6. The main components of SSPC.

Components	Part number (Features)
Power Modules	MSCSM70DUM017AG (Dual common, Small ON-state resistance)
TVS diode	AK10-380C (Min V_{br} = 401 V)
Heatsink	ABL 180ABL (Market available)
Current sensor	L34S1T0D15T (Max operating Temp. 105 ºC)
Voltage and Temp. sensors IC	ACPL-C87AT (Optically Isolated Amplifiers), OPA237UA (Op Amps)
Gate drive IC	IXDN630CI, Si8261BCD-C-IS
NTC thermistor	NTCALUG01A103F161 (Max operating Temp. 150 ºC)

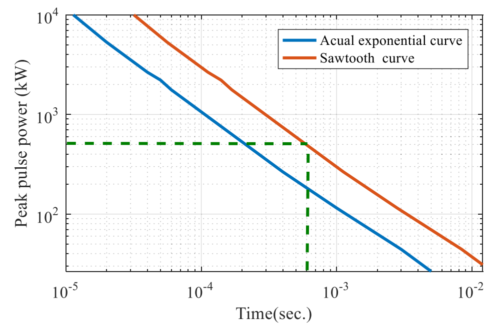

FIGURE 10. Typical dissipation power of AK10-380C diode.

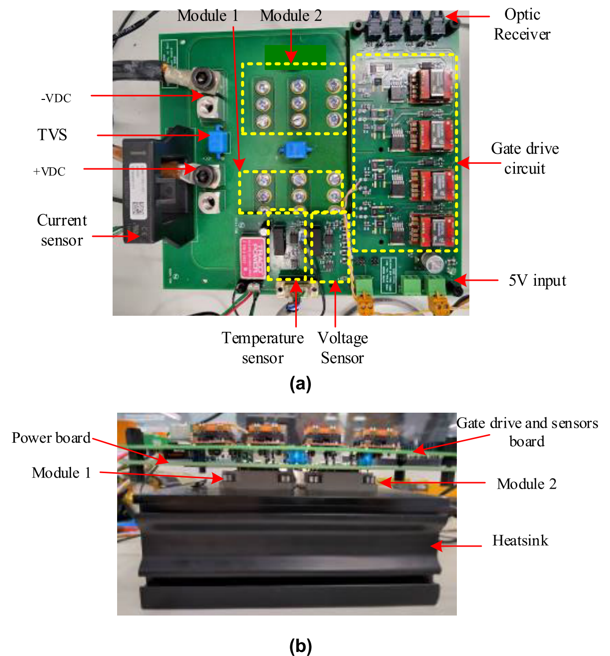

FIGURE 11. Laboratory prototype of SSPC, a) Top view and b) side view.

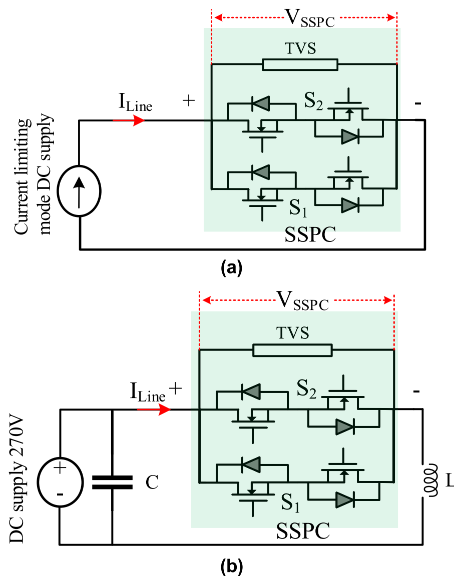

FIGURE 12. Circuit diagram of the test circuits a) Steady state test, and b) turn-off test.

drop measured on the SSPC terminals. The voltage drop of the SSPC is approximately 0.1885 V giving a conduction loss for the SSPC equals 0.1885 × 120 A = 22.6 W, the efficiency is 99.9%. This has been achieved due to the low on state resistance and dual-common source devices in the chosen semiconductor module.

The second steady-state test case involves testing the component at twice the nominal current $2\times I_{nom} \sim= 240$ A (two parallel DC supplies). This is done to verify that the component can withstand higher current levels and that it can operate continuously at this level for 2 mins, as per the requirements. Fig. 14 shows the steady state experimental result of turning on SSPC with continuous current of 240 A, including line current, and the voltage drop measured on the SSPC terminals. The voltage drop of the SSPC is approximately 0.38 V, giving a loss for the SSPC of 0.38 × 240 A = 91.2 W. The third steady-state test case involves testing the component with only one of its parallel modules turned on, at rated current of 120 A, as illustrated in Fig. 15. This is done to illustrate that with using two parallel modules can reduce power loss and increase efficiency, and to show the function of controlling each module by itself. The voltage drop of the SSPC is approximately 0.377 V giving a conduction loss for the SSPC of 0.377 × 240 A = 45 W, and then the efficiency is 99.85%. By comparing the power loss of the single-module configuration to that of the two parallel channels, it can be shown how the parallel configuration improves the performance.

The temperature rises of the heatsink can be approximately calculated by multiplying the power loss by the heatsink thermal resistance of 0.26 °C/W. The thermal status of the SSPC heatsink after continuous operation for 30 mins with currents of 120 A, 240 A, and 120 A (with only one module turned on) is shown in Fig. 16. The heatsink temperatures were measured

TABLE 7. Comparative evaluation of steady state test cases.

Test cases	1st test at 120A	2nd Test at 240A	3rd Test at 120A (one channel)
No. channels	2	2	1
Current /channel (A)	60	120	120
Voltage drop (V)	0.1885	0.38	0.377
Conduction Loss (W)	22.6	91.2	45
Heatsink Temp. (°C)	31.9	51.7	35
PCB temperature (°C)	-	49.3	

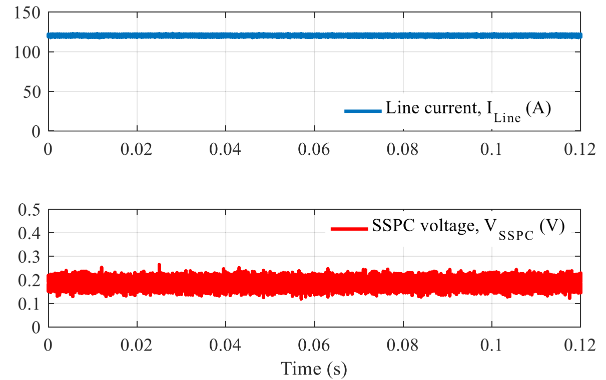

FIGURE 13. The steady state experimental result of SSPC with continuous current of 120 A.

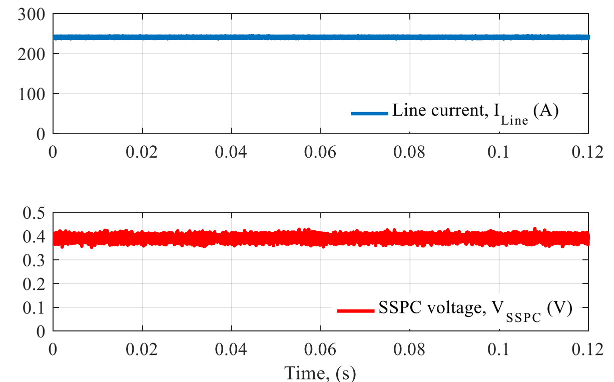

FIGURE 14. The steady state experimental result of SSPC with continuous current of 240 A.

at 31.9°C, 51.7°C, and 35°C, respectively, with an ambient temperature of 25°C. For a continuous current of 240 A, the PCB temperature is slightly lower at 49.3°C in steady state, as shown in Fig. 16(d). Table 7 summarizes the three steady state test cases.

The first turn-off test is performed at twice the nominal current (240 A), using two power supplies of PSI 9360-120 in parallel to generate the required current. To avoid high-power loads, two power supplies with a voltage of 270 V are used to provide a pulse current of 240 A for 500 ms, with a load of 0.3 Ω. The line inductance is 105 μH, which represents the inductances of the DC-bus and parasitic wiring found within the system. The test circuit diagram is shown

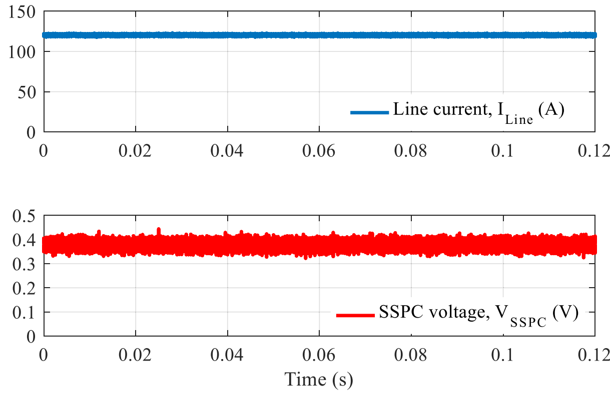

FIGURE 15. The steady state experimental result of SSPC with continuous current of 120 A using one channel.

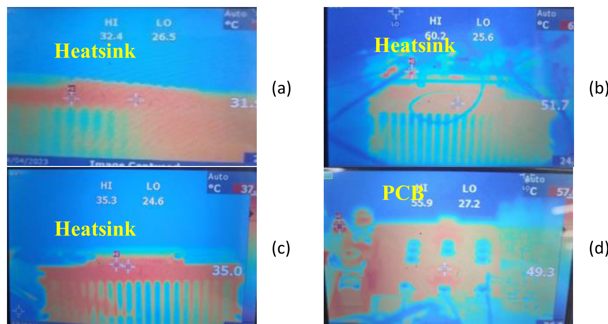

FIGURE 16. Thermal images of the heatsink at: a) 120 A, b) 240 A, c) 120 A one channel, and d) and PCB at 240 A.

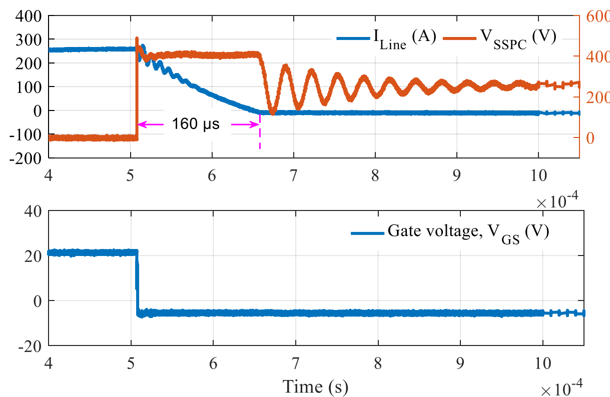

FIGURE 17. Turn-off process at 2 times I_{nom} (240 A).

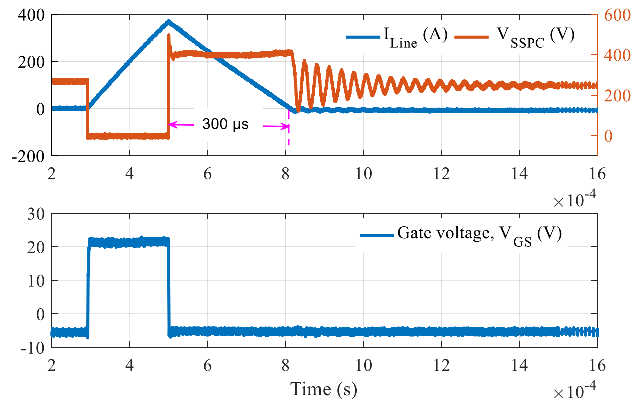

FIGURE 18. Turn-off process at 3 times I_{nom} (370 A).

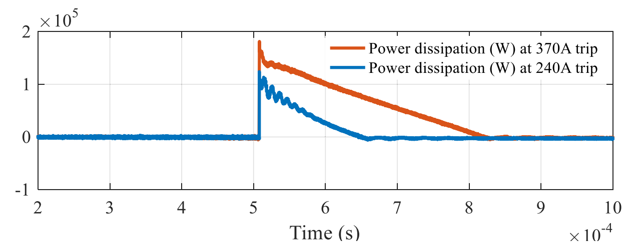

FIGURE 19. The dissipated power of the circuit for turning off 240 A (blue) and 370 A (red).

TABLE 8. Comparative evaluation of turn-off test cases.

Test cases	Turn-off test at at 240 A	Turn-off test at 370 A
Current /channel (A)	240	370
Clamping voltage V_{Cl} (Avg.) (V)	404	405
Clamping voltage V_{Cl} (Max.) (V)	470	480
Peak Power (kW)	96.9	149.8
Turn-off time (µs)	160	300
Dissipated energy (J)	7.7	22.5

TABLE 9. SSPC specification based on the approximated parameters.

Parameter	Value	Parameter	Value
Loss (W)	22.5	Weight (kg)	4.2
Efficiency (%)	99.85	Power density (kW/kg)	8.2
Cost (£)	1470	Volume (mm^3)	215×200×127

in Fig. 6. Fig. 17 shows the line current, SSPC voltage and gate drive signal when interrupting current of 240 A. The interruption of the current causes an overvoltage across the SSPC, which is clamped by the TVS devices. The average voltage is around 404 V which is like the level calculated from (7) at current 240 A trip. The maximum voltage across the SSPC is limited to 470 V. The resulting in a power dissipation of equal 96.9 kW. The fault is extinguished within 160 μs, and the estimated energy dissipation is 7.7 J.

The second test was conducted at a current of 370 A (∼3 times the nominal current), which is achieved by charging a capacitor to provide the necessary current through the 105 μH inductor for a specified turn-on time for the SSPC. The test circuit diagram for this case is shown in Fig. 12(b). Fig. 18 shows the line current, SSPC voltage and gate drive signal when interrupting current of 370 A. The average voltage is around 405 V which is quite similar to the one calculated from (7) at current 370 A trip. The maximum voltage across the SSPC is limited to 480 V and the

estimated power dissipation is 149.8 kW. The fault is resolved within 300 μs which is slightly longer than the calculated time of 287 μs that obtained from (6) for a 370 A. It is worth noting that equation (6) considers the time necessary for the average voltage to remain at 405 V until the current reaches zero. The 13 μs difference between the calculated and the experimental time is due to the transition time of the SSPC from its maximum voltage value of 480 V to the average clamping value of 405 V resulting in an additional delay, which is not considered in (6) [17]. The estimated energy dissipation in this case is 22.5 J, which considered higher than any design in the previous research [29]. Fig. 19 shows the dissipated power of the circuit for turning off 240 A (blue) and 370 A (red), which obtained by multiplying the corresponding SSPC voltage and line current for each case given in Fig. 17 and Fig. 18. Table 8 summarizes the turn-off test cases.

Table 9 provides the specifications of the SSPC unit. This includes the loss, efficiency at 270 V and 125 A, as well as the cost, weight ((Natural convection) 180ABL), power density, and volume, including both the semiconductor devices and the heatsink.

To conclude, these tests demonstrate the ability of the SSPC to interrupt current under high load conditions and disconnect it effectively. The clamping action of the TVS devices ensures that the overvoltage across the SSPC is limited, which prevents damage to the SSPC and other components in the system.

VI. CONCLUSION

This paper presents the design of a 270 V, 125 A / 250 A bidirectional DC SSPC for MEA applications. The paper provides a comprehensive explanation of the electrical design of the SSPC, highlighting the use of SiC power modules and TVS diodes in the selection process. The study involved analyzing the impact of varying the number of channels on the heatsink size, thermal resistance, and circuit temperature. Numerous factors were considered, such as conduction loss, maximum junction temperature, heatsink temperature, power density, and weight. To validate the steady-state loss and temperature rise resulting from the switches' conduction loss, both simulation studies and hardware experiments were conducted. The test cases included operation at the nominal current using one module, the nominal current using two modules in parallel and running at twice as the nominal current for a period of 2 mins as well. For the case of the nominal current, the SSPC using one module has a nominal power loss of 58 W (simulation) and 45 W (experiment). The SSPC using two parallel modules has a heat dissipation of 29 W (simulation) and 22.7 W (experiment). The difference between the simulation and experimental results is owing to the different test conditions of the ambient operating temperature which leads to different on state resistance. Moreover, the theoretical and simulated outcomes were obtained under a nominal current of 125 A, while the experimental results at 120 A due to power supply availabilities. The overvoltage protection depended on using TVS diodes. This protection circuit limits the voltage stress across the SSPCs to 480 V (as a maximum value). Furthermore, the designed SSPCs are capable of tripping at a current of 240 A and 370 A within 160 μs and 300 μs, respectively, for line inductance of 105 μH. The experimental results show that the circuit can withstand high energy of 22.5 J at a breaking current of 370 A, which is higher than the counterparts in the review.

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