Enhanced Switching in Solid Polymer Electrolyte Memristor Devices via the addition of Interfacial Barriers and Quantum Dots

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Abstract - We report on the electrical effects of single and double polymer (polymethacrylate) barriers on polyethylene oxide (PEO) based memristors. The single barrier device with an active layer embedded with WS_2 quantum dots is also investigated. The addition of a single PMA barrier yields multi cross point current-voltage hysteresis while the addition of embedded quantum dots removes multi-cross point behavior and shows repeatable uni-polar switching with the device starting in the low resistive state (LRS). The device shows some capability of reversible unipolar to bipolar operation as a function of applied voltage and device rest time. The addition of a double PMA barrier produces a reproducible unipolar switching behavior and a unipolar negative differential resistance behavior at higher voltage operation.

CCS CONCEPTS • Computing Hardware • Emerging Memory

Additional Keywords and Phrases: Memristors, Polymer Electronics, Polyethylene Oxide (PEO), Polymethacrylate (PMA)

1 INTRODUCTION

The memristor concept by Leon Chua and breakthrough 15 years ago by HP labs led to a massive resurgence in the field of dynamical non-volatile and volatile resistive memory devices. A vast array of device capabilities is needed to meet the memory demands of the future. In neuromorphic computing, applications require reliable non-volatile memory storage, reliable volatile access devices for memory[7], flexible memristors and multi-functional devices with lower power consumption. Highly non-linear volatile memristors can also be used as a selector to solve the sneak-path problem[8] whilst a more gradual changing memristor can be used in circuits and spiking systems to imitate neurons and synapses. Many materials have been explored to create reliable memristive switching for these reasons, including metal oxides[1], polymers[2], transition metal dichalcogenides[3][4] and graphene-based materials [5][6].

Solid polymer electrolyte (SPE) devices are good candidates for "green electronics". Conductive bridge random access memory (CBRAM) made from poly-ethylene oxide (PEO) act as reliable memristors[9] compared to other polymer devices, with the benefits of low cost and simple fabrication. PEO is water soluble and non-toxic and can easily be integrated with other materials/dopants to give multifunctional switching properties. Device switching properties include low switching voltages, high on/off ratios, forming free use with high or low compliance current (CC) operation leading to non-volatile or volatile memory capabilities respectively. The optimization of this material is therefore desirable.

The incorporation of quantum dots (QDs) into polymer materials is seen as a potentially important route to multi-modal device properties. For example, QDs have optical responses that can modulate electrical switching of memristors, leading to the potential development of fast vision memristor cameras with highly specific wavelength dependence [10]. Although work in the field is at a preliminary stage, tungsten disulphide QDs embedded in polymers have shown non-volatile memory operation[11] whilst more recently negative differential resistance (NDR) has been reported in a cysteine functionalised WS_2 QD memristor device[12]. NDR characteristics are becoming increasingly important for use as nano-scale oscillators in neuromorphic computing applications[13].

Interface engineering is seen as a key approach to improving reliability and modulating device volatility. Tunnel barriers in a memristor create an intrinsic current compliance that improves cyclic endurance and memory retention [14]. Conventionally, tunnel barriers are made from metal oxides while the use of polymer barriers in memristor research is not widely reported. This research focusses on poly-methyl acrylate (PMA) as a barrier material. PMA is attractive as it is solution processable and easily deposited using spin-coating. Polymer barriers have the advantage of being interrogatable with existing flexible electronics and since polymers also permit the diffusion of ions and in some cases functional molecular species, polymer barriers could provide the means to tailor the volatility of neuromorphic memristor devices, providing short term or long-term memory dynamics by modulating the formation and rupture of conductive filaments.

2 FABRICATION METHODOLGY

The memristor crossbar devices were fabricated on glass substrates (25 mm x 25 mm) with a vertical sandwich-style architecture, as shown in Fig.1a. The glass was chemically cleaned via sonication in acetone, methanol, ethyl lactate, isopropanol, and DI water for 15 minutes each, followed by ozone cleaning (Ossila UV Ozone) for 5 minutes. Bottom electrodes were patterned via thermal evaporation (Edwards Auto 306). The poly-ethylene oxide (PEO) switching layer, 2% PEO (Sigma Aldrich Mw 600,000) solution by weight, was prepared by adding 0.2 g PEO to 4.8ml (4.8 g) of high purity de-ionised water. This was stirred on a hot plate at 40˚ C for 24 hrs at 500 rpm. The poly methacrylic acid (PMA) barrier layer, 3 mg/ml PMA, was created by adding 12 mg PMA (Scientific Polymer) to 4 g (4 ml) of ethanol. The quantum dot (QD) layer consisted of WS_2 QDs (Sigma Aldrich) dispersed in PEO with a concentration of 0.01mg/ml 2%. All solutions were de-gassed in a sonicater for 15 mins. Undoped and QD doped solutions were spin coated onto substrates at

1250 rpm for 60 s (thickness ≈125 nm) followed by a dehydration bake in an extraction oven at 95˚ C for 2 hrs. The PMA barriers were spin coated at 3000 rpm for 30 s (thickness ≈ 10 nm) and allowed to dry before addition of the active layers. Dual barrier devices underwent a second PMA coating before the addition of Ti top electrodes (50 nm), patterned via a shadow mask and deposited via thermal evaporation. A Keithley 2400 was used for electrical characterization.

3 RESULTS

A range of Ti-PEO-Ti devices with and without single and double PMA barriers, Fig.1a, were explored and electrically characterized. Fig. 1b shows typical I-V sweeps for a device containing no barriers. The pinched hysteresis loop, the signature behavior of a memristor, illustrates the bi-polar nature of the device. No forming step was needed to initiate switching and the device in its pristine condition was in the low resistive state (LRS), which is not common for memristors.

The addition of single and double barriers into the device significantly changed the I-V characteristic with all showing vertical lines at the end of the sweep, indicating intrinsic volatility. The addition of a single barrier, Fig.1c, results in a much lower operation current (nA) even at high voltage, which is expected for the insertion of an insulating barrier.

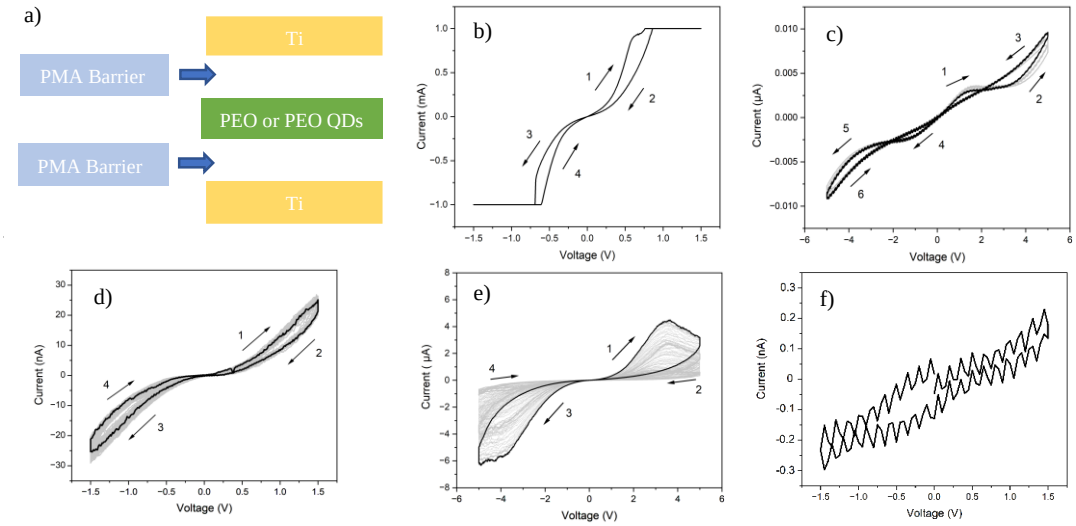

Fig. 1 a) Device schematic, b) I-V properties of a device containing no barrier layer (Ti-PEO-Ti) and showing bipolar memristor properties. (CC = 1mA), c) I-V sweeps (3 cycles) of a device with a single 10nm PMA barrier (Ti-PMA-PEO-Ti) and showing a triple cross point hysteresis curve and significantly reduce nanoamp current. D) I-V sweeps (25 cycles) of a double barrier device (Ti-PMA-PEO-PMA-Ti) and showing highly reproducible unipolar volatile switching, e) Repeated I-V sweeps over a higher voltage range (5 V) on a double barrier device. f) I-V properties of the control device (Ti-PMA [10 nm]-Ti).

Additionally, triple or double cross-points are observed among devices, indicating that the PMA barrier creates an intrinsic capacitance. In contrast, a double barrier device produced similarly low operation current (nA) but instead single unipolar hysteresis over a low voltage range, Fig.1d. To explore the I-V properties of device in the high voltage regime the voltage range was extended to ± 5 V. Fig 1e. shows a substantial increase in the operating current (μA) and the same unipolar behavior but with an enhanced hysteresis. However, over repeated sweeps (50 cycles) the output current diminished,

indicating aging. A PMA barrier control device was made consisting of just a single layer of PMA, Fig.1f. Only a very small current was observed, indicating the formation of a good insulating barrier. The oscillations are electronic noise.

QDs allows the possibility to exploit NDR responses for nano-oscillating applications or controllable discrete energy levels for photonic applications. Here WS_2 QDs suspended in the PEO layer, with and without PMA barriers, were explored. The reference device in Fig. 2a has similar characteristics to the original PEO device shown in Fig. 1a, except for a larger hysteresis and an initial HRS state. Fig. 2b shows the I-V sweep of a PEO-WS_2 QD active layer device with a single PMA barrier, Ti-PMA PEO(QD)-Ti. The I-V sweep show repeatable and reproducible unipolar volatile switching behavior. This was observed across similar devices on the same chip and multiple chips with the same structure. Fig. 2c shows I-V properties of the same device but with sweeps to a much higher voltage, ± 5.0 V. It was observed that the nature of the switching changed from unipolar volatile switching to bipolar memristor switching. The device was left for a period from 24 hrs up to a week and the typical unipolar characteristics were re-observable at a low voltage sweep from 1.5 V to - 1.5 V. This illustrates the controllable reversable switching behavior between uni-polar volatile and bi-polar memristor switching, although further work must be done to understand the mechanism involved. The endurance PEO-QD bipolar device (Fig. 2e) showed higher stability that the PEO-QD unipolar device (Fig. 2f) over 100 iterations. The noise and low separation of the resistance states points to the device high volatility in operation.

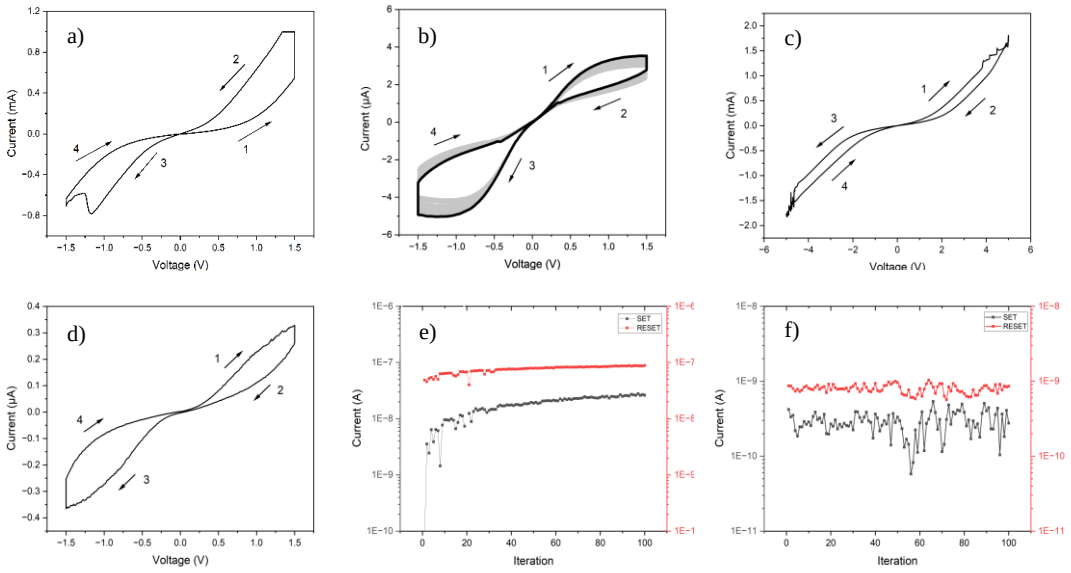

Fig 2. a) I-V properties of a QD memristor (Ti-PEO(QDs)-Ti) with bi-polar non-volatile switching b) Uni-polar volatile switching (50 cycles) in a single barrier device (Ti-PMA-PEO(QD)-Ti). c) Higher voltage switching (±5 V range) in a single barrier device. d) Uni-polar behavior observed once again after resting (±1.5 V range). e) Endurance (100 iterations) of the bipolar device (SET/RESET = ± 5V). f) Endurance (100 iterations) of the unipolar device (SET/RESET = + 1.5 V/0 V).

4 DISCUSSION

The conduction mechanism of PEO memristors is expected to be from a mixed contribution of ohmic transport and space charge limited conduction in the PEO active layer[9]. While cysteine functionalized WS_2 QDs/polymer device conduction is cited to be a consequence of tunnelling transport and transport via empty trapping states, which can lead to NDR at low voltage operation[12]. Our results show a variety of interesting effects with the addition of interfacial barriers and quantum dots into polymer PEO devices. With the addition of a single polymer PMA barrier, a triple-cross point hysteresis curve is observed in the I-V properties, Fig 1c. Some devices with this structure also showed non-zero double cross-point hysteresis, and this was highly reproducible over many cycles. The latter effect has been observed in other bulk memristor materials[4] and notably in monolayer transition metal dichalcogenide active layers[16], but have not been widely reported in SPE memristors. The nature of the double cross-point hysteresis has been speculated to come from an intrinsic capacitance built into the system, widely accepted to be parasitic capacitance caused by the vertical parallel-plate capacitor like structure separated by the dielectric active layer. The likely mechanism of this parasitic effect is attributed to large negative and positive ion build up on the interface between the active layer and the electrodes. Equivalent circuit models have been proposed to explain this I-V response with an ideal memristor and capacitor arranged in parallel[17]. In this case however the model would need to be modified because of the additional thin film insulating barrier, poly methacrylic acid[18].

The transition from bipolar operation, Fig.2a, to unipolar operation, Fig.2b, in the QD devices is likely caused by the same mechanism as that in the non-QDs devices (Fig.1b and Fig.1c), whereby the insertion of the insulating PMA barrier acts to inhibit formation of a robust conductive filament (CF). A filament that doesn't easily degrade is necessary for non-volatile memory operation. The volatile behavior of memristors has generally been attributed to the size of the CF with a lower width leading to quicker spontaneous rupture[19]. A key observation across the QD devices is the reversible and repeatable process of changing between uni-polar and bi-polar switching regimes as the maximum sweep voltage is increased, Fig.2b and 2c. A range of voltages were explored to discern the voltage required to switching to bipolar behavior and it was found in general that operating the device with a 4 V range and above was required. The switching process may be attributed to changes in the PMA layer since this is the layer that limits the current the most. These changes in the PMA layer likely continue since repeated sweeps are no longer uniform. The switch from bi-polar to uni-polar operation is reversible but only after a long time without device operation, the minimum time observed being 24 hours. Multiple devices exhibited this behavior and there was a common trend that the uni-polar operation current was always at least a factor of 10 lower in comparison to the uni-polar operating current before bipolar switching was induced in the device. The lower output current could possibly be attributed to field-driven surface diffusion that forms defects (holes) in the Ti electrodes making it more difficult for new conductive filaments (CF) to form across the device junction [19].

A double polymer barrier device was investigated. The device exhibited unipolar behavior across both low (±1.5 V) and high (± 5 V) voltage sweep ranges. At low voltage the current consistently stayed within the nA range, whilst the 5V sweep had a much higher current and increased hysteresis of the memristor curve. This is likely attributed to the much higher current limiting from the addition of 2 barriers either side of the active layer compared to PEO alone. The double barrier device suffered from increased aging at higher voltage sweeps, however the uni-polar behavior was still present after 50 cycles. Further work is required to optimise this device for improved repeatability and performance.

5 CONCLUSIONS

The work has shown the effect of PMA interfacial barriers and WS_2 quantum dots embedded in PEO based memristors. A single PMA barrier adds multi or triple cross points to the current-voltage response of the device while the addition of a

single barrier with embedded QDs removes multi-cross point behavior. The device with the addition of single barrier and QDs can reversibly change between uni-polar and bi-polar operation when operated at low or high voltage respectively and allowed to relax for a minimum of 24 hrs between operation. The addition of a double physical barrier yields uni-polar negative differential resistance at higher voltage operation which could have potential for use as nano-scale oscillators for neuromorphic computing applications. Overall, the tailoring of the volatility of devices and their operation modes could be used for short term or long-term memory along with a variety of other dynamical memory applications.

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