

Article

A Novel Multiport DC-DC Converter for Enhancing the Design and Performance of Battery–Supercapacitor Hybrid Energy Storage Systems for Unmanned Aerial Vehicles

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Abstract: This paper proposes an integrated multiport non-isolated DC–DC converter system for integrating battery–supercapacitor hybrid energy storage with photovoltaics for solar-powered unmanned aerial vehicles applications. Compared to the traditional topologies used, the proposed converter allows a size reduction of at least 20% of the supercapacitor by maximizing the utilization of the rated energy capacity. In addition, by proposing to use a phase-shifted carrier modulation technique, the inductors' current ripple is reduced, which enables a further reduction in the inductor size. These improvements in capability and performance of the proposed topology are experimentally validated on a 500 W PV/battery–supercapacitor integrated power system prototype.

Keywords: unmanned aerial vehicles; hybrid energy storage; multiport DC-DC converter



Citation: Fares, A.M.; Klumpner, C.; Sumner, M. A Novel Multiport DC-DC Converter for Enhancing the Design and Performance of Battery–Supercapacitor Hybrid Energy Storage Systems for Unmanned Aerial Vehicles. *Appl. Sci.* **2022**, *12*, 2767. <https://doi.org/10.3390/app12062767>

Academic Editor: Alessandro Serpi

Received: 31 January 2022

Accepted: 7 March 2022

Published: 8 March 2022

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1. Introduction

Unmanned aerial vehicles (UAVs) are nowadays experiencing unprecedented technological progress, which promoted them as a significantly cost-effective solution for many applications such as geographical survey, communications support, agriculture, and remote sensing [1–4]. Alternative propulsion based on environmentally friendly energy sources is rapidly growing to minimize carbon dioxide emissions. Accordingly, the applications of electric UAVs powered by electric power sources are expected to have more expansions, especially for the photovoltaic (PV)-powered UAVs that became widely popular due to their increased flight endurance [5–7]. Advanced applications of electric UAVs in advanced remote sensing techniques using synthetic aperture radar (SAR) as a payload [8,9] introduce more challenges for the design of UAVs power system, which is required to supply the high-power pulses consumed by these payloads whilst being restricted by the weight/volume limits imposed on UAVs' subsystems. For instance, the limited surfaces and weight available for installing the PV cells on UAVs' structure limit its power and energy harvesting capabilities; hence the power system should rely on an energy storage system (ESS) to supply the high load power peaks. This, in return, introduces more challenges in the design of the ESS, which due to the relatively large amount of energy required, is likely to require a Lithium-ion type of battery, and therefore may result in a contradictory relationship between the specific energy and the specific power that a battery struggles to fulfill. In this context, hybrid energy storage systems (HESS) based on high specific energy Li-ion batteries and high-power dense supercapacitors (SCs) have become more popular in UAVs applications [10,11]. Integration of the HESS and the PVs to the DC-bus typically utilizes separate converters that control the charge/discharge operations of the battery/SC and the maximum power point tracking of the PVs as shown in Figure 1a [10–13]. In this architecture, the range of the SC voltage, which defines the utilization level of the SC rated energy capacity, allowed by the interfaced converter playing an important role in the sizing

of SC, is analyzed in Section 2. Allowing discharge of SC to lower voltage levels increases the energy extraction from the cells but, for given power demand, results in higher currents ratings for the power semiconductors and the heavier magnetic components [14,15]. Many converter topologies can be utilized for extending the range of the voltage swing for the SC either by increasing the voltage boosting ratio [16–19] or enabling buck–boost operations [20–23] but at the cost of a significant increase in the number of power switches and/or passive components. Recently, the multiport converter (MPC) was introduced as a better option to interface and integrate the HESS and power sources to the DC-bus (as illustrated in Figure 1b) with higher system efficiency, lower cost, compact and simpler control compared to the distributed converter architectures [24,25]. In [26–32], MPCs were proposed with two bidirectional ports that suit the interfacing of the HESS to the power bus, but with increased components count and only allowing voltage boosting at the input ports, which limits the allowed voltage range for the SC. The MPCs proposed in [33,34] provided buck/boost operation for the SC port to extend its voltage range, but at the cost of increased components count.

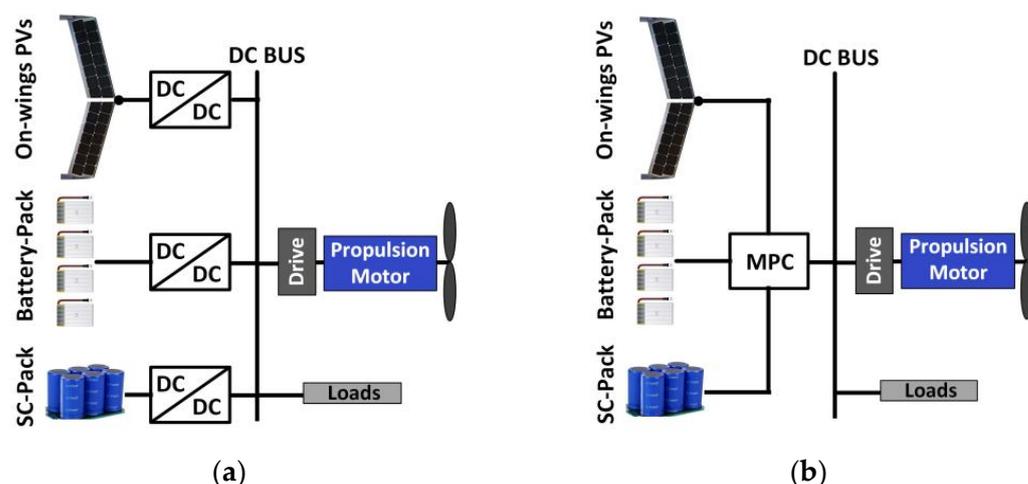


Figure 1. Block diagram for the PV-powered UAV power system: (a) with separated converters; (b) with MPC.

This paper proposes a new MPC topology with multiple input ports for PV, battery, and supercapacitor strings that are suitable for UAV applications and investigates the potential design improvements of the power system by achieving the following benefits:

- (1) Fully controlled voltage step-down and step-up capability for the battery and SC was obtained at no extra cost/component size;
- (2) A significantly wider voltage range was available for the SC to maximize the utilization of its energy capacity and hence reduce its size without added penalties in terms of components count, current stress, and the sizes of the corresponding inductors;
- (3) The ability to reduce the switching current ripple in inductors by using the interleaved phase-shifted carriers modulation technique for the different input port currents.

The paper is organized into seven sections. In Section 2, the ability of the proposed converter architecture to maximize the utilization of SCs is analyzed and compared with other topologies. In Section 3, the operating principles of the proposed converter are presented. In Section 4, the proposed phase-shifted carriers interleaved modulation technique and its effect on the ripple of the inductor current was analyzed, whilst the control of the proposed converter architecture is introduced in Section 5. A detailed experimental evaluation of the proposed converter architecture is included in Sections 6 and 7 summarizes the conclusions of this work.

2. The Proposed Converter Topology

In the HESS, the rated energy capacity (REC) of the SC is defined considering an ideal SC that can be fully discharged as:

$$EC = \frac{1}{2} C V_{\max}^2 \tag{1}$$

where C and V_{\max} are the rated capacity and the maximum voltage of the SC, respectively. However, due to the difficulty to fully discharge the SC and the extremely high current required to handle a given power share at low voltage levels, the sizing of the SC is usually performed considering the utilized energy capacity (UEC), which is defined as:

$$UEC = \frac{1}{2} C (V_{\max}^2 - V_{\min}^2) \tag{2}$$

where V_{\min} is the selected minimum voltage of the SC. Therefore, the utilization level of the REC of the SC is determined by its allowed maximum and minimum voltages, which are determined by the interfaced converter capabilities.

Figure 2a illustrates the effects of the selected maximum and minimum voltages (as relative to a constant bus voltage V_o) of the SC unit on the utilized energy capacity for the SC cells within the unit in one hand and the maximum current for the SC unit on the other hand. As can be observed, considering a simple boost converter for interfacing the SC limits its V_{\max} to be around the bus voltage (V_o), and hence the UEC can be enhanced only by minimizing V_{\min} , which in turn maximizes the current stress of the SC (I_{\max}) and occurs at the selected V_{\min} and the current rating of the converter. Point A in the graph represents common designs of V_{\max} for the SC at V_o and V_{\min} at $0.5 V_o$, which results in utilizing only 75% of the REC of the SC-cell whilst I_{\max} is twice the load current (I_o). Increasing the UEC of the SC under this topology is possible by applying more reduction in V_{\min} , which requires the converter to operate at a large duty cycle reducing its efficiency, and significantly increasing I_{\max} compared to I_o as depicted by point B in the graph at which 93.75% of the REC utilization can be achieved (25% increase in utilization compared point A) by setting V_{\min} at $0.25 V_o$ but at the cost of increasing I_{\max} to four times the load current (I_o). Reasonable efficiencies for the converter at such low levels of V_{\min} can be achieved by using other boost converter topologies such as the topologies proposed in [17,18], which can achieve a high boosting ratio at sufficient efficiency, but at the cost of the increased number of semiconductor switches and passive elements in addition to the increased current stress of the converter and SC.

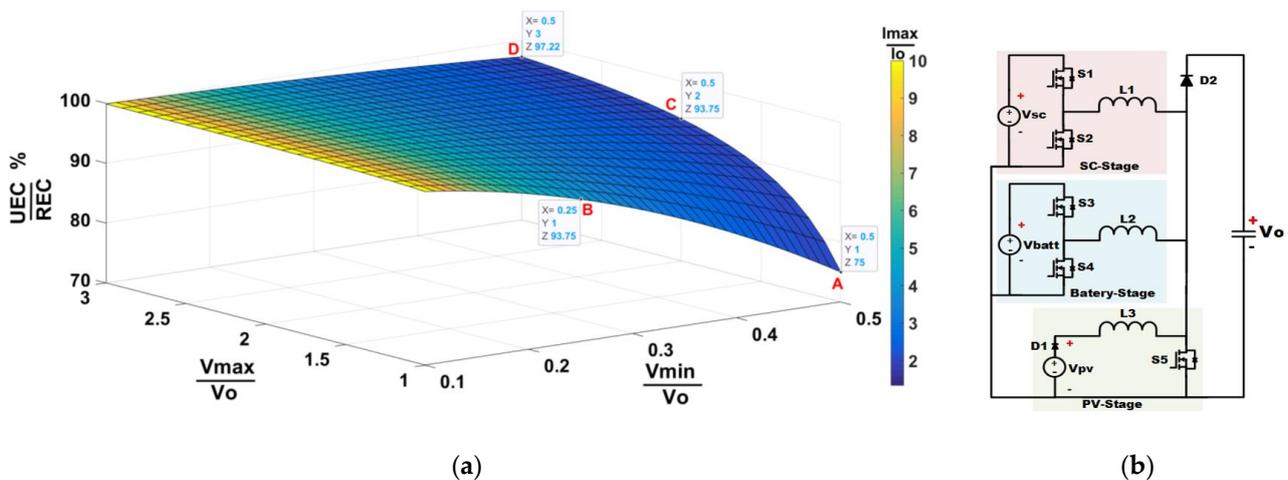


Figure 2. (a) Variation in UEC of SC-cells with different design choices for maximum and minimum voltages of SC unit as relative to the constant bus voltage; (b) schematic diagram for the proposed MPC topology.

Implementing a buck–boost converter for interfacing the SC to the DC-bus instead of the boost converter can enable a significant increase in the UEC of the SC by allowing V_{\max} to be increased above V_o and hence extend the voltage range of the SC whilst maintaining V_{\min} at a reasonable level to limit I_{\max} . Accordingly, designing V_{\max} of the SC at $2 V_o$ and V_{\min} at $0.5 V_o$ can result in utilizing 93.75% of the REC (as deprecated by point C in the graph), which is the same utilization level at point B but at a reduced I_{\max} (50% compared to point B). Increasing V_{\max} beyond $2 V_o$ increases the utilization level REC but at a less significant rate (at point D, only 3.7% increase in the utilization of the REC compared to point C that corresponds to a 50% increase in V_{\max}). Many buck–boost converter topologies can be implemented for this purpose such as those proposed in [20,23]; however, this also in the cost of the increased number of semiconductor switches and/or passive elements.

The proposed MPC showed in Figure 2b consists of a voltage step-up (boost) PV stage integrated with two voltage step-down (buck) stages to interface with the battery and the SC, the integration of these three stages in a single MPC results in a buck/boost voltage capability for the battery and the SC ports concerning the bus voltage without the need for extra components, given that the PV boost stage switch S5 can handle the overall current. The proposed converter can be utilized in a centralized architecture based on a single converter cell as presented in this paper, or it can be utilized in modular architectures that use a number of converter cells connected in a cascade similar to the concept proposed in [35], which is suitable for higher voltages applications that are out of the scope of the paper.

In order to compare the added merits of the proposed converter architecture with other topologies targeting SC design enhancements by implementing either extreme boosting ratios or buck–boost functionality, converter parameters for the different topologies are determined and presented in Table 1 considering the same bus voltage (V_o) and appropriate.

Table 1. Comparison between the SC-port of the proposed MPC and other converters considering the utilization of 93.75% of the rated energy capacity of the interfaced SC.

Parameters	Standard Boost Converter	Boost Converter in [17]	Boost Converter in [18]	Buck/Boost Converter in [20]	Buck/Boost Converter in [23]	SC-Stage in the Proposed MPC
Range of SC voltage swing required	$V_{\min} = 0.25 V_o$ $V_{\max} = V_o$	$V_{\min} = 0.09 V_o$ $V_{\max} = 0.35 V_o$	$V_{\min} = 0.08 V_o$ $V_{\max} = 0.3 V_o$	$V_{\min} = 0.5 V_o$ $V_{\max} = 2 V_o$	$V_{\min} = 0.5 V_o$ $V_{\max} = 2 V_o$	$V_{\min} = 0.5 V_o$ $V_{\max} = 2 V_o$
Duty cycle at V_{\min}	0.75	0.75	0.55	0.5	0.5	0.5
Count of semiconductor switches	2	5	6	4	3	2
Count of inductors	1	2	2	1	2	1
Count of capacitors *	0	4	4	0	2	0
Inductor max. current	$4 I_o$	$I_{L1} = 11.5 I_o$ $I_{L2} = 4 I_o$	$I_{L1} = 7.7 I_o$ $I_{L2} = 4.4 I_o$	$2 I_o$	$I_{L1} = 3 I_o$ $I_{L2} = I_o$	$2 I_o$
Inductor's inductance	$L_1 \geq \frac{0.25V_o}{f_s \Delta I_{L1}}$	$L_1 \geq \frac{0.073V_o}{f_s \Delta I_{L1}}$ $L_2 \geq \frac{0.8V_o}{f_s \Delta I_{L2}}$	$L_1 \geq \frac{0.04V_o}{f_s \Delta I_{L1}}$ $L_2 \geq \frac{0.14V_o}{f_s \Delta I_{L2}}$	$L_1 \geq \frac{0.5V_o}{f_s \Delta I_{L1}}$	$L_1 \geq \frac{0.4V_o}{f_s \Delta I_{L1}}$ $L_2 \geq \frac{0.4V_o}{f_s \Delta I_{L2}}$	$L_1^{**} \geq \frac{0.37V_o}{f_s \Delta I_{L1}}$
Max. voltage stress on semiconductor switches	V_o	$0.3 V_o$	$Q_{1,5} = 0.2 V_o$ $Q_2 = 0.4 V_o$ $Q_{3,4,6} = 0.6 V_o$	$2 V_o$	$2.5 V_o$	$2 V_o$

Table 1. Cont.

Parameters	Standard Boost Converter	Boost Converter in [17]	Boost Converter in [18]	Buck/Boost Converter in [20]	Buck/Boost Converter in [23]	SC-Stage in the Proposed MPC
Max. current stress on semiconductor switches	$Q_{1,2} \geq 4 I_o$	$Q_1 \geq 13 I_o$ $Q_{2,3,5} \geq 4 I_o$ $Q_4 \geq 5 I_o$	$Q_1 \geq 12 I_o$ $Q_{2,5} \geq 6 I_o$ $Q_{3,4,6} \geq 2 I_o$	$Q_{1,2} \geq 2 I_o$	$Q_1 \geq 4 I_o$ $Q_{2,3} \geq 2 I_o$	$Q_{1,2} \geq 2 I_o$ $Q_{1,2} \geq I_o + I_{pv} + I_{batt}$

* Excluding filtering capacitors at input/output. ** Based on the implementation of the proposed phase-shifted carriers modulation technique described in Section 4 voltage range for the SC (V_{max} and V_{min}) depending on each topology to enable $\approx 93.75\%$ utilization of REC of the SC (targeting the design at point C that enables 25% more utilization of the REC compared to traditional designs at point A). For fair comparisons between the single input and the multi-input converters considering devices count, sizing of the passive components, and current rating, only the SC-stage in the multi-input converter is considered in this comparison. According to Table 1, the proposed converter architecture through its SC-stage enabled the achievement of the targeted 25% enhancement for the utilization of SC, and hence size reduction by the same percentage without added penalty in the converter parameters in terms of component size, count, or current stress compared to other topologies presented. The switch S5 and the diode D2 of the proposed converter have higher current stress as it should handle the PV current in addition to both battery and SC currents during some modes of operations, but it is still lower current stress compared to the other topologies presented. In addition to this enhancement for the interfaced SC, the proposed MPC can also enable energy manipulation between battery and SC, which may be required in some HESS applications that require pre-charge/pre-discharge of SC before a scheduled peak power loading/generation.

3. Operation of the Proposed Converter

The proposed converter shown in Figure 2b consists of five reverse conducting power semiconductor switches, three inductors, and a single diode (D2). The diode (D1) is a blocking diode that is normally embedded with the PV panels to prevent reverse conduction through the PV during the unavailability of the PV power and is not part of the proposed converter. V_{PV} is the voltage of the PV array connected to the unidirectional input port of the converter, V_{batt} is the voltage of the battery connected to one of the bidirectional input ports, and V_{SC} is the voltage of the SC connected to the other bidirectional input port.

The possible operation modes of the proposed MPC as illustrated in Figure 3 are:

- Single input–double output (SIDO) mode (Figure 3a): where the PV supplies the required load power whilst any excess is charging the battery;
- Single input–triple output (SITO) mode (Figure 3b): where a significant amount of power is produced by the PV that can supply the load power, and due to limitations of maximum charging power of the battery, all excess is stored in the SC;
- Double input–single output mode-I (DISO-I) (Figure 3c): where the PV is unable to supply the load power, and any deficit is provided by the battery, where the load is not excessive (medium power peaks);
- Triple input–single output (TISO) mode (Figure 3d): where the PV, the battery, and the SC are supplying the load power during high power peaks, which exceed the available PV power and the battery discharge power capability;
- Single input–single output (SISO) mode (Figure 3e): where the battery provides power for supplying the load during the unavailability of the PV power;
- Double input–single output mode-II (DISO-II) (Figure 3f): where both the battery and the SC provide power for supplying the load during significant load power peaks that happen during the unavailability of PV power.

In order to simplify the analysis of the converter, continuous conduction mode (CCM) is considered for all modes of operations, and the power MOSFETs and diodes are assumed to be ideal.

3.1. Operation Principle during the SIDO Mode

The typical waveforms and current paths of the converter under SIDO mode are shown in Figures 4 and 5, assuming the SC is completely charged and its voltage is higher than V_O . The steps of operation during this mode can be described as follow:

- Step I: PV switch S5 is turned ON whilst the battery stage switch S3 is still in conduction from the previous cycle. The voltage across L3 is V_{PV} , and the voltage across L2 is V_{batt} , where the diode D2 is OFF;
- Step II: S5 is still in conduction, and D2 is still OFF when S3 is switched OFF. The voltage across the L2 becomes zero (shorted to ground via S4 and S5) whilst the voltage across L3 is still V_{PV} ;
- Step III: S5 is switched OFF, and D2 starts conduction whilst S3 is still OFF. Therefore, the voltage across the L2 is $(-V_O)$, and the voltage across L3 is $(V_{PV}-V_O)$;
- Step IV: S5 is still OFF, and D2 is still ON when S3 is switched ON. Therefore, the voltage across the L2 is $(V_{batt}-V_O)$, and the voltage across L3 is $(V_{PV}-V_O)$.

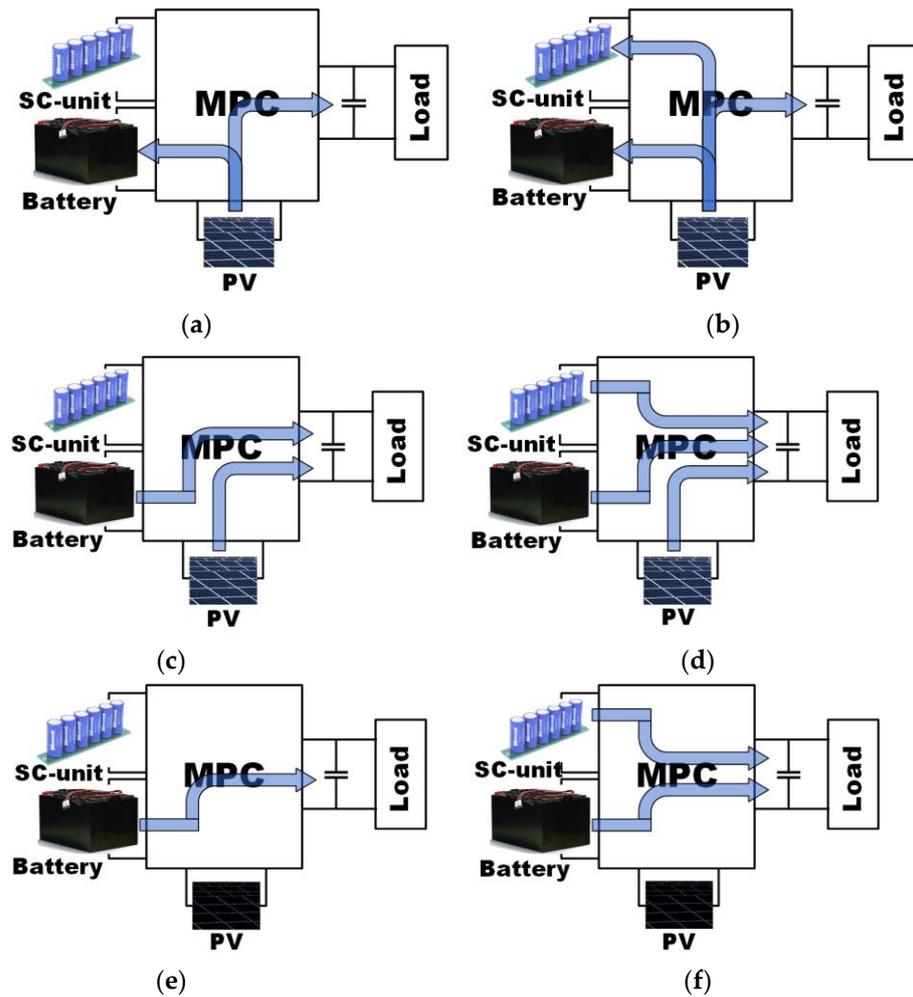


Figure 3. Possible operation modes of the MPC: (a) SIDO mode; (b) SITO mode; (c) DISO-I mode; (d) TISO mode; (e) SISO mode and (f) DISO-II mode.

By applying the voltage balance principle on the inductors L3, the following equation can be obtained:

$$d_5 V_{PV} + (1 - d_5)(V_{PV} - V_O) = 0 \tag{3}$$

Therefore

$$V_{PV} = (1 - d_5)V_O \tag{4}$$

where d_5 is the duty cycle of the PV stage switch S5, and for a given bus voltage V_O is dependent only on PV voltage to enable extracting maximum power from the PV.

Similarly, by applying the voltage balance principle on the inductors L2, the following equation can be obtained:

$$d_3 V_{batt} - (1 - d_5) V_O = 0 \tag{5}$$

Therefore

$$V_O = \frac{d_3}{(1 - d_5)} V_{batt} \tag{6}$$

where d_3 is the duty cycle of the switch S3, which, for a particular d_5 and bus voltage, is dependent only on the battery voltage.

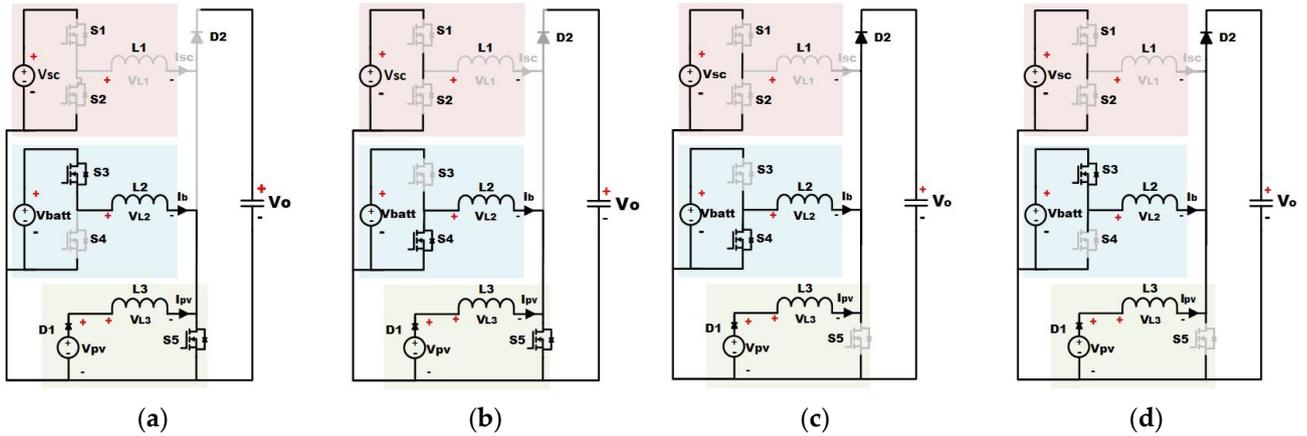


Figure 4. Illustration of the current paths (black lines and gray lines indicate the activated and deactivated paths, respectively) during the different steps of operation of SITO mode: (a) Step I, (b) Step II, (c) Step III, and (d) Step IV.

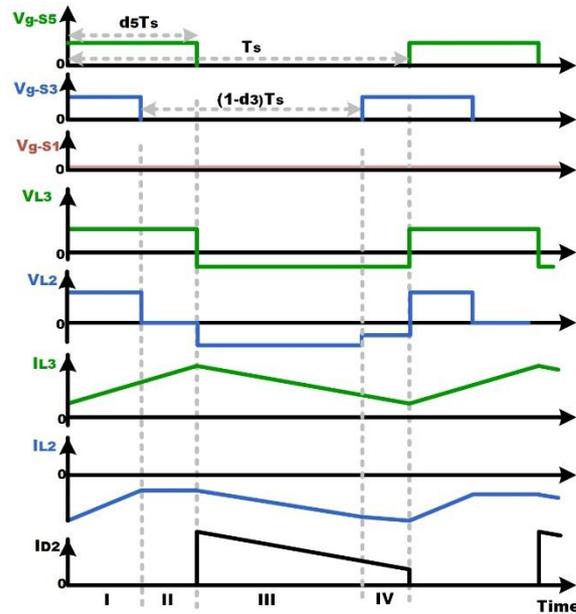


Figure 5. Relevant voltage and current waveforms during SITO mode.

3.2. Operation Principle during the SITO Mode

The operation of the converter under the SITO mode is similar to the SITO mode with SC in operation, as can be observed from the typical waveforms and current paths shown in Figures 6 and 7.

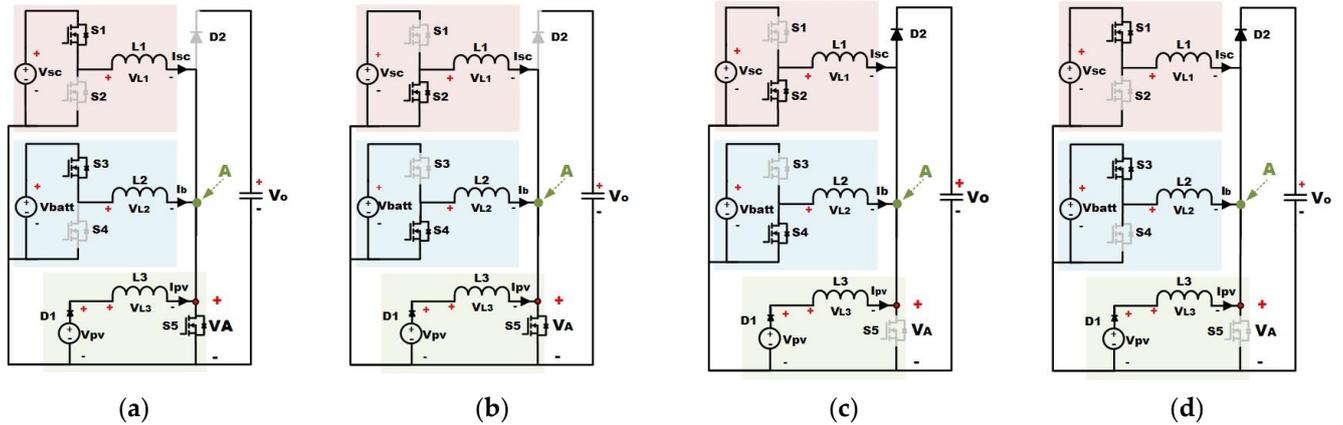


Figure 6. Illustration of the current paths (black lines and gray lines indicate the activated and deactivated paths, respectively) during the different stages of operation of SITO mode: (a) Step I, (b) Step II, (c) Step III, and (d) Step IV.

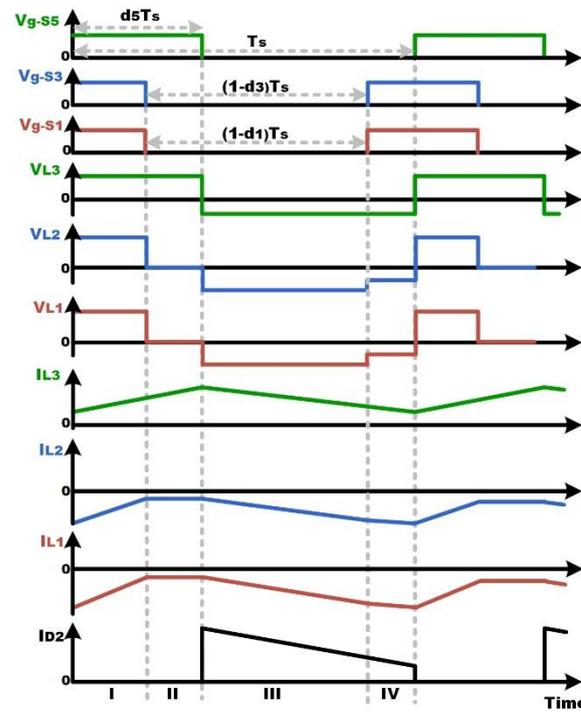


Figure 7. Relevant voltage and current waveforms during SITO mode.

During this mode, the voltage of the SC changes significantly from $V_{sc_{min}}$ up to $V_{sc_{max}}$. Therefore, to prevent the undesired conduction of the switch S1 through its body diode to maintain the controllability of the charging current, the average voltage at point A (shown in Figure 6) should always be less than V_{sc} . This average voltage (V_A) under this mode can be defined as:

$$V_A = (1 - d_5)V_O \tag{7}$$

Accordingly, to ensure the controllability of the SC current under the large variation in its voltages during charge/discharge operations, the minimum duty cycle of the switch S5 should satisfy:

$$d_{5min} \geq 1 - \frac{V_{sc_{min}}}{V_O} \tag{8}$$

where $V_{sc_{min}}$ is the minimum voltage of the SC. It can be observed that the maximum power point tracking (MPPT) function using S5 can be overridden when the required duty

cycle of S5 (d_5) is less than d_{5min} . In this particular case, the switch S5 is forced to operate with a duty cycle of d_{5min} , causing the PV to work away from the maximum power point, which can be accepted for a short time until the SC voltage is increased to be higher than V_A . The output voltage during this mode can be calculated based on (6).

3.3. Operation Principle during the DISO-I and TISO Modes

The operation of the converter during the DISO-I mode is similar to the operation during the SIDO mode, with opposite polarity for the current of L2. Moreover, the operation in TISO mode is similar to the operation during SITO, with opposite polarity for the currents of L1 and L2.

3.4. Operation Principle of the SISO Modes

During the SISO mode, as PV power is unavailable and consequently the switch S5 should be turned OFF, the battery supplies the load power through the battery stage, which represents a conventional buck converter, and by assuming that the SC voltage is at ($V_{scmax} > V_O$), the output voltage can be defined as:

$$V_O = d_3 V_{batt} \tag{9}$$

Accordingly, the maximum output voltage during this mode is limited to the battery voltage, compared to the previous modes of operation at which the maximum output voltage can be higher than the battery voltage. This requires the battery voltage to be designed at a voltage greater than the required output voltage to maintain the regulation of the output voltage. However, by operating the switch S5 during this mode with a duty cycle that is controlled by the output voltage control loop, the buck–boost operation of the proposed converter achieved in other modes of operation can be sustained, and regulation of the output voltage can be achieved with a battery voltage either higher or lower than the output voltage. Accordingly, to prevent the undesired conduction of the switch S3 through its body diode to maintain the controllability of battery charging current, the minimum duty cycle of the switch S5 should satisfy:

$$d_{5min} \geq 1 - \frac{V_{battmin}}{V_O} \tag{10}$$

where $V_{battmin}$ is the minimum voltage of the battery at the lowest state of charge (SoC).

Typical waveforms and current paths of the converter under this mode are shown in Figures 8 and 9. The output voltage during this mode can be driven by applying voltage balance on L2, same as in (5) and (6).

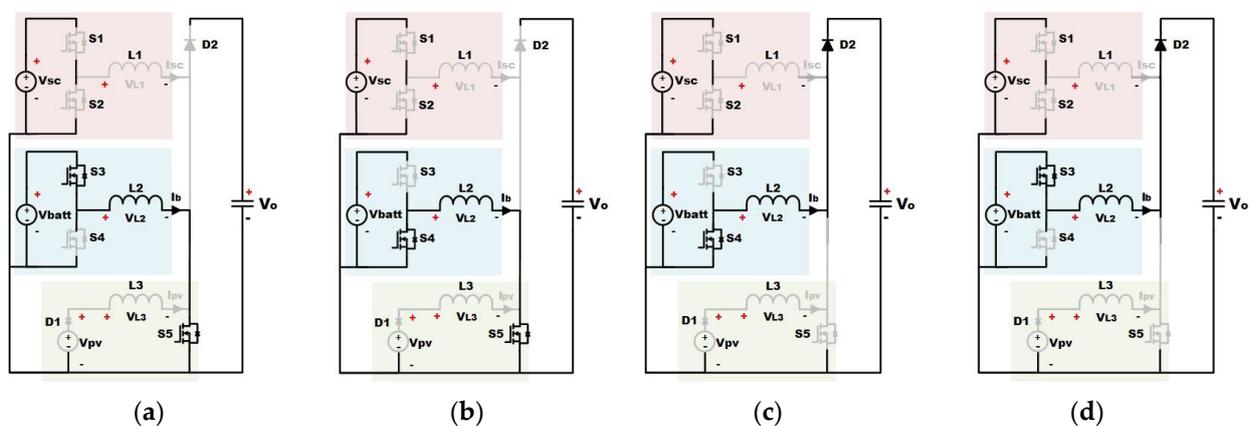


Figure 8. Illustration of the current paths (black lines and gray lines indicate the activated and deactivated paths, respectively) during the different stages of operation of SISO mode: (a) Step I, (b) Step II, (c) Step III, and (d) Step IV.

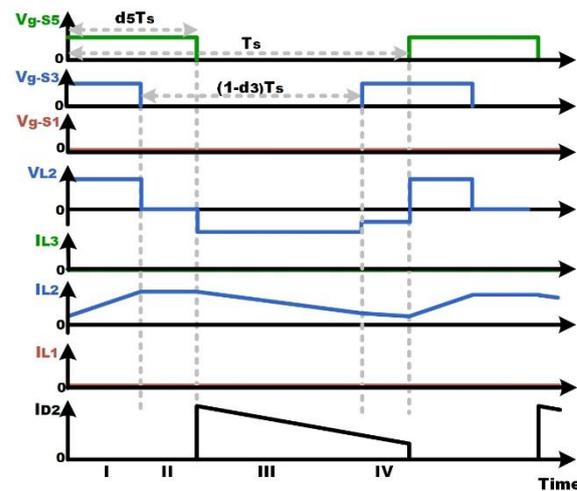


Figure 9. Relevant voltage and current waveforms during SISO mode.

3.5. Operation Principle during the DISO-II Modes

During this mode, as the SC discharges and its voltage decreases significantly, the duty cycle of the switch S5 should satisfy (8). The output voltage during this mode can be driven by applying voltage balance on L2, same as in (5) and (6).

4. The Phase-Shifted Carriers Modulation

In order to define the size of the battery/SC stages inductors (L1, L2), the ripple currents of these inductors at the boundaries of the operating voltage range for both battery and SC need to be considered. By considering the converter output voltage of V_o , which is defined by the application, the operating voltage range of the battery can be considered as wide as from $0.75 V_o$ at the lowest SoC up to $1.5 V_o$ at the highest SoC. Accordingly, the operating voltage range of the PV array considering these conditions can be selected to be from $0.5 V_o$ up to $0.75 V_o$. Accordingly, four operation boundary points of the battery stage inductor (L2) can be obtained, A, B, C, and D. At points A and B, the PV voltage is at its minimum; however, at point A the battery is at the highest SoC and at point B the battery is at lowest SoC. On the other hand, at points C and D, the PV voltage is at its maximum; however, at point C, the battery is at the highest SoC, and at point D, the battery is at the lowest SoC. The corresponding duty cycles for the battery and PV switches and the current ripple (ΔI) of the inductor L2 at each of these boundary points at a switching frequency (f_s) are listed in Table 2, and the relevant waveforms are shown in Figure 10a.

Table 2. The peak-to-peak current ripple of the battery stage inductor (L2) at the boundaries of the operating range with/without phase-shifted carrier modulation technique.

V_{PV} \ V_{batt}		$1.5 V_o$		$0.75 V_o$	
		A		B	
$0.5 V_o$	$d3 \approx 0.33$ $d5 = 0.5$	$\Delta I _{\theta=0} = \frac{0.5V_o}{L_2 f_s}$	A	$d3 \approx 0.67$ $d5 = 0.5$	B
		$\Delta I _{\theta=\frac{5\pi}{4}} = \frac{0.165V_o}{L_2 f_s}$			
$0.75 V_o$	$d3 = 0.5$ $d5 = 0.25$	$\Delta I _{\theta=0} = \frac{0.5V_o}{L_2 f_s}$	C	$d3 = 1$ $d5 = 0.25$	D
		$\Delta I _{\theta=\frac{3\pi}{4}} = \frac{0.25V_o}{L_2 f_s}$			

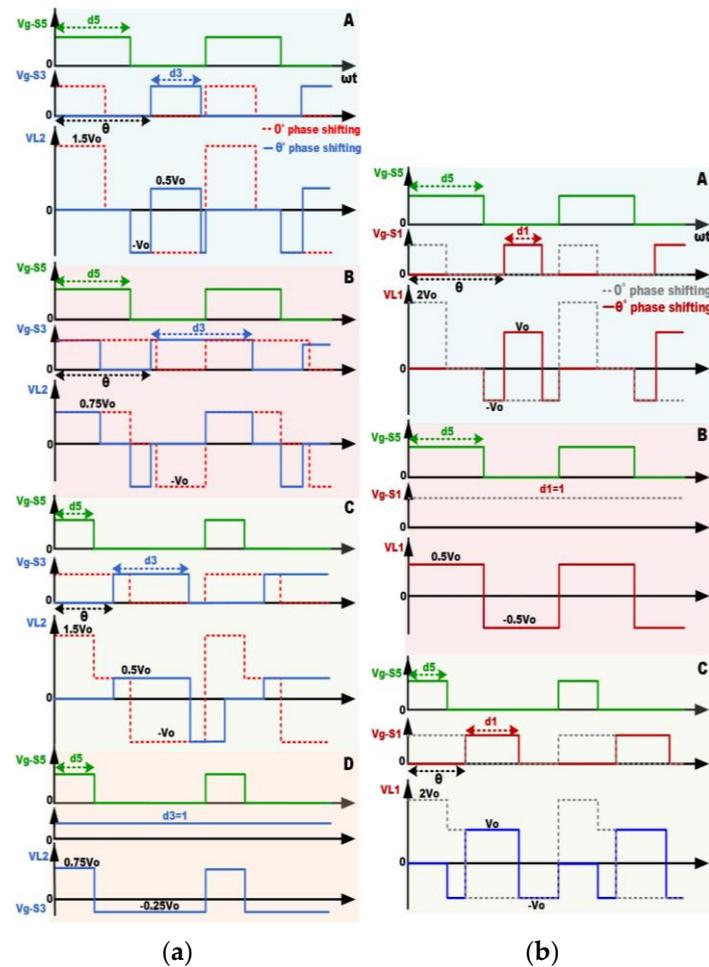


Figure 10. (a) battery stage gating and inductor voltage waveforms at the operation boundaries (A–D); (b) SC stage gating and inductor voltage waveforms at the operation boundaries (A–C).

In order to minimize the inductor L2 current ripple, a phase-shifted carrier modulation (PSCM) technique was employed by adopting a phase-shift angle of (θ°) between the PWM carriers of the switches S5 and S3 to minimize the voltage across the inductor and consequently its current ripple. The angle should be varying based on the value of the duty cycles to avoid the deadlock situation that would prevent power flow to/from the battery, which occurs when $d_3 = (1 - d_5)$ and $\theta^\circ = 360 d_5$. Therefore, to achieve the minimum current ripple for L2 and avoid deadlock situations, the phase shift angle should satisfy:

$$\theta = (2d_5 + 0.25)\pi \tag{11}$$

From the estimated inductor current ripples under different conditions presented in Table 2, a minimum of 50% reduction in the inductor L2 current ripple was achieved by implementing the PSCM technique.

Similarly, the SC stage inductor (L1) current ripple can be reduced by implementing the PSCM technique. A minimum of 25% can be achieved as presented in Table 3, which represents the corresponding duty cycles for the SC and PV switches as well as the inductor L1 current ripple at each point, and the waveforms are shown in Figure 10b. It should be noted that when the voltage of the PV at MPP is $0.75 V_o$, and V_{sc} is $0.5 V_o$, the converter is forced to work at point B, away from MPP until SC charges and V_{sc} reaches $0.75 V_o$, which may take a few tens of seconds, hence not affecting the PV energy harvesting.

Table 3. The peak-to-peak current ripple of the SC stage inductor (L1) at the boundaries of the operating range with/without phase-shifted carrier modulation technique.

Vpv	VSC	2 Vo	0.5 Vo
0.5 Vo	d1 ≈ 0.25 d5 = 0.5	$\Delta I _{\theta=0} = \frac{0.5V_O}{L_1 f_s}$ $\Delta I _{\theta=\frac{5\pi}{4}} = \frac{0.25V_O}{L_1 f_s}$	$\Delta I = \frac{0.25V_O}{L_1 f_s}$
	A		
0.75 Vo	d1 = 0.375 d5 = 0.25	$\Delta I _{\theta=0} = \frac{0.5V_O}{L_1 f_s}$ $\Delta I _{\theta=\frac{3\pi}{4}} = \frac{0.375V_O}{L_1 f_s}$	B
	C		

5. Control of the Proposed Converter

The basic idea of the control strategy for HESS is that the SC supports the high frequency/high amplitude components in the load power, which is usually estimated by a load voltage controller, and the battery supports the low-frequency power/high energy component. Therefore, a low pass filter (LPF) is usually employed to separate the slow varying average power component, which is used to derive the reference current to the battery current control loop whilst the highly dynamic power component is used to produce the reference value for the SC current control loop [36,37]. In order to further reduce the stress of the battery, an asymmetric charge/discharge current limiter was considered, as in [38]. The resulting mismatch in the battery power is added to the error component of the battery current to produce the SC reference current, which facilitates a faster and more accurate regulation of the output load voltage. The control strategy of the proposed converter prototype follows the above philosophy to accommodate the limited current capability of the high specific energy batteries used in HESS, and the resulting block diagram is shown in Figure 11, where the symbols for the state variables are indicated in the circuit diagram shown in Figure 6. First, the converter output voltage (Vo) is compared with the reference voltage (Vo_R), and the error is inputted to a PI controller. This controller estimates the current that is consumed by the load and supplied by the converter and detects any imbalance that causes deviation of load voltage from the reference. This is then used to calculate the total power (Pt) that has to be supplied by both the battery and SC whilst taking into account the available power extracted from the PV. This total power required from the energy storage is then separated into low and high-frequency components by an LPF. The reference battery power (Pb-R) is obtained by applying an asymmetric limiter to the low-frequency power component to control the charge/discharge power of the battery based on specified limits to preserve its lifetime. Given that the battery power is defined by the battery stage inductor current (Ib) multiplied by the average voltage seen at point A (shown in Figure 6), which is estimated using (7), the reference value for the battery stage inductor current Ib-R that is required to deliver this battery power is determined and passed to the battery current control loop that generates the PWM for the switches S3 and S4 accordingly. On the other hand, the SC’s reference power (PSC-R) is obtained by subtracting the reference battery power Pb-R (subject to specific battery limitations) from the total energy storage power requirement (Pt). Based on the required power from the SC and the average voltage seen at point A, the reference value for the SC stage inductor current (ISC-R) is determined and given to the SC’s current control loop, which generates the PWM for the switches S1 and S2 accordingly. The switch S5 has dual functionality: (i) to control the operating point of the PV to follow the MPPT and (ii) to ensure the controllability of the SC and battery stages’ inductors (L1, L2) is maintained, which depends on the voltage level of the SC and the battery, as described in Section 3. As the latter is a system function, therefore it has higher priority. Accordingly, the duty cycle of S5 is selected as the maximum value (that corresponds to a minimum average voltage VA)

calculated based on these two functions. To clarify, considering the condition where the PV power is unavailable, the voltage of the battery (V_{batt}) is at 75% of the output voltage (V_o), and the voltage of the SC (V_{sc}) is higher than the battery voltage. Under these conditions, the calculated value for the duty cycle of the switch S5 based on MPPT function should be 0% (as there is no power available from the PV), whilst the calculated value based on the battery stage operation (based on 10) should be 25%, which is higher than the calculated value based on the SC stage according to (8) as the battery has higher voltage as mentioned above. Accordingly, the value of the duty cycle for the switch S5 should be defined by the maximum of those values, and hence S5 will operate at a 25% duty cycle. However, if for the same battery voltage, the SC voltage is 50% of the output voltage (lower than the battery voltage), then the duty cycle calculated based on the SC stage according to (8) is 50%, which is the value calculated based on battery stage according to (10), which is 25% in this case. Therefore, the switch S5 should operate by the maximum value of those two values, which is 50%.

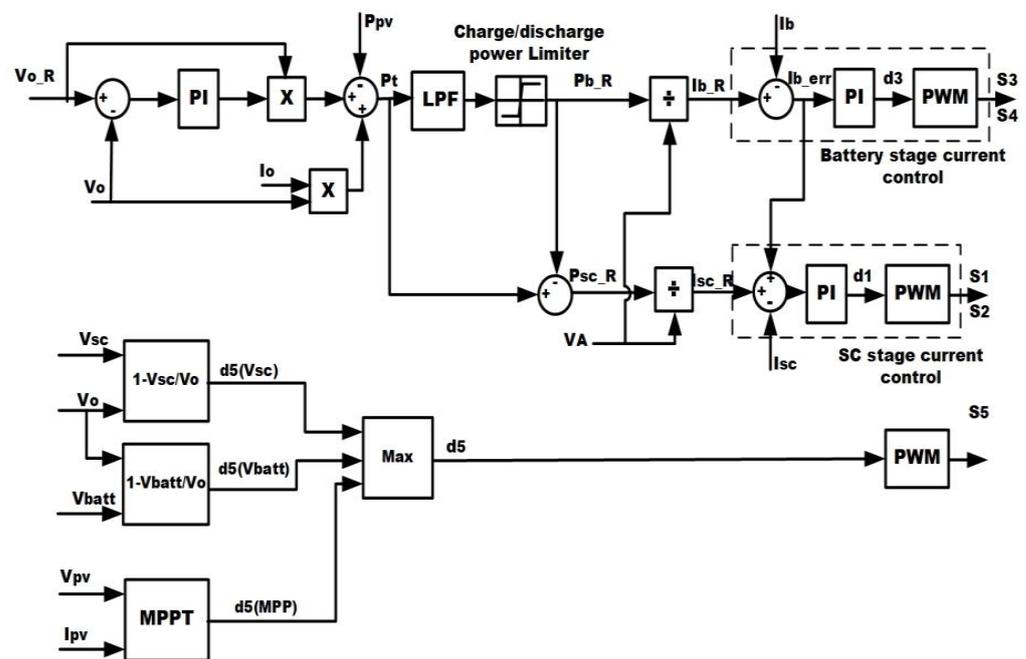


Figure 11. The control scheme of the proposed converter.

6. Experimental Results

In order to validate the proposed converter, an experimental integrated power system setup (500 W/30 V) was implemented. The system consists of the proposed converter system that interconnects a Li-ion battery, an SC, a programmable power supply that acts as a PV emulator, and a programmable electronic load that enables the generation of customized load transients. The control scheme is implemented on a control platform that consists of TMS320C6713 DSP performing the calculations and a ProASIC[®]3 FPGA custom board used for the A/D conversion of voltage and current measurements and PWM signal generation. The DSP sampling and the PWM carrier switching frequency are both set to 10 kHz. The complete setup is shown in Figure 12, with the corresponding specifications listed in Table 4.

The response of the converter system is evaluated under step load power transient experiments. The first test evaluates the response of the system following a large constant power peak load, as shown in Figure 13. Initially, the load consumes a constant power of 160 W, which is slightly more than the PV available power which remains constant for the duration of this experiment. As the required power from the energy storage is small, this is provided by the battery, which discharges with a low current (1 A) that is assumed to be below its current limit, and consequently, the SC current is zero, as can be seen in

Figure 13a. At ($t = 38$ s), a large step change in the load power was applied ($p = 400$ W), causing the required power delivered by the energy storage to be significantly increased. As a result, the discharging current of the battery, which is the main source of stored energy, raises, reaching its limit of 5 A. The control senses this and forces the SC to contribute and support the load power peak by increasing its current to 11 A. This causes the discharge of most of SC stored energy which is seen in the SC voltage drop from 50 V to 22 V at the end of the peak power load ($t = 65$ s), as can be seen in Figure 13b. This test confirms the capability of the converter to maintain the output voltage(V_o) regulated at the desired value (30 V) as well as active control of the power share between the battery and the SC under the large disturbance introduced by the load power peaks. It also validates the buck–boost capability of the proposed converter at the SC port, which allowed the voltage of the SC to be changed from the higher value (50 V) that is above the V_o to the lower value (22 V) and below the V_o (which increase the utilization of SC energy capacity as discussed in Section 2) whilst maintaining the full controllability of the converter.

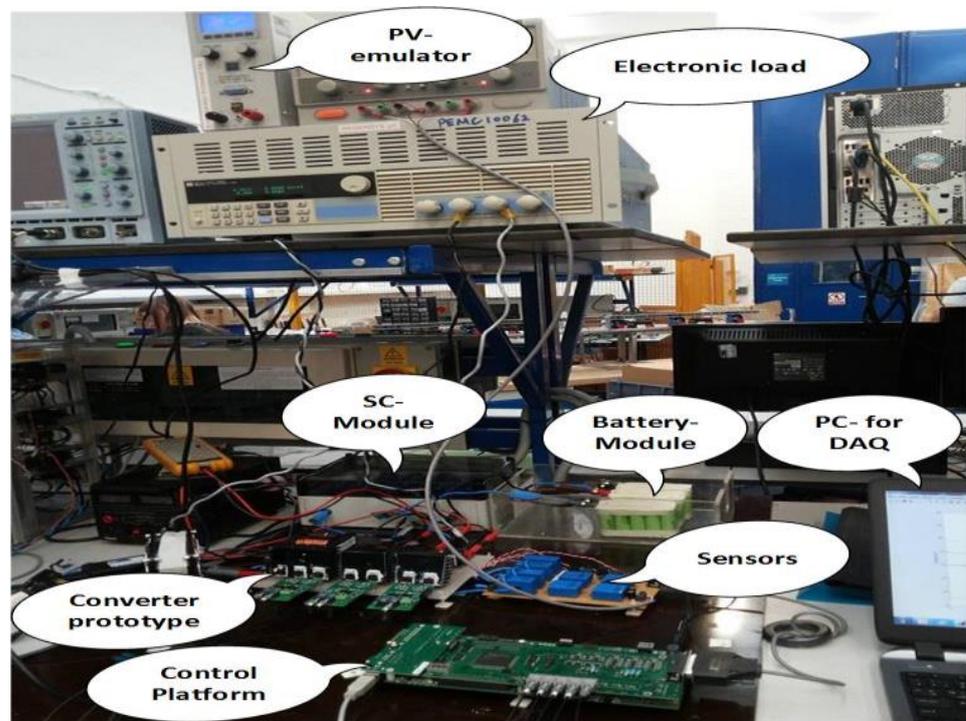
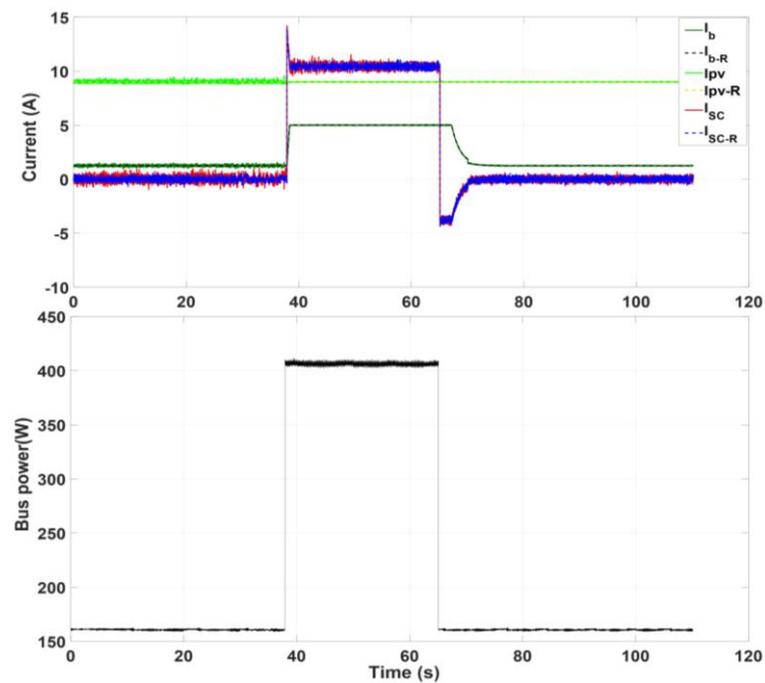


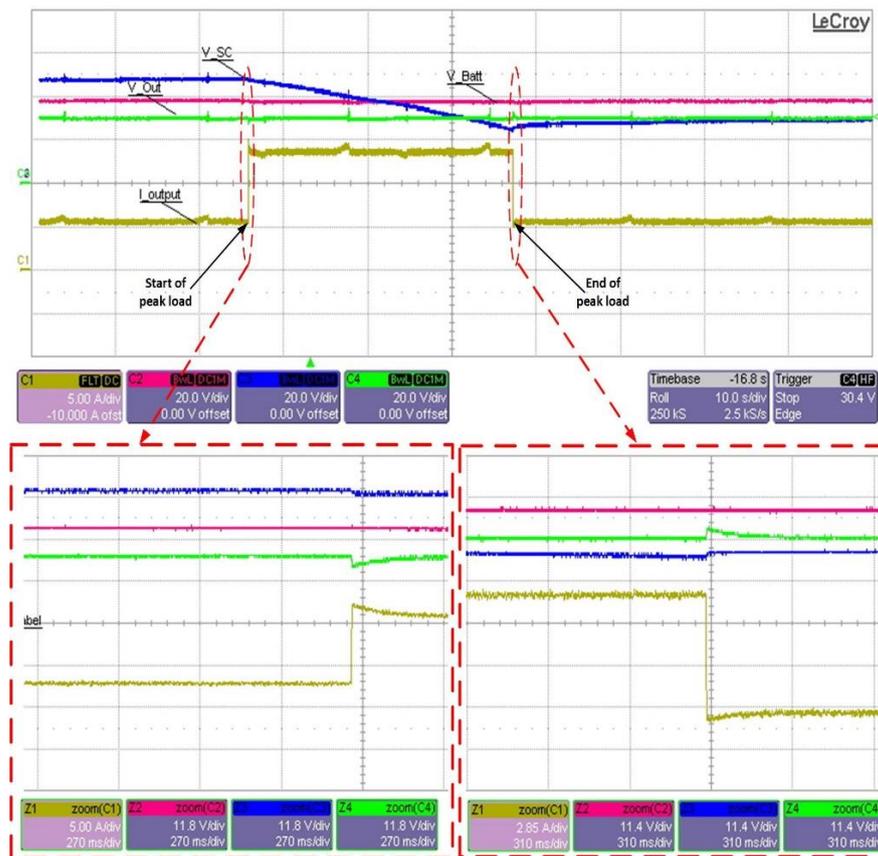
Figure 12. Experimental setup for validating the proposed converter.

Table 4. Specifications of the used components in the experimental setup.

Type/Name	Rating/Specifications
Battery module	42 V / 6 Ah based on Panasonic NCR18650B cell with $V_{\max} = 42$ V and $V_{\min} = 25$ V
SC-module	8 F / 60 V based on AVX SCCW45B107 cell with $V_{\max} = 60$ V and $V_{\min} = 15$ V
PV module emulator	$V_{pV_{MPP}} = (15 - 22.5)$ V, $I_{pV_{MPP}} = (6 - 9)$ A
SC stage inductor (L1)	120 μ H
Battery stage inductor (L2)	240 μ H
PV module inductor (L3)	120 μ H
DC-link capacitor (C_O)	2200 μ F
Switching frequency (F_s)	10 kHz



(a)

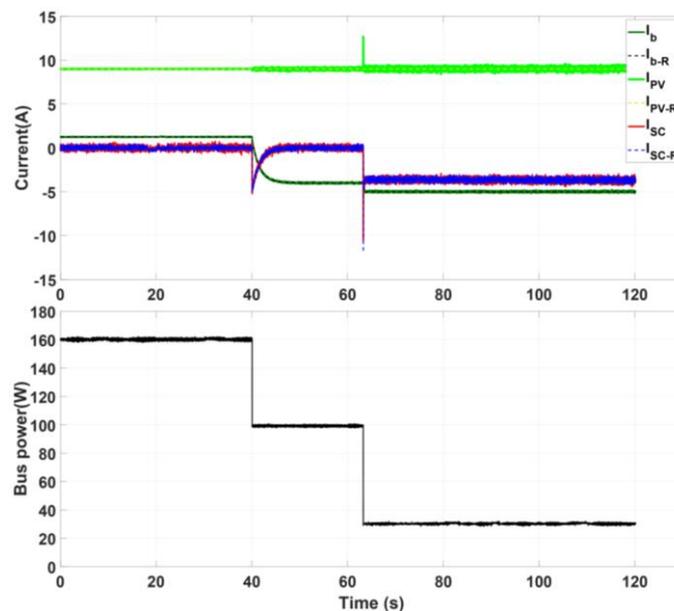


(b)

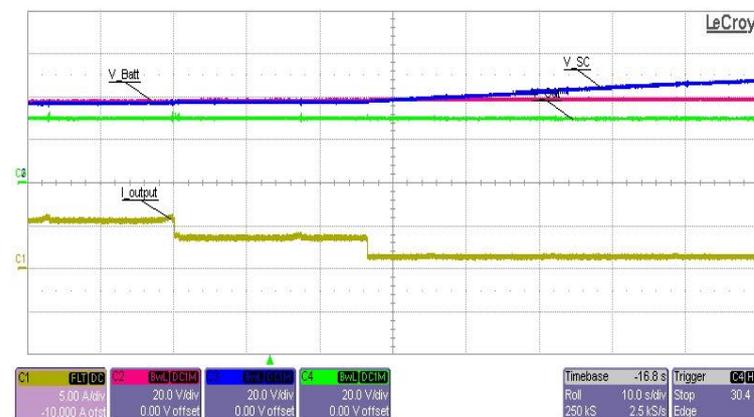
Figure 13. Experimental results during peak power loading: (a) Battery, SC, and PV currents and bus power; (b) Battery, SC, and output voltages and output current.

The second test evaluates the performance of the proposed converter during the charging mode under imposed changes in the load. The changing scenarios are shown

in Figure 14a. Initially, the load is consuming a constant power of 160 W, larger than the available PV power, and therefore, the battery discharges with a current of (≈ 1 A). When the load power reduces to 100 W ($t = 40$ s), there is extra power available from the PV, and this causes the battery to charge with 4 A. As this current is below the assumed battery current limit of 5 A, the SC contributes with charging current only during short-term transients as expected from the low/high-frequency filter effects on the reference ESS power. The SC current then reduces to zero after battery power compensates for the excess PV power. When a significant reduction in the load power occurs ($t = 63$ s), the battery current reaches its specified limit, and hence the SC has to absorb current during the transient period as well as absorb the excess power remaining after PV/load/battery power exchanges. This results in a noticeable rise of the SC voltage, as seen in Figure 14b. If there is excess power when the SC reaches its maximum voltage (not shown here), the control of the PV should change and move away from MPPT by capturing only the power that is consumed by the load and possibly to be absorbed by the battery. The test confirms the capability of the proposed converter to maintain the output voltage V_o regulated and perform active power share control under different variations in the loads during the charging mode of the ESS.



(a)



(b)

Figure 14. Experimental results during different loading scenarios with (a) battery, SC, and output voltages and output current; (b) Battery, SC and PV currents, and bus power.

The last test evaluates the response of the converter system under the disturbances of the PV power, as shown in Figure 15. Initially, the load draws a constant power of 70 W, and the PV is supplying enough power to cover the load power and to charge the battery with 6 A. At $t = 30$ s, the PV source becomes unavailable; this is sensed by the control that orders the SC unit to act quickly and bridge the short-term power gap and orders the battery to start to discharge to supply the load until the PV power becomes available again at $t = 85$ s. As can be observed, due to the low power consumed by the load, the battery current remains below its limit (set at 10 A for this test); therefore, the SC supplies only the short-term component of the load (transient period). The test results confirm the capability of the proposed converter to maintain the regulation of the output voltage V_o under the disturbances caused by the presence/absence of the primary power source (PV) relaying on the active power share control of the ESS.

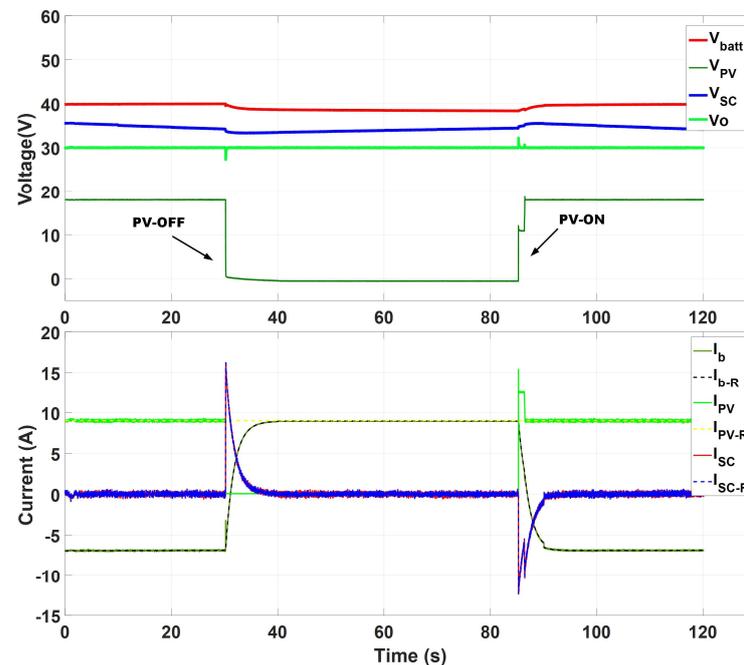


Figure 15. Experimental results during sudden absence/presence of PV power.

A general observation that applies to all three transients is that the controller can maintain a constant output voltage with minimum disturbance (maximum of 8% of the set value).

7. Conclusions

A novel multiport converter topology for integrating a photovoltaic power source with battery–supercapacitor hybrid energy storage for PV-powered UAV applications was proposed in this paper. The proposed converter provides two ports with voltage step-down/step-up capability for interfacing the battery and supercapacitor unit and a voltage step-up port for interfacing with the PV source. The buck–boost capability of the SC port enabled a wider operating voltage range for the SC, which increases the utilization of supercapacitor energy capacity that enabled a 20% reduction in the size of the supercapacitor unit compared to the conventional approaches that utilize (voltage step-up only) topologies to interface supercapacitors. A phase-shifted carrier modulation technique was proposed, which allowed further reduction in the sizes of the inductors for the battery and supercapacitor stages. The performance of the converter was experimentally evaluated on an integrated power system prototype, which was subject to power pulses/step transients. The results showed an excellent transient response of the proposed converter and its control.

Author Contributions: Conceptualization, A.M.F.; methodology, A.M.F. and C.K.; software, A.M.F.; validation, A.M.F.; formal analysis, A.M.F. and C.K.; investigation, A.M.F. and C.K.; data curation, A.M.F.; writing—original draft preparation, A.M.F.; writing—review and editing, A.M.F., C.K. and M.S.; visualization, A.M.F.; supervision, C.K. and M.S.; funding acquisition, A.M.F. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Ministry of Higher Education, Egypt, through a Ph.D. scholarship funded by the Cultural Affairs and Missions Sector.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: The authors also gratefully acknowledge support from the ESTEEM project, which received funding from the Clean Sky 2 Joint Undertaking under the European Union’s Horizon 2020 research and innovation program under grant agreement No 755485.

Conflicts of Interest: The authors declare no conflict of interest.

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