New Asymmetric Cascaded Multi-level Converter with Reduced Components

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***Abstract*—Multi-level converters have been used in several industrial applications. The following work seeks to present a novel power inverter structure featuring a low amount of devices for a multi-level converter with an asymmetric cascaded connection. The suggested architecture consists of a modified T-type structure and a half-bridge inverter that is back-to-back connected. The proposed circuit includes five dc voltage sources and nine semiconductor switches that generate 23 levels. To show the superiority of the proposed structure, a detailed comparison is made with other comparable multi-level converter structures. Simulations in MATLAB/Simulink are shown to validate the behaviour of the proposal.**

***Index Terms*—symmetric and asymmetric, optimal structure,cascaded multi-level converter.**

I. Introduction

Multi-level inverters (MLI) are the main selected power conversion devices in industrial applications. These applications mostly comprise motor drives for all voltage and power ratings. Multi-level inverters are also finding their applications in grid-connected systems, uninterruptible power supply (UPS), electric vehicles and FACTS devices. All these applications are possible due to the ability of the MLI to provide a better output voltage with a more sinusoidal shaped waveform, improved efficiency due to lower switching frequency operation of switches, lower blocking voltage requirement with reduced dv/dt and improved electromagnetic compatibility. Another positive impact of MLI is the reduction of the filter size and cost due to reduced harmonics at the output [1]–[7]. The conventional multi-level inverter structures with the industrial application include flying capacitor (FC), cascade H-bridge (CHB) multi-level and neutral point clamped (NPC) inverters [8]–[11]. Cascaded H-bridges inverter makes for modularized design and package. In CHB, the output levels count may be double than the count of dc sources. CHB can be classified into two groups: asymmetrical and symmetrical structures, which are given by the dc source magnitudes. For a symmetric architecture, the magnitude is the same for the different dc voltage sources. For an asymmetrical architecture, the dc sources magnitudes are selected differently to reach maximum output voltage level [12], [13].

Several new structures for MLIs and their control are developed in [14], [15]. The main driving force for the design of new multilevel inverter structures is the reduction of the components count and total standing voltage (TSV) of the structures [16]–[18].

This research proposes a new module MLI which reduces the components count compared to other MLI structures. The total standing voltage is also reduced in this structure. Next, a new cascaded MLI is introduced by choosing the magnitude of dc sources differently. The capability of the proposed structure is demonstrated by a comparison between the new architecture and other MLIs, including aspects such as quantity of devices, dc sources and the amount of TSV on switches.

II. Proposed Structures

A. Proposed New Module

This paper seeks to introduced the general basic architecture of a 23 voltage-level optimal inverter which is depicted in Fig. 1. The module has five dc sources along with nine unidirectional switching devices $S_1, \bar{S}_1, S_2, \bar{S}_2, T_1, \bar{T}_1, T_2, \bar{T}_2$ and one bidirectional switch S_3. Dc sources values are $(V_1 = V_2, V_3, V_4 = V_5)$ wich are all different. Therefore, the proposed structure offers an asymmetric structure. This module uses a two-switch configurations: unidirectional and bidirectional. To avert short-circuits in the dc sources, the unidirectional switches $S_1, \bar{S}_1, S_2, \bar{S}_2, S_3, T_1, \bar{T}_1, T_2, \bar{T}_2$ operate in an opposite mode. In this basic module, switches $T_1, \bar{T}_1$ are used to generate positive levels and switches $T_2, \bar{T}_2$ are used for negative levels. Considering this information, Table I details the feasible switching combinations of the suggested module. The optimal module creates nine levels by choosing the values of dc sources equally. If these magnitudes are different, the suggested inverter will generate more voltage levels. In this paper, they are considered as follows:

$$V_1 = V_2 = 1V_{dc} \tag{1}$$

$$V_3 = 3V_{dc} \tag{2}$$

$$V_4 = V_5 = 6V_{dc} \tag{3}$$

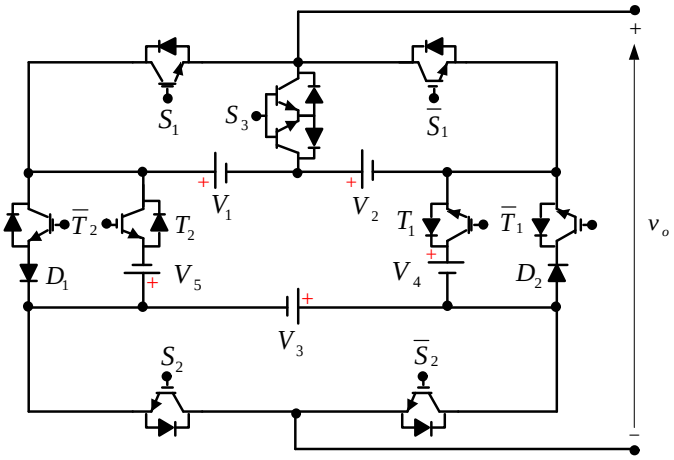

Fig. 1: Topology of the proposed twenty-three levels converter.

TABLE I: Available Switching of the Twenty-Three Levels converter

No.	Output Voltages	S_1	S_2	S_3	T_1	$\bar{T}_1$	T_2	$\bar{T}_2$
1	$+11V_{dc}$	1	1	0	1	0	0	0
2	$+10V_{dc}$	0	1	1	1	0	0	0
3	$+9V_{dc}$	0	1	0	1	0	0	0
4	$+8V_{dc}$	1	0	0	1	0	0	0
5	$+7V_{dc}$	0	0	1	1	0	0	0
6	$+6V_{dc}$	0	0	0	1	0	0	0
7	$+5V_{dc}$	1	1	0	0	1	0	0
8	$+4V_{dc}$	0	1	1	0	1	0	0
9	$+3V_{dc}$	0	1	0	1	1	0	0
10	$+2V_{dc}$	1	0	0	1	1	0	0
11	$+1V_{dc}$	0	0	1	1	1	0	0
12	0	1	1	0	0	0	0	1
13	$-1V_{dc}$	0	1	1	0	0	0	1
14	$-2V_{dc}$	0	1	0	0	0	0	1
15	$-3V_{dc}$	1	0	0	0	0	0	1
16	$-4V_{dc}$	0	0	1	0	0	0	1
17	$-5V_{dc}$	0	0	0	0	0	0	1
18	$-6V_{dc}$	1	1	0	0	0	1	0
19	$-7V_{dc}$	0	1	1	0	0	1	0
20	$-8V_{dc}$	0	1	0	0	0	1	0
21	$-9V_{dc}$	1	0	0	0	0	1	0
22	$-10V_{dc}$	0	0	1	0	0	1	0
23	$-11V_{dc}$	0	0	0	0	0	1	0

The TSV of the switching devices of this inverter is:

$$TSV = V_{S1}+V_{\bar{S}1}+V_{S2}+V_{\bar{S}2}+V_{S3}+V_{T1}+V_{\bar{T}1}+V_{T2}+V_{\bar{T}2} \quad (4)$$

The blocking voltage of the pair of switches is equal to:

$$V_{S1} = V_{\bar{S}1} \quad (5)$$

$$V_{S2} = V_{\bar{S}2} \quad (6)$$

$$V_{\bar{T}1} = V_{\bar{T}2} \quad (7)$$

$$V_{T2} = V_{T2} \quad (8)$$

Thus, TSV by the power switch can be written as follows:

$$TSV = 2(V_{S1} + V_{S2} + V_{\bar{T}1} + V_{T2}) + V_{S3} \quad (9)$$

After calculation, the amount of TSV on each switch is obtained as:

$$V_{S1} = 2V_1 \quad (10)$$

$$V_{S2} = 2V_2 \quad (11)$$

$$V_{S3} = V_1 \quad (12)$$

$$V_{\bar{T}1} = 2V_1 + V_2 + V_3 \quad (13)$$

$$V_{T2} = V_1 + V_2 + V_3 + V_4 \quad (14)$$

Considering the above relations and (9), TSV is defined as:

$$TSV = 13V_1 + 6(V_2 + V_3) \quad (15)$$

B. Proposed Cascaded Connection

Cascading several modules is another way to grow the level counts (Fig. 2). In order to maintain the modularity, each module connected in cascade is assumed to be identical, i.e. the number of components is constant. This will generate more levels count from the cascade connection with a constant number of devices. The equations of components and TSV for the proposed configuration with n modules are detailed in Table II.

TABLE II: Equation of Cascaded Connection

	Based on number n modules
No. Switches	$9n$
No. Drivers	$9n$
No. IGBTs	$12n$
No. Diodes	$12n$
No. Dc Sources	$5n$
TSV	$\sum_{j=1}^{n} 13V_{1j} + 6V_{2j} + 6V_{3j}$

III. Comparisons Studies

In this section a comparative study considering three cascaded MLIs detailed in [8], [11], [16], is presented. This analysis is done to show the capability of the suggested structure.

Table II gives the comparison of the different basic modules of the proposed structure, considering the quantity of components, dc sources and TSV against the quantity of levels in operation mode II and mode III. Various amounts of dc sources are chosen within the presented structures [8], [11], [16]. Thus, in all the structures the best modes of operations are selected which can create a maximum number of levels with the fewer devices count. For the selected structures [8], [11] and [16] two operation modes are considered for a better comparison according to Table IV.

The variation of switches count against the levels count in all presented structures and the proposed structure are all modes indicated in Fig. 3(a). It can be seen that the proposed cascaded MLI produces the same voltage levels count with less switch counts compared to other cascaded MLIs. For example, the proposed structure for the generating 31 voltage levels in the proposed mode III required nine switches and [16] in mode II, twenty-two switches and other structures need up to

TABLE III: Magnitudes Values of dc Voltage Sources and Other Parameters

Modes	Mode I	Mode II	Mode III
Magnitudes dc voltage sources for $j = 1, 2, \cdots, n$	$V_{1j} = V_{2j} = V_{3j} = V_{4j} = V_{5j} = V_{dc}$	$V_{1j} = V_{2j} = V_{dc}$, $V_{3j} = 3V_{dc}$, $V_{4j} = V_{5j} = 6V_{dc}$	$V_{1j} = V_{2j} = 23^{j-1}V_{dc}$, $V_{3j} = 3(23^{j-1})V_{dc}$, $V_{4j} = V_{5j} = 6(23^{j-1})V_{dc}$
Maximum load voltage	$4nV_{dc}$	$11nV_{dc}$	$[(23^n - 1)/2]V_{dc}$
Number of levels	$4n + 1$	$22n + 1$	23^n

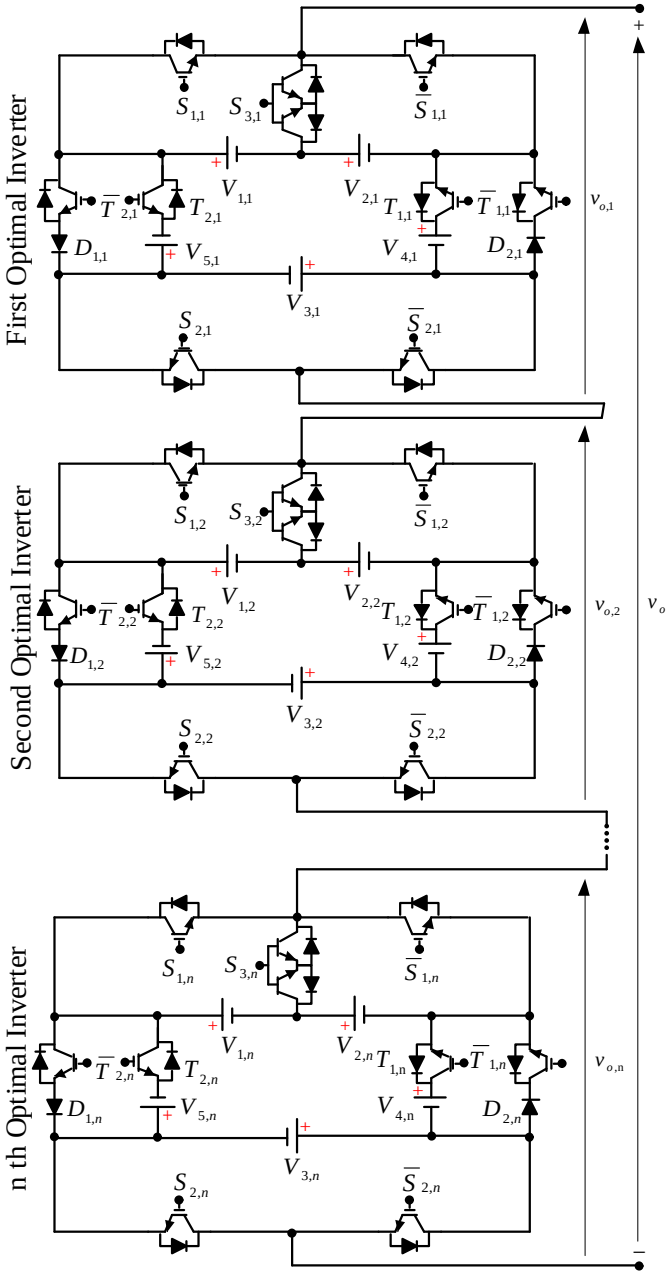

Fig. 2: The cascade arrangement of proposed structure.

twelve switches. In the proposed structure, the driver's count is same as the switches count; so another benefit of the proposed structure is the reduction of the drivers count.

The variation of IGBTs count against the levels count among proposed cascaded MLI and other cascaded MLIs are displayed in Fig. 3(b). The proposed structure produces same levels count with less IGBT count compared to other MLI structures. Similarly, the proposed structure for generating 31 voltage-levels based on mode III requires ten IGBTs, which are lesser amount of IGBTs required compared to mode II in [16], which require twenty-three IGBTs and other structures need up to twelve IGBTs.

Reducing the number of dc voltage sources has been another important criterion in selecting an MLI. Fig. 3(c) indicates the variation between the dc voltage sources count required among the proposed structure and other MLI structures in all modes. According to Fig. 3(c), the proposed structure create same number of levels with lower dc voltage sources in mode II compared to [11], [16] in mode I, except for the CHB and [16] in mode II.

Fig. 3(d) displayed the variation between N_{varity} and levels count in the proposed cascaded MLI and other cascaded MLIs. As can be seen from Fig. 3(d), the cascaded MLI in mode II, creates the same amount of level counts with lower N_{varity} compared to other MLI structures.

The variation in TSV compared to the levels count among the proposed MLI structures are indicated Fig. 3(e). The TSV's values are different in classical CHB and for present structure and MLI structures presented [16] are the same in both of the proposed modes.

According to Fig. 3(d), the proposed cascaded structure is decreasing the value of TSV compared to other MLI structures, except CHB. The CHB must be supplied differently with a higher rate of switches because the rate of voltage on switches is higher in each unit than in the proposed structure. Also, it is clear that CHB structures require many switches, IGBT, and drivers in comparison with the proposed cascaded structure.

Generally, the application of autonomous dc voltage amounts is not possible within MLI structures and the suggested structure. There are two options for solving this issue, the first option applies the multistep transformer that can set a desired input voltage by modifying the secondary turns of the transformer [17]. The second option is employing dc-dc converters that can generate the desired input voltage [18].

Therefore the proposed cascaded structure reduces the components count based on this comparison using the same levels count than other cascaded MLIs.

TABLE IV: Comparison Component Count and Other Calculated Parameters in different MLIs Structures and Proposed Structure

	CHB		**(BUMLI) [11]**		**(ST-Type) [16]**		**Proposed**	
	Binary I	***Tinary II***	***Mode I***	***Mode II***	***Mode I***	***Mode II***	***Mode II***	***Mode III***
N. Switches	$4[\log_2^{(N_L+1)}-1]$	$4\log_3^{N_L}$	$[(5N_L)+87]/12$	$5\log_2^{(N_L+5)/8}$	$(N_L-1)/2$	$10\log_{17}^{N_L}$	$9(N_L-1)/22$	$9\log_{23}^{N_L}$
N. IGBTs	$4[\log_2^{(N_L+1)}-1]$	$4\log_3^{N_L}$	$[(5N_L)+87]/12$	$5\log_2^{(N_L+5)/8}$	$3(N_L-1)/4$	$12\log_{17}^{N_L}$	$10(N_L-1)/22$	$10\log_{23}^{N_L}$
N. Diodes	$4[\log_2^{(N_L+1)}-1]$	$4\log_3^{N_L}$	$[(5N_L)+87]/12$	$5\log_2^{(N_L+5)/8}$	$3(N_L-1)/4$	$12\log_{17}^{N_L}$	$10(N_L-1)/22$	$12\log_{23}^{N_L}$
N. dc sources	$[\log_2^{(N_L+1)}-1]$	$\log_3^{N_L}$	$(N_L+7)/4$	$[3\log_2^{(N_L+5)/8}]+1$	$(N_L-1)/4$	$4\log_{17}^{N_L}$	$5(N_L-1)/22$	$5\log_{23}^{N_L}$
TSV ($\times V_{dc}$)	$2(N_L-1)$	$2(N_L-1)$	$[(10N_L)-9]/3$	$[(7N_L)-2]/2$	$5(N_L-1)/2$	$5(N_L-1)/2$	$67(N_L-1)/22$	$67(N_L-1)/22$
Nvariety	$[\log_2^{(N_L+1)}-1]$	$\log_3^{N_L}$	2	$\log_2^{(N_L+5)/8}$	2	$2\log_{17}^{N_L}$	$(N_L-1)/22$	$3\log_{23}^{N_L}$
Negative Level	With H-bridge		With H-bridge		Inherent		Inherent	

IV. Simulation Results

In order to test the cascaded MLI, a single-phase 45-level cascade structure using mode II is simulated under MATLAB/Simulink software. Fig 4. indicates the power structure of the single-phase 45-level proposed cascaded structure that comprised two basic modules. The whole of semiconductor devices such as switches and diodes are supposed ideal in this simulation. Here, the selected values of input dc voltage sources are established on mode II i.e. $V_{1,1}=V_{2,1}=V_{1,2}=V_{2,2}=50V$, $V_{3,1}=V_{3,2}=150V$, and $V_{4,1}=V_{5,2}=300V$.

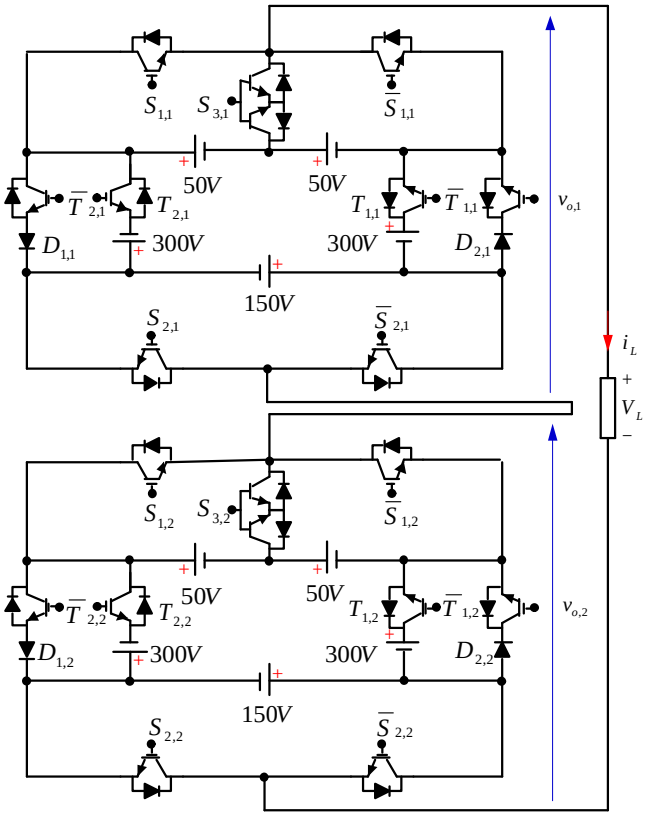

Fig. 4: Power structure of proposed single-phase 45 levels cascaded MLI.

The peak of the output voltage is $1100V$ having a voltage step of $50V$ with $50Hz$ output frequency. For this simulation, the kind of load is a series connected R-L load with amounts of 150Ω and $10mH$.

Fundamental frequency commutation, space vector (SVPWM) and pulse-width modulation (PWM) techniques are conventional control strategies for the switching of MLI

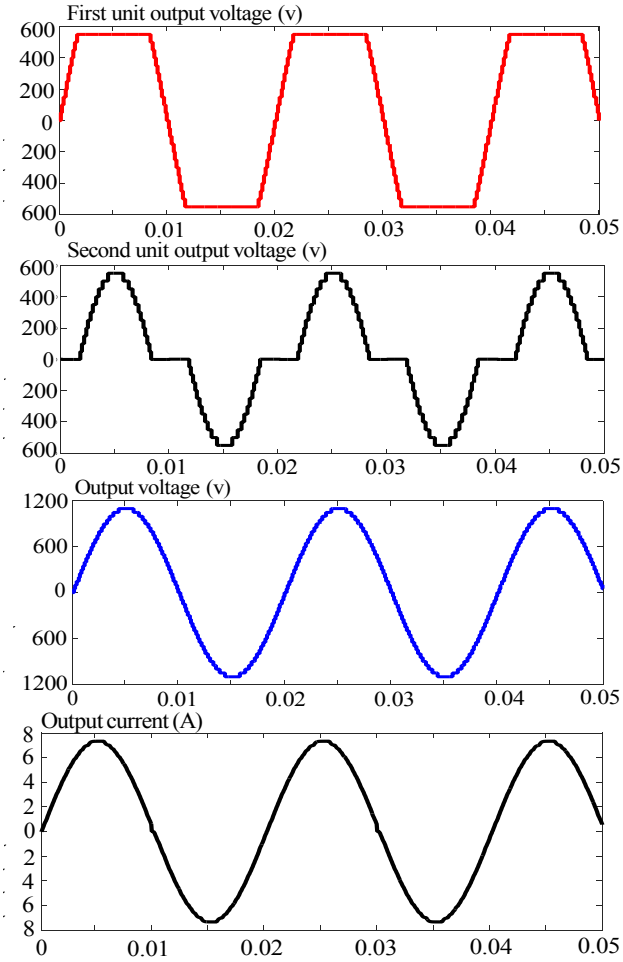

Fig. 5: (a) Simulation study for first optimal inverter output voltage waveform; (b) second optimal inverter output voltage waveform; (c) total output voltage waveform of cascaded MLI; (d) output current waveform of cascaded MLI.

structures [19]. In the proposed cascaded MLI for production of the gate pulse of switches, the fundamental frequency control switching is applied because this strategy works with the fundamental frequency. Namely, this strategy turns on and turns off switches only one time in each switching period, which reduces the switching losses compared to other switching strategies [20].

The output voltage curves of two cascaded module in each module of the proposed cascaded MLI are illustrated in Figs. 5(a) and (b), respectively. Both inverters create the same values of voltages from 0 to $\pm 550V$ with step of $50V$ for the

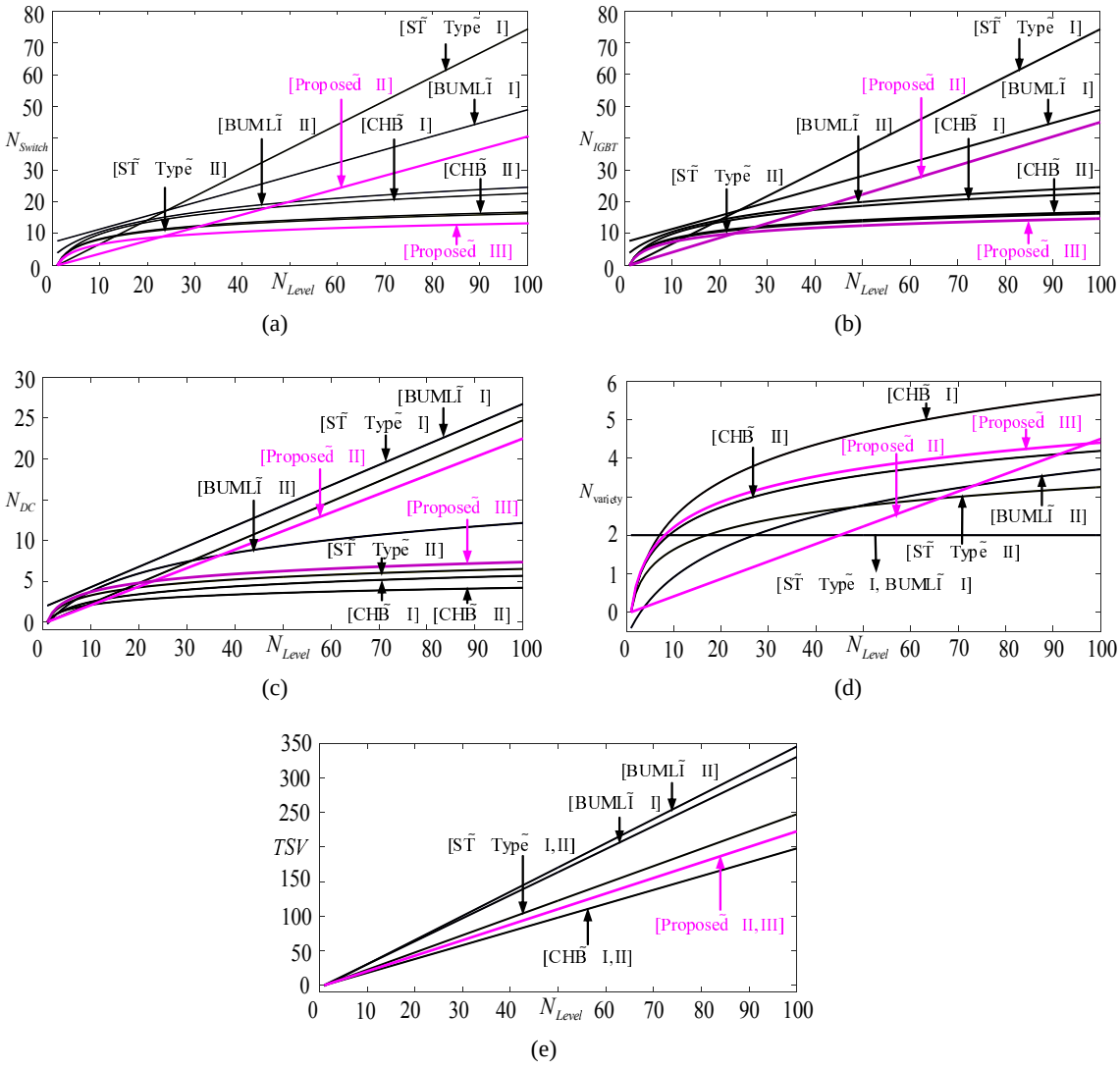

Fig. 3: Variation of; (a) switches count against N_L ; (b) IGBT count against N_L; (c) dc voltage sources count against N_L; (d) $N_variety$ against N_L; (e) TSV against N_L.

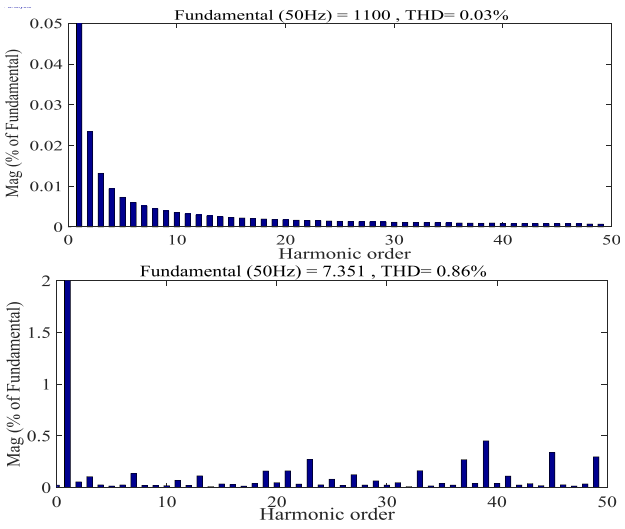

Fig. 6: FFT analysis; (a) for output voltage; (b) for output current.

positive and negative voltages. The 45-levels of the suggested cascaded MLI is illustrated in Fig. 5(c) which is very close to a sinusoidal curve. The voltage's peak of the cascaded connection is $1100V$ with a voltage step of $50V$. Fig. 5(d) illustrates the current output curve of two cascaded modules that peak of current is $7.3A$. FFT values for the output current and voltage are shown in Figs. 6(a) and (b). From this figure, it is evident that the value of FFT for the load voltage is 0.03% and for the output current is 0.86%.

The simulation results of suggested cascaded inverters reconfirm the proposal of new suggested topology based on theoretical design. The suggested cascaded inverter generates a sinusoidal waveform at the output with low harmonics without LC output filters that it can account a superior advantage of the suggested structure.

V. Conclusion

A new 23-level optimal inverter structure has been introduced in this paper with the advantage of having reduced

switching device and dc voltage sources as well as blocking voltage. To achieve all levels, two different modes of dc voltage selection have also been presented. Both of these modes reduce the need for switching devices count and blocking voltage, which makes the proposed structure more practical. An in-depth comparison with other recently presented structures demonstrates the benefit of the presented asymmetric structure. The theoretical explanation of the suggested structure was verified by simulations.

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