SiC power MOSFETs Threshold-voltage hysteresis and its impact on Short Circuit operation

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***Abstract*—V_{TH} subthreshold hysteresis is an aspect of MOSFET's threshold instabilities that is gaining interests in last few years. As a matter of fact, reliability concerns are raised due to the fluctuation of the threshold voltage depending on the previous bias state. The subthreshold drain current, also called drain leakage current, is enhanced after a negative gate bias is applied to put the device in OFF-state. This phenomenon affects the static characteristics and might also change the dynamic behaviour of the devices, but such measurements have not yet been reported. This study reports the impact of the Hysteresis on the Short Circuit behaviour of a commercially available SiC MOSFET. A physical interpretation of the measurement is given in order to provide the fundamentals necessary for the evaluation of the reliability of these power devices.**

Keywords—V_{TH} Hysteresis; V_{TH} instabillities; Short Circuit; SiC MOSFET; reliability

I. INTRODUCTION

It is a well known fact that Wide Band Gap devices present a range of advantages over Si counterparts. The power conversion industry is slowly shifting to converters using this "new" type of devices for providing gain in efficiency, power density and costs through:

- higher breakdown voltage
- lower Ron
- higher temperature
- higher switching frequency

Before we can make proper use of these emerging technologies, industry standards need to be met. Some of the difficulties that prevent WBG devices from becoming mainstream are related to concerns such as reliability and specific driver needs. The reliability of SiC MOSFETs is actually plagued by NBTI [1,4-8] caused mainly by hole trapping in the oxide [2]. This phenomenon affects the operation of the device by shifting its V_{TH} either permanently or in a recoverable manner. The changes in V_{TH} during device operation are a serious reliability issue that needs to be understood and prevented in order to enhance the lifetime of the power devices, thus lowering maintenance costs. As a matter of fact, MOSFETs which have an increasing V_{TH} due to PBTI are likely to not go through the desired level of overdrive and exhibit a slightly higher ON-state resistance. NBTI on the other hand, causes power MOSFETs to exhibit a low V_{TH} and as a consequence to be prone to higher drain leakage currents or even to undesired conduction, which may lead to higher power losses and failure in the worst case.

Another major concern is the right evaluation of the permanent and recoverable parts of BTI since the values reported can depend highly on the measurement protocol. While the permanent part has already been addressed to some extend, only a few studies focus on the recoverable part of the BTI. Theses studies report the effect on the static characteristics of the device and only on the subthreshold domain. In this paper we will focus on the influence of the V_{TH} subthreshold hysteresis on the Short Circuit operation.

II. THEORETICAL BACKGROUND AND RELIABILITY CONCERNS

The Threshold Voltage instabilities are composed of a permanent and a recoverable part. The first is usually observed during HTGB/HTGS and produces a permanent increase/decrease of the V_{TH} of the MOSFET. Most usually, N-channel MOSFETs are more affected by NBTI, whereas P-channel MOSFETs are more affected by PBTI [12]. This is related mostly to the operation of the device itself, since switching the device ON requires a positive gate bias for N-MOSFET and a negative gate bias for P-MOSFETs, as opposed to no bias for OFF state. The presence of broad distributions of slow electron and hole traps defines the dynamics of the BTI and is responsible for the aging of devices.

The recoverable part of the Threshold instability is defined in detail in the next section.

A. What is the Vth subthreshold hysteresis?

It has been observed that the drain leakage current SiC MOSFETs depends on the OFF-state voltage applied on the gate [1,3]. When a negative gate bias is applied for a short time in the OFF-state, the drain current leakage is enhanced for as long as the applied bias is kept under the threshold voltage. If the gate bias is switched beyond the V_{TH}, the leakage current is restored to its normal value. This hysteretic phenomenon can be observed during a static characterisation of the transfer characteristics performed in the upward and the downward

directions using different negative starting gate bias voltages as it is shown in Fig. 1. The V_{TH} subthreshold hysteresis is then defined as the difference between the gate bias in the up-sweep direction, V_G^{UP}, and the gate bias in the down-sweep direction, V_G^{DOWN}, at 100 nA of drain leakage current.

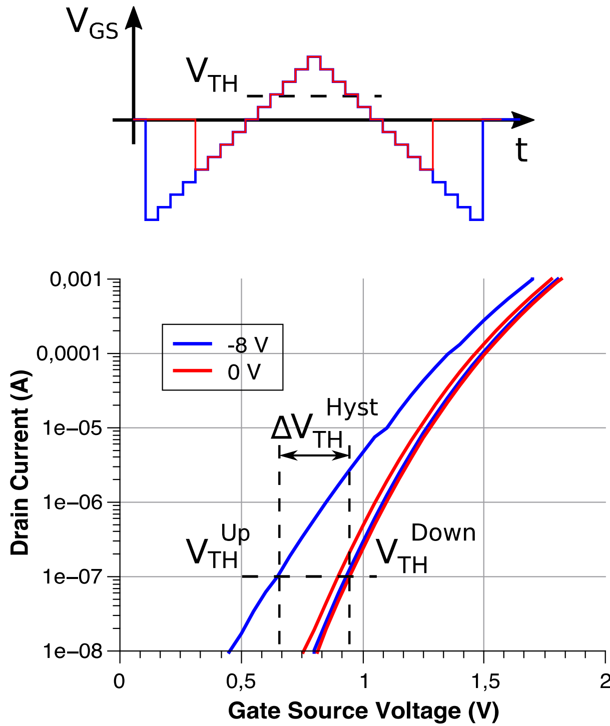

Fig. 1. Characterisation and definition of the Drain current Hysteresis in the subthreshold domain (V_{TH} Subthreshold Hysteresis) of SiC MOSFETs.

The reason behind this behaviour has been attributed mainly to hole trapping in the oxide near the interface [3-7]. The relatively fast hole traps are filled when a negative bias is applied to the gate. The newly trapped holes contribute to the attraction of the electrons at the interface when going from depletion to inversion, producing a higher leakage current. Fig. 2 illustrates the trapping/releasing of holes and electrons in the oxide of 4H-SiC MOSFETs in accumulation and inversion regimes. As can be seen in this figure, when the Fermi level is near the valence band (accumulation) at equilibrium, the hole traps above its level are filled and the electron traps under its level are neutral. When the device is biased in inversion regime and the equilibrium is attained, the holes under the Fermi level are released and the traps are neutral, whereas the electron traps are filled with electrons coming from the channel. From experimental observations on commercially available MOSFETs, the broader distribution of energy levels and bigger concentrations of hole traps compared to electrons traps prevent the later from contributing in a measurable way to the V_{TH} hysteresis. When the equilibrium is not established yet during fast switching from accumulation to inversion, the captured holes will be slowly released. Depending on their emission time constants, their effect can be relevant even beyond the threshold voltage. The effects of such behaviour beyond the threshold voltage are expected to be beneficial since they can improve switching losses due to improved turn-on and by producing an overshoot at the beginning of the switching. This helps to establish the channel faster and provide a lower channel resistance [8]. This statement takes into account neither the possible enhancement of the V_{TH} hysteresis during aging nor its contribution to the current spread in a module composed of several paralleled devices.

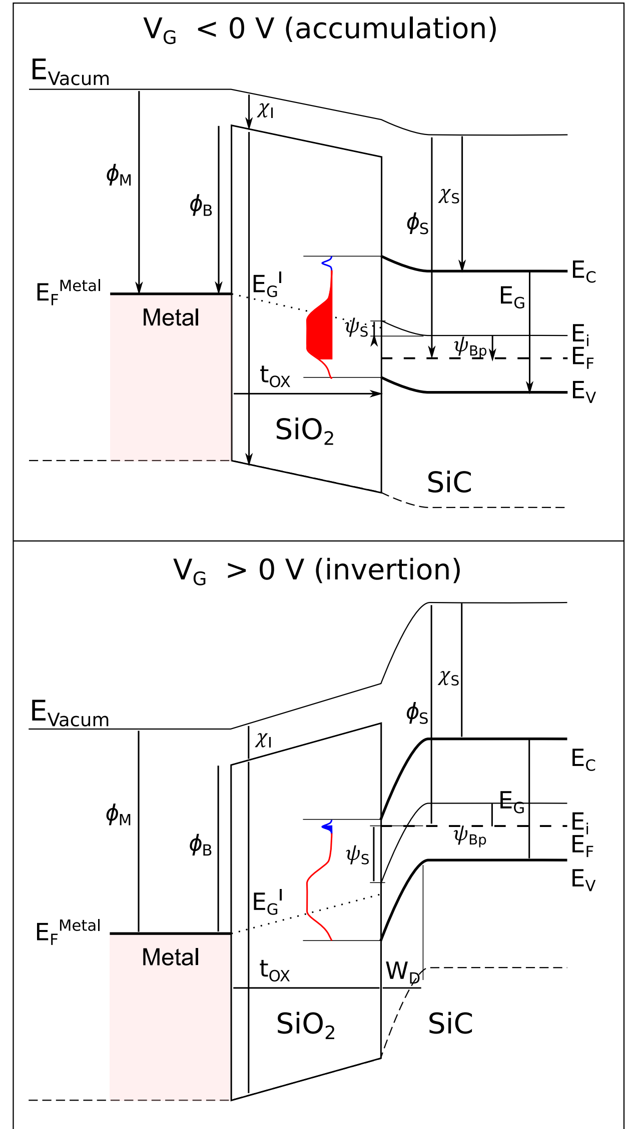

Fig. 2. Schematic illustration of the band diagram of the MOSFET in accumulation and inversion regime. Holes and electrons are trapped/released in the oxide depending on the position of the Fermi level at the interface as related to the distribution of traps in the oxide bandgap. V_{FB} and V_{TH} are affected from the trapped charge in the oxide.

B. Short Circuit operation

These type of events are out of the safe operating area of power devices, but are likely to happen during the lifetime of the device. This requires for the devices to be robust enough to handle a duration of short circuit necessary to detect and remove it before the device failure. In Silicon standards it is defined to be of at least 10 µs.

In literature, it is stated that the V_{TH} subthreshold hysteresis is erased for gate biases beyond the V_{TH} [1,3,4], but it seems that it is the case only for static measurements, where the equilibrium is achieved. Almost Short Circuit tests, with gate bias just above the threshold voltage, show that hysteresis is still present and has a great impact on the device performance [10]. The power dissipation in the device can be almost twice as high, but the testing conditions are far from real applications ones, since the applied gate bias does not provide the required overdrive and thus does not guarantee the lowest possible ON-state resistance. In this paper we show that the hysteresis affects the short circuit operation of commercially available SiC MOSFETs even for real application bias conditions. A comparative study between commercially available SiC MOSFETs from different manufacturers has shown that hysteresis depends on technology (planar and trench) and operating temperature [1]. Such a comparative study on Short Circuit operation can be of great interest when it comes to the reliability of SiC MOSFETs as it can shed some light on the role of the hysteresis in dynamic events and its reliability related issues.

III. MEASURMENT SETUPS

A. Short Circuit Test Setup

For test purposes, 160 mOhm – 1200 V MOSFETS from two different manufacturers were submitted to two types of tests. First one is Almost Short Circuit test, which provides a positive gate bias of 8 V after a negative bias of several seconds. The second one is Short Circuit test, which switches the gate bias from a negative voltage to a 18 V bias. In order to explore the impact of the drain bias, both tests were carried out at 100 V and 400 V. The pulse duration is kept constant of 5 µs for the safety of the device and the test rig. All the test conditions are resumed in Table 1.

TABLE I. TEST PARAMETERS

Drain bias	***Gate bias***	
100 V	Almost SC	Short Circuit
400 V	0 V – 8 V – 5 µs -3 V – 8 V – 5 µs -6 V – 8 V – 5 µs	0 V – 18 V – 5 µs -3 V – 18 V – 5 µs -6 V – 18 V – 5 µs

The custom made test bench is designed to minimise the stray inductances in order to allow for very sharp switching. The input signal is provided by a general purpose generator. The adjustable parameters are the Drain Voltage, which remains constant throughout the test, the ON-state gate bias, defined as V_{GS}^{ON}, the OFF-state gate bias, defined as V_{GS}^{OFF} and the pulse duration. The monitored parameters are the drain current (short circuit current), gate bias voltage and the drain bias voltage, which are measured by means of an oscilloscope. The schematic view of the test setup is shown in Fig. 3.

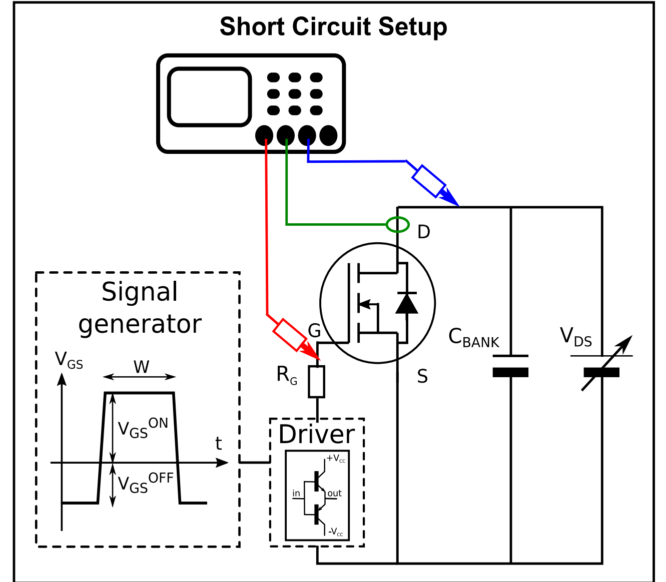

Fig. 3. Custom made Short Circuit setup for SiC MOSFETs.

As explained previously (sect. II.C), the first test does not stress the devices to its limit since the gate bias supplied does not provide the necessary overdrive required for the channel resistance to attain its lowest value. Nevertheless, the power dissipation is high and serious degradation can occur if the device is exposed to large pulse duration.

B. Drain Current Hysteresis Measurement Setup

I(V) measurements have been carried out using a B1505A Power Device Analyser. V_{DS} has been kept constant at 1V, while V_{GS} is swept up and down from a starting voltage of V_{GS}^{Start} up to 4V with a 100mV step. V_{GS}^{Start} ranges from – 20V to 0V with a 1V step. All I(V) measurements were carried out after a fast V_{GS} up-sweep preconditioning from 0V to 10V in order to erase the effects coming from previous biases [6]. The schematic view of the I(V) test setup is illustrated in Fig. 4.

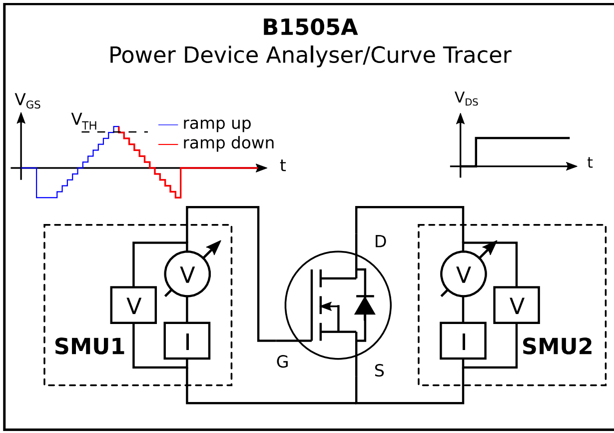

Fig. 4. V_{TH} subthreshold Hysteresis measurement setup. Drain voltage is kept constant whil the Gate bias is swept up from V_{GS}^{Start} to 4V and down to V_{GS}^{Start}.

The V_{TH} hysteresis is determined as explained in sect. II.A.

C. *Temperature dependent Capacitance Measurement Setup*

C(V) tests were carried out in order to determine the flat band voltage V_{FB}, the threshold voltage V_{TH} and the operating (accumulation, depletion or inversion) regime of the MOSFET. The schematic C(V) setup is shown in Fig. 5. Drain and Source electrodes have been shorted during the measurement and the gate voltage V_G was swept from – 20 V to 10 V, with a 100 mV step. An AC signal of 25 mV – 1 MHz was superposed to the DC sweep voltage in order to measure the device capacitance. Measurement have been made for several operating temperatures controlled with a degree precision regulated hot plate, in order to qualitatively guess the distribution of the traps.

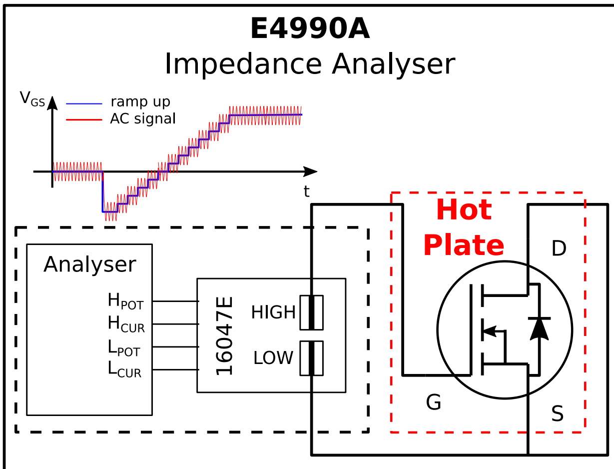

Fig. 5. Temperature dependent capacitance characteristics measurements setup. Drain and Source are shorted and the gate bias is swept up from accumulation to depletion.

IV. Experimental Results

A. *Impact of V_{TH} susbthreshold hysteresis on Short Circuit Operation.*

The Almost Short Circuit Operation exhibits an enhancement of the drain current depending on the OFF-state bias conditions. Fig. 6 and Fig. 7 show the results obtained for two commercially available 160 mOhm – 1200 V MOSFETs from two different manufacturers. When submitted to switching from a negative gate bias of – 6 V to just above the threshold voltage an enhancement of the drain current independently of the drain bias voltage is experienced by the device. Even for – 3 V of negative bias OFF-state, all tests exhibit a slight increase of the drain current. The main reason for this behaviour is attributed to the V_{TH} subthreshold hysteresis even though this phenomenon is said to be recovered for higher bias than the threshold voltage.

The current enhancement raises some serious concerns, since the temperature would also experience an increase. The most concerning fact is that this mode of operation is not a standard one, since it does not provide the necessary gate bias overdrive needed to lower the channel resistance to its minimal value. If the effect of the hysteresis is the same at normal conditions, the lower channel resistance could enhance the short circuit current to dramatic levels and make the device fail to comply with the existing standards.

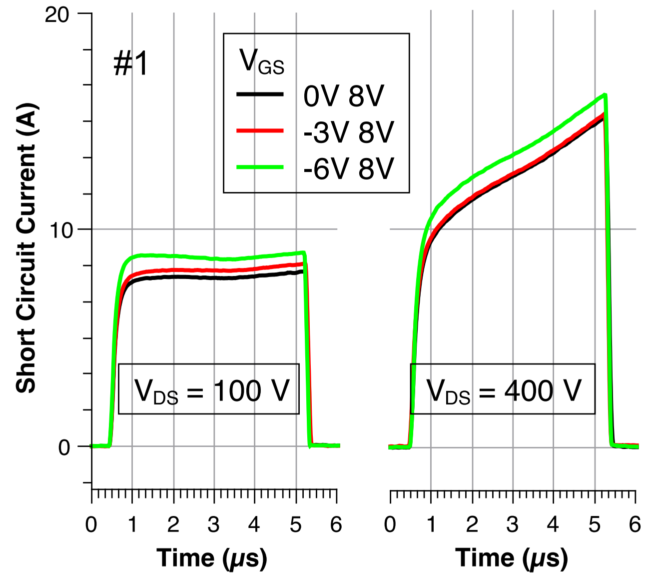

Fig. 6. Almost Short Circuit operation (Gate bias just above threshold) of the 160 mOhm – 1200 V MOSFET from manufacturer 1, depending on the OFF-states bias of the Gate. For lower OFF-state Gate bias, higher Short Circuit Drain current is observed.

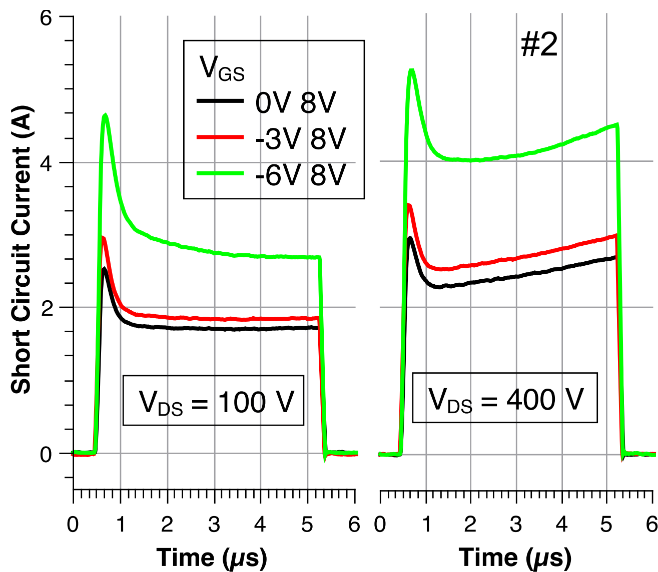

Fig. 7. Almost Short Circuit operation (Gate bias just above threshold) of the 160 mOhm – 1200 V MOSFET depending on the OFF-states bias of the Gate. For lower OFF-state Gate bias, higher Short Circuit Drain current is observed.

Fortunately, the normal Short Circuit conditions (Fig. 8 and 9) show that the value of the hysteresis is reduced and compensates the effect expected by the bias overdrive. Device #1 is not affected by the current enhancement in nominal conditions and shows a full recovery of the hysteresis effect.

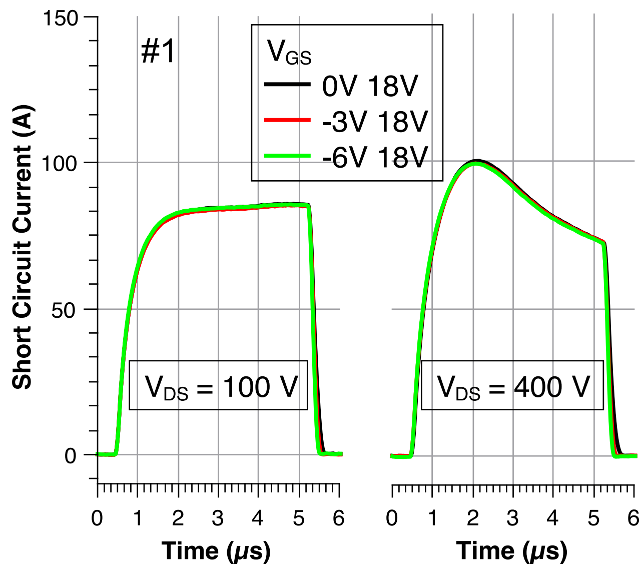

Fig. 8. Short Circuit operation of the commercially available 160 mOhm – 1200 V MOSFET from manufacturer 1, depending on the OFF-states bias of the gate. The value of the OFF-state bias doesn't affect this device neither at 100 V, nor at 400 V of drain bias voltage. The hysteresis has been fully recovered.

On the contrary, MOSFET #2 still exhibits a slight effect of the hysteresis for 100 V drain bias. For 400 V drain bias, the hysteresis effect is negligible and would not produce an increase of the temperature of the device. This means that the hysteresis depends not on the mainly on the negative OFF-state voltage, but on the ON-state gate bias and on the drain voltage as well.

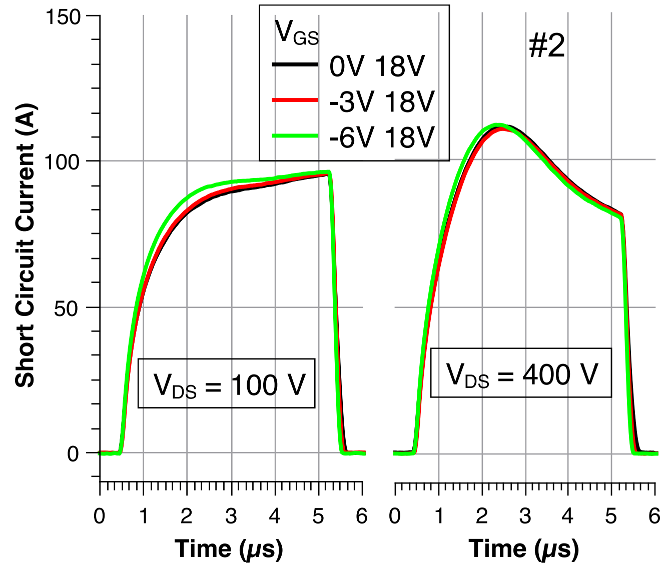

Fig. 9. Short Circuit operation of the commercially available 160 mOhm – 1200 V MOSFET from manufacturer 2, depending on the OFF-states bias of the Gate. A small effect of the hysteresis persist both at 100 V and 400 V of drain bias voltage. The hysteresis has not been fully recovered.

In the case of 100 V drain bias, the hysteretic effect produces a maximal increase of the current of 6 % for – 6 V of OFF-state bias compared to 0 V of OFF-state. It isn't as high as for the Almost Short Circuit test. Nevertheless, an absolute increase of the Short Circuit current of 5 A is observed and shouldn't be neglected, especially when the expectations are to not have any influence of the V_{GS} at OFF-state. The short circuit ruggedness might be challenged when hysteresis is involved, since the critical current may be achieved and make the device to fail before the critical temperature is experienced. This can be explained by the multiple failure mechanisms during Short Circuit [11].

In the case of 400 V drain bias, the hysteretic effect produces a maximal increase of the current of 2,5 % for – 6 V of OFF-state bias compared to 0 V of OFF-state. This enhancement is lower than for 100 V drain bias, which is closer to conditions on real industrial applications. Based on this observation, the effect of the drain voltage can be beneficial as it could help the acceleration of the release of holes from the oxide traps near the interface, thus diminishing the hysteretic behaviour.

To assure the reader that the current enhancement is a result of the V_{TH} hysteresis, the waveforms supplied by the driver to both devices are shown in Fig. 10 and 11 respectively. All the curves overlap at ON-state, independently of the OFF-state.

This is a hard proof that the effect observed both in Almost Short Circuit and Short circuit operation is not due to a design flaw of the driver, or a difference between gate signals depending on the OFF-state.

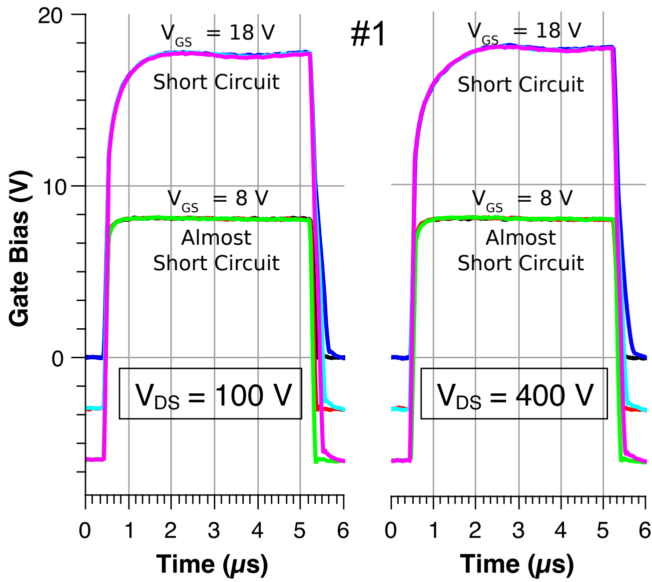

Fig. 10. V_{GS} signals provided by the driver to device #1 during Almost Short Circuit and Short Circuit operation for drain bias of 100 V (left) and 400 V (right). All curves overlap for the ON-state for both 8 V and 18 V independently of the OFF-state voltage. The current enhancement is not due to the gate signal.

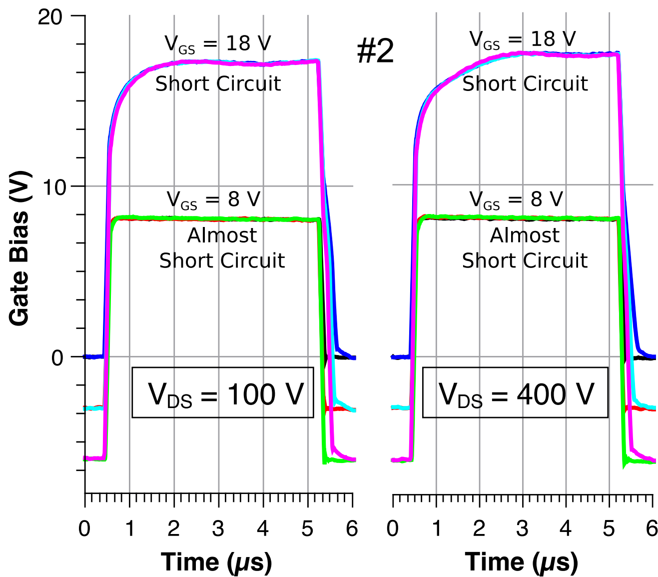

Fig. 11. V_{GS} signals provided by the driver to device #2 during Almost Short Circuit and Short Circuit operation for drain bias of 100 V (left) and 400 V (right). All curves overlap for the ON-state for both 8 V and 18 V independently of the OFF-state voltage. The current enhancement is not due to the gate signal.

The actual Short circuit experiments have been performed at room temperature. High temperature tests are still going on. Further investigations with higher ON-State gate bias and devices coming from different manufacturers will help us elucidate the real impact of the hysteresis on the Short Circuit ruggedness of SiC MOSFETs. The actual results must be correlated with TCAD simulation for a better understanding of the hysteresis dynamics.

B. V_{TH} Subthreshold Hysteresis of 1200 V commercially availlable SiC MOSFETs

The V_{TH} subthreshold hysteresis is shown in Fig. 12. Depending on V_{GS}^{Start} the traces of the log scale transfer characteristics take different paths in the subthreshold domain. The up-sweep traces are identified by the dashed oval and show that as V_{GS}^{Start} approaches 0 V the value of the hysteresis decreases to almost 0 V. In physical term, the hole traps in the oxide are mainly localised at deeper energy levels than the position of the Fermi level for no bias. The down-sweep traces are identified by the small oval. They almost overlap independently of V_{GS}^{Start} showing that near the valence band there is a very low concentration of electron traps.

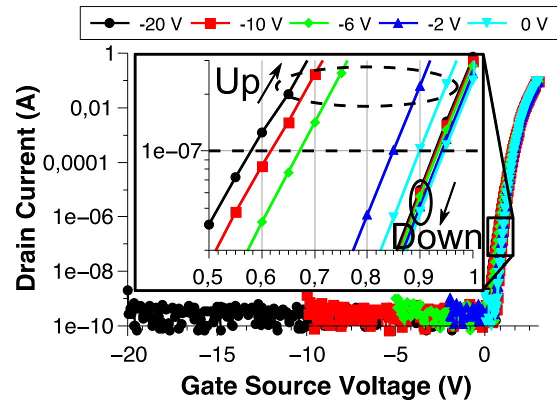

Fig. 12. V_{TH} Subthresold hysteresis effect in a commercial 1200 V 4H-SiC MOSFET transistor.

This behaviour is better resumed in Fig. 13 where the evolution of the hysteresis as a function of the V_{GS}^{Start} is shown. Three typical domains of hysteresis can be distinguished according to its variation. No hysteresis for very high V_{GS}^{Start} since there is lower density of traps in the upper half of the gap and in depletion there are no holes at the interface to be trapped. From -2 V to -10 V, the traps are swept by the Fermi level and their occupancy changes in relation to its level. The more the trapped holes, the higher is the value of the hysteresis. For V_{GS}^{Start} lower then -10 V, almost all the traps are filled so the hysteresis saturates.

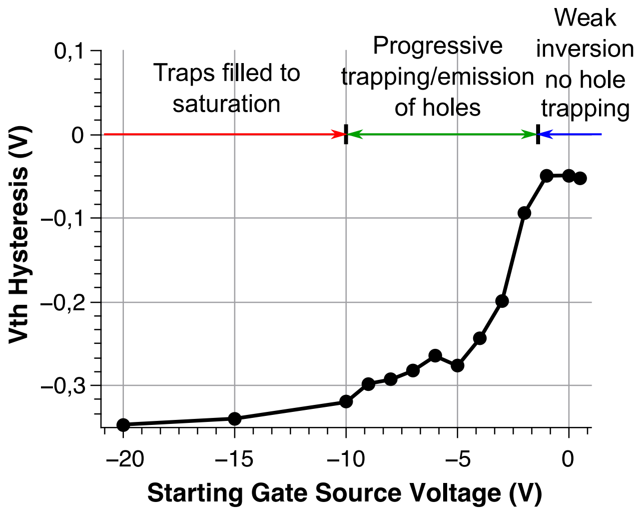

Fig. 13. Dependence of the VTH subthreshold hysteresis on the V_{GS}^{Start} gate bias of a 1200 V commercially available MOSFET.

The position of the holes can be qualitatively estimated from the C(V) characteristic as well. As shown in Fig. 14, only its left part is affected by the temperature, which indicates that the hole traps energy levels are mostly found in the lower part of the gap of SiC. The insets show both a zoom in on the V_{FB} and the V_{TH}, emphasizing the fact that there are no holes trapped above 0 V. The V_{FB} increases at higher temperature, since the trapped holes near the valence band are released faster.

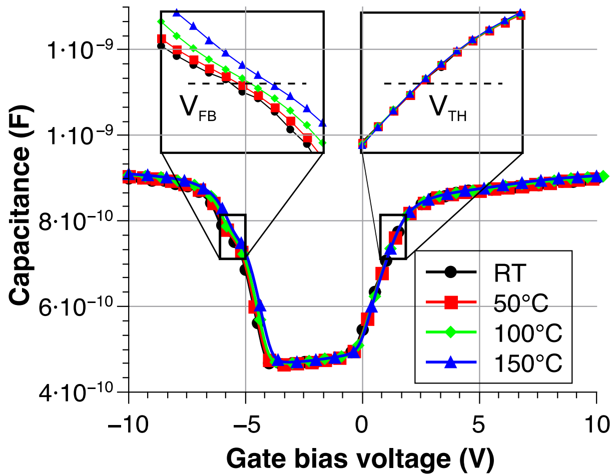

Fig. 14. Gate capacitance is affected by holes trapped near the valence band since the V_{FB} is affected by temperature whereas V_{TH} remains constant.

Even though the hysteresis value extracted from static measurements is lower than 350 mV and 3 V for a V_{GS}^{Start} of -20 V on device #1 and device #2 respectively, we have to consider carefully its dynamic behaviour because at high speed switching, trapped charge might not have enough time to be released and drastically change the behaviour of the device.

V. Conclusions

This paper shows that the V_{TH} subthreshold hysteresis is not limited to the subthreshold domain as it affects the Short Circuit behaviour of MOSFET. The impact of this effect on the reliability has yet to be studied, but is nonetheless to be taken into account when designing power converters.

A physical interpretation of the measurement is given according to the actual ongoing research on hole trapping in the oxide and seems to corroborate with the experimental observations.

The enhancement of the Short Circuit current smaller than 2,5 %. This increment doesn't seem dramatic, but shows that the hysteresis effect is not limited to the subthreshold domain. Further investigations should shed more light on the bespoke phenomenon and provide with data necessary to the manufacturers to fine tune their fabrication processes.

The presented results also show a need for dedicated standards for SiC technology.

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