Multi-Chip SiC MOSFET Power Modules for Standard Manufacturing, Mounting and Cooling

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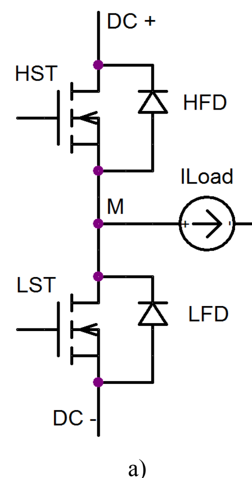
***Abstract*— Taking full advantage of the superior characteristics of SiC Power MOSFETs in the application requires the development of bespoke packaging solutions. Their design needs to thoroughly encompass electro-magnetic and electro-thermal aspects to yield major system-level benefits. New design approaches are needed in particular for parallel multi-chip structures at higher voltage ratings. With the aim of enabling full exploitation of the disruptive potential of SiC technology, this paper proposes a review of learnings made in the development of SiC bespoke power modules, focusing in particular on module designs compatible with the most widely established manufacturing, converter assembly and thermal management solutions for large volume applications.**

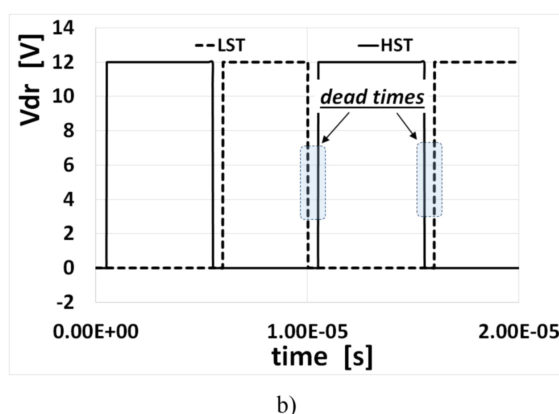
***Keywords*— The authors shall provide up to 4 keywords or phrases (in alphabetical order and separated by commas) to help identify the major topics of the paper.**

I. Introduction

The analysis of a very broad range of power electronic converters can be reduced, in terms of the operation of the semiconductor devices within them, to the study of a half-bridge switch (HBS) architecture with free-wheeling diodes, a characteristic building block of a large category of inverters and dc-dc converters. In the case of power MOSFETs, a typical arrangement is as depicted in Fig. 1 a), which is most often operated with a switching sequence as in Fig. 1 b): between turn-off of the high-side transistor (HST) and turn-on of the low-side one (LST), and vice-versa, a dead-time is interposed to avoid shoot-through phenomena; at least during the dead-times, in the most typical situation of inductive load, continuous current conduction needs to be ensured by the high-side and low-side free-wheeling diodes (HFD and LFD, respectively). After that, synchronous rectification over the transistors channel is a usually implemented option, given the good third quadrant conduction characteristics of MOSFETs. So, the dead-time can be made a more or less significant portion of the overall transistor conduction time in any given modulation scheme, depending primarily on the switching speed capability of the devices. Interest exists to minimize its duration, as this is beneficial from both an efficiency point of view and, in AC systems, for the harmonic signature of the output waveforms [1]. Depending on the specific application and design targets, the freewheeling diodes in the HBS can be intrinsic to the MOSFET (body-diode) or external components can be used (with SiC, the most typical solution is to use Schottky diodes): whenever possible, use of the MOSFET intrinsic diode is looked at as an opportunity to contain costs and increase power density. SiC MOSFET technology has progressed significantly over the last few years and most available devices nowadays, enable a reliable use of the MOSFET body-diode, having solved long-standing issues such as stacking faults and bipolar degradation in the SiC crystal [2].



a)



b)

Fig. 1. a), schematic diagram of a half-bridge switch powering an inductive load; b), corresponding switching sequence implementing synchronous rectification with variable dead-times.

In physically realizing the switch topology of Fig. 1, it is very important to optimize the design of the current commutation loop between HST and LFD and LST and HFD to minimize parasitic inductance components which can result in undesirable voltage overshoots and ringing during the switching transitions. This is best achieved if the devices are co-packaged within the same module, a realization which has recently led to the development of new half-bridge type industrial package standards [3]. SiC MOSFETs can easily be switched ten times faster than Si IGBTs in the same voltage class. So, containment of parasitic inductance associated with layout and assembly is paramount for the achievement of good switching performance.

II. 1.2 KV POWER MODULE

Fig. 2 shows a 3-phase all SiC MOSFET half-bridge power module, developed for use in a 2-level chopper/inverter topology. Fig.2 a) shows a detailed view of the individual switch: only MOSFETs were used, rated at 1.2 kV-30 A, without nay external free-wheeling diode.

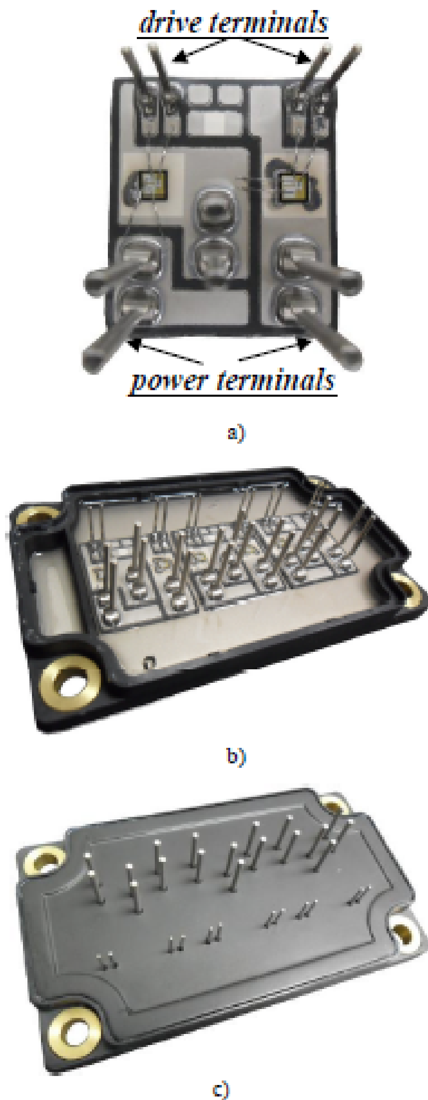


Fig. 2. Assembled switches a), full power module b) and encapsulated device c).

The main objectives in the development and testing of this module were: to assess the reliability of a small footprint/high-power density lightweight solution with thinned baseplate; investigate the electro-thermal and electro-magnetic operational limits. Extensive design and experimental characterization results are reported in [4, 5].

The design feature which mainly distinguish it from established solutions developed for Si are:

- built-in reliability design approach, with optimum matching of substrate, base-plate and solder materials and thicknesses to yield minimum thermo-mechanical stresses and the required target reliability, using a thin baseplate (2mm vs. the more traditional 3mm);
- low-parasitic inductance by layout design and increased power connector sizes;
- full separation of the gate-drive and power loops, so as to avoid delayed switching and higher power dissipation due voltage drops on the gate-loop internal source terminal parasitic inductance.

The module was instrumental in demonstrating extremely high switching speeds, well below 100 ns over a very broad range of bias conditions. Fig. 3 shows results for the turn-on and turn-off waveforms at 540 V input voltage and 20 A peak output current.

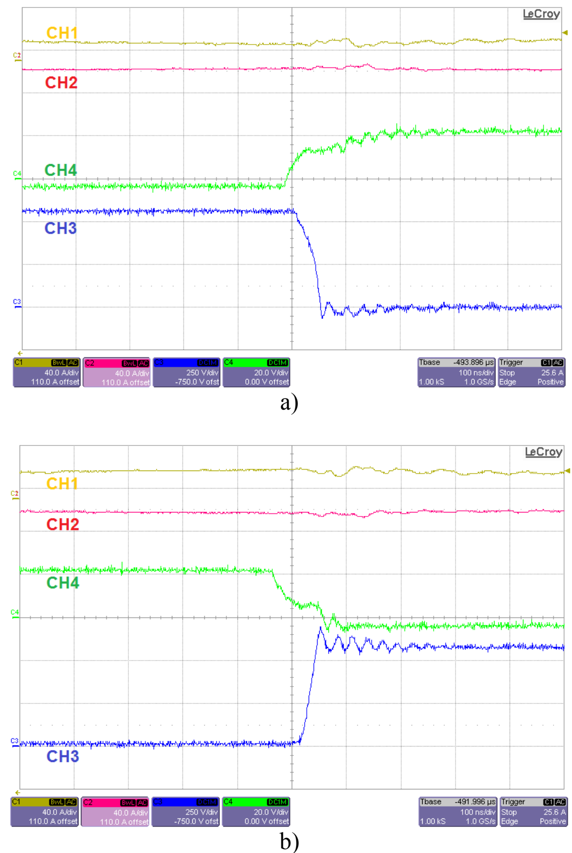


Fig. 3. Turn-on, a), and turn-off waveforms, b), at fsw=100 kHz, full-load (CH1 and CH2: Current in phase A and B, 40A/div, CH3:Vds=250V/div, CH4:Vgs=20V/div, timebase=100ns/div).

It was also used to illustrate the drastic reduction in output filter inductance that can be achieved by the increased switching frequencies, in particular going up to 100 kHz at an output load of 6 kW. Fig. 4 a) shows the phase output currents with a filter inductance of 3 mH; Fig. 4 b) shows the phase output current without any output filter inductance other than that associated with connection cables and resistors.

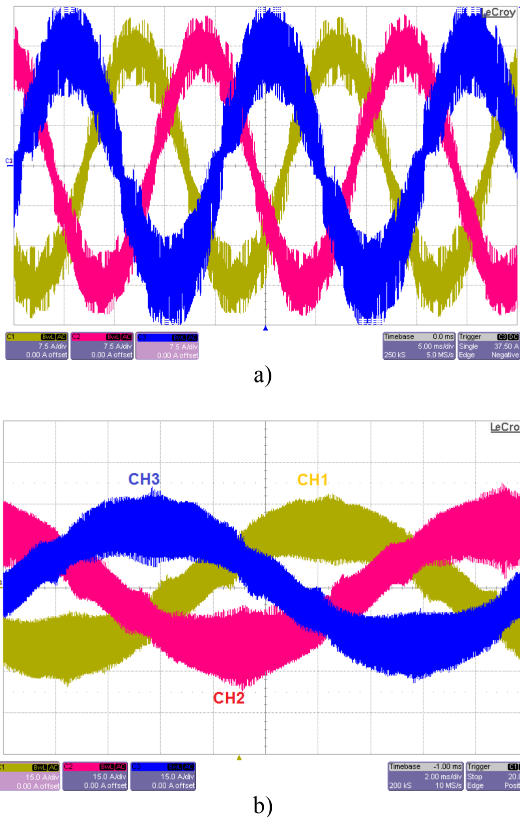


Fig. 4. Output current waveforms at f_s=100 kHz, full-load (CH1= Phase A current 15 A/div, CH2= Phase B current 15 A/div, CH3= Phase C current 15A/div, timebase= 2ms/div).

Fig. 5 shows the measured efficiency over switching frequency at 6 kW output power: as can be seen, the performance at higher switching frequencies remains credible and viable, especially for motor-drive type applications, where the overall system efficiency is in any case not primarily determined by the power electronics.

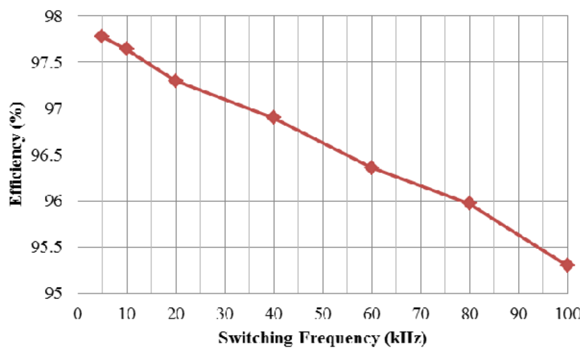


Fig. 5. Efficiency versus switching frequency for an output power of 6 kW.

In terms of handling the higher losses at module level, it is interesting to also point out that the module was operated safely without any heatsink, reaching a baseplate temperature of 90 °C at 2.5 kW output load for a 5 kHz switching frequency and 1.5 kW output load for an 80 kHz switching frequency. Fig. 6 shows the corresponding thermal maps of the module baseplate.

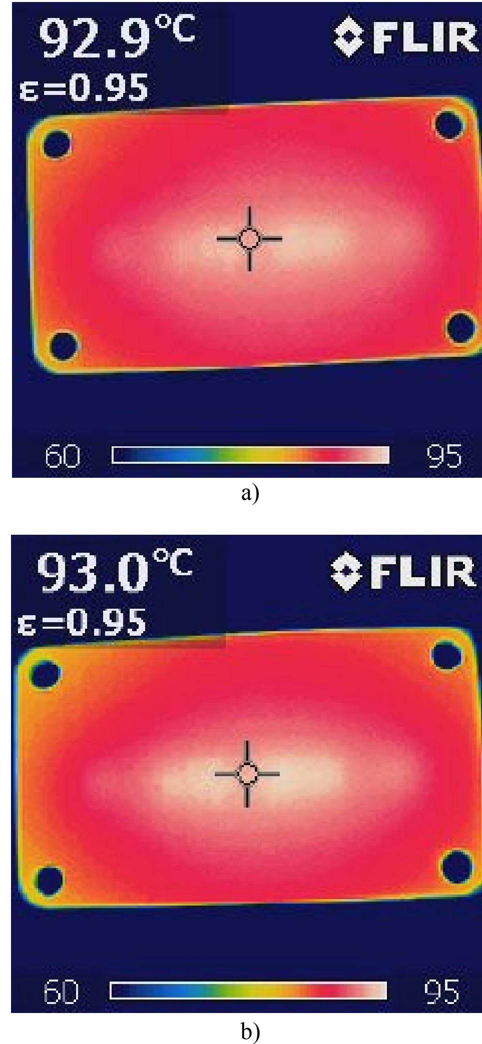


Fig. 6. Thermal maps of the module baseplate: a), P_{OUT}=2.5 kW and fs=5kHz; b), P_{OUT}=1.5kW and fs=80 kHz.

The main limitation in deriving a markedly disruptive performance in the application of the module was due relatively large common mode currents flowing at the higher end of the switching frequency range. In a power module, common mode currents are mainly contributed by the parasitic capacitance associated with terminal M in the schematic illustration of Fig. 1 a). In a SiC MOSFET HBS, this node swings between DC+ and DC- voltages at high frequencies and relatively high voltages, with very high dV/dt's. So, it is crucial to contain the value of parasitic capacitance between this node and ground if common mode currents are to be limited. This aspect was duly taken into account in the design of a second module generation, populated this time with state-of-the-art 3.3 kV SiC MOSFETs [6].

III. 3.3 KV POWER MODULE

Here, a single-phase HBS was built, but using two parallel devices for both the HSM and LSM to achieve a nominal 100 A current rating and still relying only on the transistors body-didoe for the current-freehweeling action. The module design is illsutrated in Fig. 7 a). Many of the design features of the previous version are kept for minimsing parasitic inductance and ensuring a fast switching symmetrically balanced electro-magnetic circuit. However, the extension of the mounting track for the LSM collector is intentionally reduced to minise commone mode capacitance towards the baseplate underneath (grounded in the application). The amount of metal track size reduction that can be realistically achieved is determined by the need for trading-off on thermal performance and esnuring uniform temeprature distribution and symmetrical electro-thermal performance for all devices. Design optimisation was based on extensive structural simulation, of the kind shown in Fig. 7 b) [7].

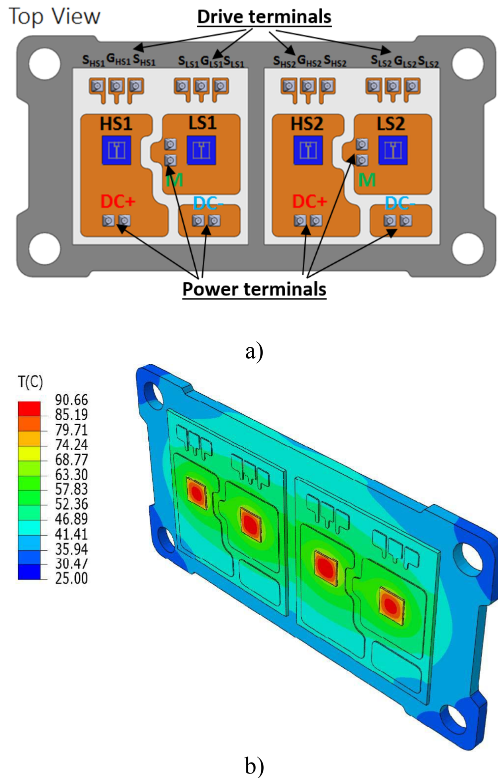


Fig. 7. Module design of the 3.3 kV-100A half-bridge module: a), module layout; b), thermal simulation showing uniform temperature distribution even with asymmetrical sizing of the copper tracks used for mounting and cooling the chips.

Fig. 8 shows the module hardware prototype, fully covered in insulating gel, but still without the lid. The module was tested extensively for switching performance of the single and parallel dies, including a parametric analysis of switching energy over temperature, load current and input voltage. Reported in Fig. 9 are representative voltage and current switching waveforms at 1.8 kV and 30 A (per transistor), which show the ability to operate with significant dV/dt's values.

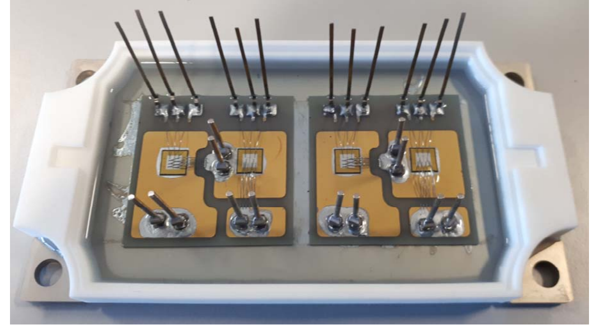


Fig. 8. 3.3 kV -100 A SiC MOSFET power module prototype.

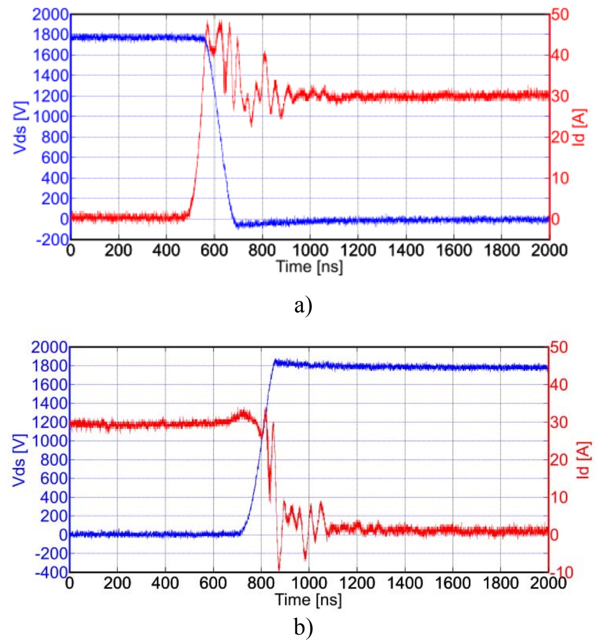


Fig. 9. Representative voltage and current waveforms at turn-on, a), and turn-off, b).

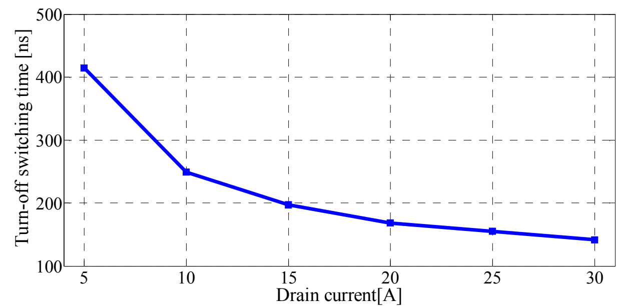


Fig. 10. Turn-off switching time as a function of load current.

Interesting in relation to this are the results of Fig. 10, which report a marked dependence of the turn-off switching time as a function of the load current, an effect which was not highlighted in the testing of devices with lower voltage rating and which needs to be duly taken into account in the optimization of the design parameters of a power converter. The longer switching times do not adversely affect switching energy, since they are associated with lower load current values. Moreover,

since realistically the target switching frequencies at higher voltages are reduced compared to lower voltage applications, the maximum measured values are deemed fully suitable for the achievement of excellent performance.

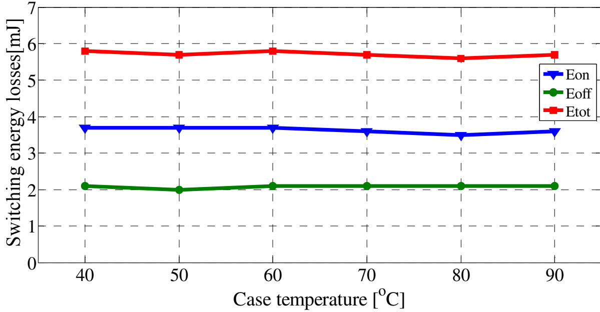


Fig. 10. Turn-off switching time as a function of load current.

IV. Multi-Chip Power Module Robustness

In power electronics applications, semiconductor power devices are intended mainly to operate as high-frequency switches, which are either fully on, that is, conducting current with virtually zero voltage drop between their terminals, or fully off, that is, blocking voltage with virtually zero current through them. The on and off bias points and the switching trajectories between the two points need to be fully contained within the so-called *Safe Operating Area* (SOA) of the transistors or diodes. The situation is illustrated in Fig. 11.

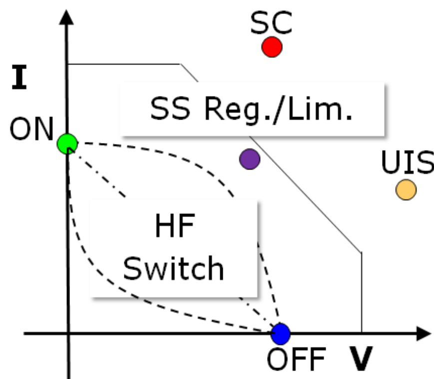
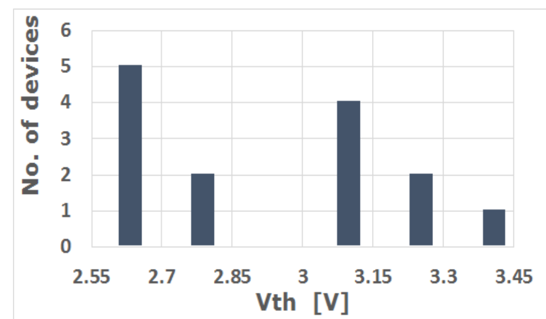


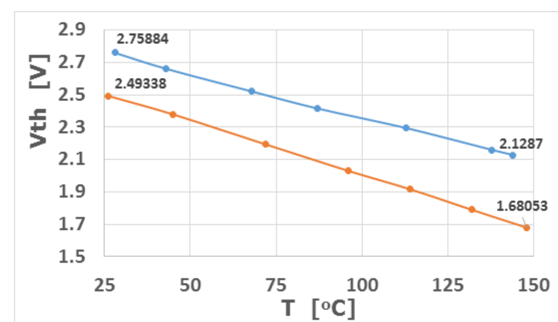
Fig. 11. Illustration of power device operation against its nominal SOA.

As depicted, next to their nominal operation, the devices are also expected to safely withstand a number of *Edge-of-* or *Out-of*-SOA transient events: short circuit (SC) is probably the most important one, being required in virtually all motor drives applications (a very large percentage of all power electronics applications); for the specific case of SiC MOSFETs, unclamped inductive switching (UIS) is also of interest, since the material properties and device features enable dissipation of significant energy values in the avalanche regime [8]; solid-state (SS) current regulation and limiting are gaining more and more relevance. Although some of these operational situations may be non-intentional, that does not necessarily mean that they are infrequent during system operation. So, relevant are both the devices *single event* withstand capability and its aging as a result of *repetitive stress* application. The performance, robustness and failure mechanisms of single SiC devices have been exhaustively explored in relatively recent studies [1, 8-9], which have generally highlighted steady progress in technology development, with the recent overcoming of long-standing issues, such as threshold voltage, *Vth*, stability of SiC MOS interfaces or body-diode degradation as a result of stacking-faults and bipolar degradation. Also, short-circuit and avalanche robustness have been investigated in depth, pointing out limitations and ways to improve robustness where strictly necessary [10-11]. Thorough investigations of parallel chips robustness are, on the other hand, still wanting, with very few initial studies published on the subject [12].

For example, Fig. 12 a) reports a measure of the threshold-voltage value, *Vth*, on a number of commercial 1.2 kV devices (not of latest generation): the values are contained within data-sheet specification, but the spread is much more significant than in silicon and in view of the switching speed of SiC MOSFETs. Moreover, the quantitative spread is temperature dependent, as Fig. 12 b) shows, so that transistors with a Vth difference of about 250 mV at ambient temperature may end up having nearly twice as much as the temperature is increases towards the nominal maximum of 150 °C (it is worth considering that during transient operation, the actual device junction temperature can rise well beyond the maximum nominal steady-state value, which is mainly package related).



a)



b)

Fig. 12. Measured *Vth* distribution on a sample population of 14 SiC MOSFETs (1200V – 80 mΩ; data-sheet specification is 2-4 V), a), and *Vth* temperature variation for two devices, b).

As further shown in Fig. 13, which reports the measured short circuit current waveforms for some of the devices from the lot of Fig. 12, the implication of the *Vth* difference alone can be, for instance, that devices used in parallel within a module are actually exposed to very different stress levels during short-circuit events, with a significant difference in the maximum chip temperature in terms of module reliability and lifetime and inherent presence of a *weak-spot* for parallel use, requesting the introduction of bespoke derating measures.

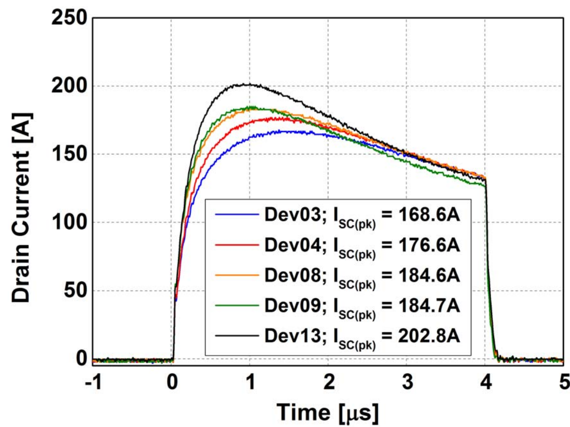


Fig. 13. Experimental short-circuit waveforms for *Vth* ranging between 2.55 and 3.45 V (in these tests, V_{DS} = 600 V, T_{CASE} = 300 K and V_{GS} = 18 V).

In relation to unclamped inductive switching and avalanche energy dissipation capability, Fig. 14 reports the distribution of measured breakdown voltage, V_{BD}, against *Vth*. Here, the spread is quite contained, compatible with statistical device design and processing parameters spread. It is worth stressing that although the results of Fig. 14 seem to indicate a correlation between V_{BD} and *Vth*, specifically, that devices with lower *Vth* exhibit higher V_{BD}, the present interpretation is actually only that probably devices from two distinct manufacturing batches were tested here, one group having somewhat higher V_{BD} and one lower and each group featuring some spread in their *Vth* value.

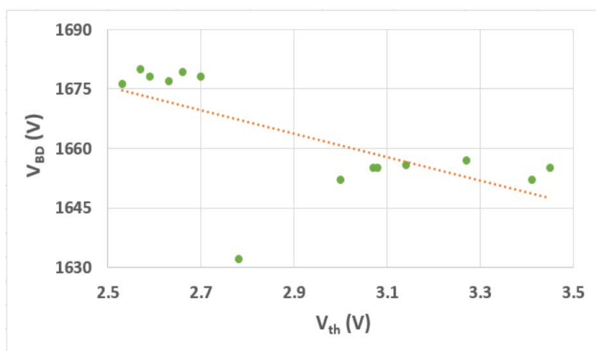


Fig. 14. Measured breakdown voltage, V_{BD}, over threshold voltage, *Vth*, for the same devices used for the results of Fig. 12.

Results of dynamic UIS tests run with different device pairs connected in parallel, have consistently indicated a behavior as illustrated by the results of Fig. 15, which shows representative drain-source voltage, V_{DS}, and drain current, I_D, for two transistors (indicated as Dev06 and Dev14, respectively) during avalanche breakdown. As can be seen, when the SiC MOSFETs are first turned-off, at time t=0 µs, one of the two (Dev06) takes on the full current, while the other (Dev14), turns-off: this is attributed to Dev14 having a higher Vth value and thus turning-off sooner than Dev06. Dev06 is subsequently also the first to go into avalanche breakdown, having also slightly lower value of V_{BD}; however, shortly after avalanche has commenced, V_{BD}, of Dev06 increases as a result of temperature and soon causes Dev14 to also avalanche. Thus, the load current tends to be shared uniformly and tests run at higher current values have confirmed such behavior and the possibility to robustly use devices in parallel for energy dissipation of UIS.

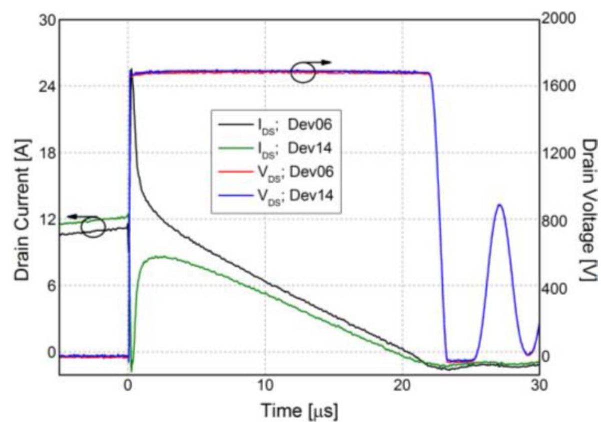


Fig. 15. Measured drain current, I_D, and drain-source voltage, V_{DS}, of two parallel SiC MOSFETs during a UIS event.

Functional tests on parallel devices in the higher voltage class, 3.3 kV, have also indicated very good parallel performance, with very contained spread of the main device parameters [13]. For illustration, Fig. 16 proposes the body-diode currents of two parallel MOSFETs during free-wheeling and subsequent turn-off: the only apparent difference is in the value of the reverse recovery current peak.

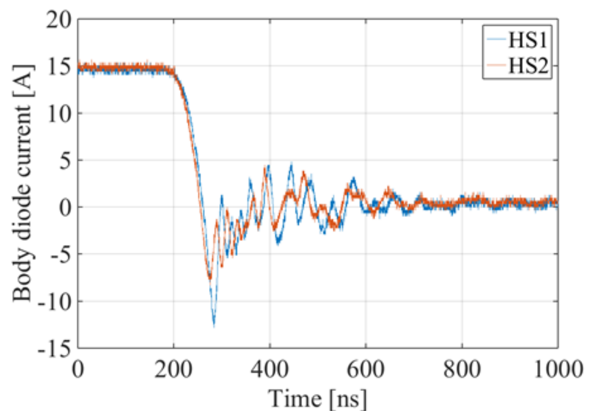


Fig. 16. Measured breakdown voltage, V_{BD}, over threshold voltage, *Vth*, for the same devices used for the results of Fig. 12.

V. CONCLUSION

This paper has presented and discussed the development of multi-chip power modules using well established design solutions and assembly methodologies for the specific case of fast-switching SiC power MOSFETs of different voltage classes. Next to the broadly acknowledged need to minimize parasitic inductance, largely shared with Si power modules, key aspects of performant design in the case of SiC are:

- separation of gate drive and load current switching loops;
- minimization of parasitic capacitance and common mode currents;
- symmetry of layout and device screening for device parameter matching in parallel operation.

Hints at the need for bespoke investigations of SiC MOSFET paralleling derating guidelines have also been proposed and, in the near future, it is expected that comprehensive evaluation of higher voltage (3.3 kV, 6.5 kV) device robustness towards short-circuit and other stressful events will also commence. Particular attention in this regard is dedicated to avalanche robustness and unclamped inductive switching capability: this feature is only exploited in Si at low voltages (indicatively, below 100-200 V) and has come as the result of significant effort invested in the improvement of device design and manufacturing to avoid the activation of the parasitic bipolar BJT in MOSFETs. In SiC, the ability to withstand significant avalanche energy dissipation comes as a result of the material properties (the wider band-gap) and can in principle be taken advantage of even in high voltage devices. Indeed, this might very well be one feature enabling a disruptive revision of traditional power system design in the high voltage high power class (e.g., railway, naval, surface traction; wind), revisiting established voltage de-rating rules and snubbering/protection circuit deployment towards more competitive system development. As such, ability to exploit this particular feature could play a key role in the discussion on compensating the higher purchase price of the semiconductors with cost reductions in other parts of the system. For this to happen, however, the margin between nominal and actual breakdown voltage will need to decrease or shift towards multi-level topologies employing devices with lower voltage rating should be considered. Concurrent improvements in passive device technology will be crucial for enabling more marked improvements and achieving best performance in future SiC based power converters.

Finally, alternative mounting schemes characterized in particular by the removal of the base-plate or its replacement with either ceramic or Insulated Metal Substrate (IMS) components have also been presented, which enable more performant or more cost-effective design, contributing the possibility of counterbalancing higher semiconductor material price, with savings elsewhere in the system [14, 15].

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