Power Density Optimization of a DC/DC Converter for an Aircraft Supercapacitors Energy Storage

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***Abstract*—This paper presents a computationally efficient design algorithm for a DC/DC converter, optimized for power density. Interleaving and series-connecting of several converter cells is included in the analysis. The choice of the converter design parameters, such as the semiconductor devices or the number of interleaved converter cells may have unpredictable impacts on the resulting power density. Therefore, fully analytical models of the operating waveforms, the converter losses and also the converter weight are introduced. Using those models, an algorithm is developed to optimize a 2 kW DC/DC converter for an aircraft supercapacitors energy storage system.**

***Index Terms*—Synchronous Buck Converter, Modelling, Optimization, Power density, Supercapacitor, More Electric Aircraft**

I. Introduction

The More Electric Aircraft (MEA) is a new concept in the development of next-generation aircrafts [1, 2]. Traditional hydraulic and pneumatic actuators used to drive critical flying surfaces are increasingly replaced by electrical systems, which have the potential to be significantly more efficient and light-weight, which would reflect in lower fuel consumption. However, adopting the MEA concept imposes challenges to the design of the electrical power system as its power rating significantly increases. Therefore, it is crucial that the electrical components are optimized for power density.

This work is related to the design of a supercapacitor energy storage system which is needed to smoothen the ripple of the power system, deal with regeneration and enhance the power surge capability. The system will consist of a supercapacitor stack, interfaced with the aircraft's 270 V DC bus via a bidirectional non-isolated DC/DC converter and the synchronous buck converter has been chosen as the preferred topology for this study. In addition to the generic topology, more complex variants such as interleaved (parallel channels) and cascaded (series connection of cells) converters are considered.

Deciding on design parameters of the converter is a complex task. The choice of semiconductor devices, the number of interleaved half bridges, the amount of inductance, the switching frequency, all those parameters have great influence on power density which are hard to predict. The approach in this paper helps to establish a link of analytical equations between the design variables and the power density.

The synchronous buck converter, although being a hard-switched topology, has been shown to achieve attractive power densities [3, 4] when using wide-bandgap (WBG) power semiconductors operating at hundreds of kHz which enables minimization of magnetics whilst the cooling requirements remain reasonable due to the lower switching losses.

Analytical models providing an evaluation of current and voltage waveforms in this topology and the evaluation of the losses have been investigated in [5–7], also weight minimizations have been proposed in [7, 8]. The benefits of interleaving have been analyzed in [6, 9–11]. This paper adds the analysis of cascaded converters and further modelling of the converter weight. Moreover, the ripple charge of the input capacitor is analyzed for interleaved converters.

The optimization procedure in this work is based on fully analytical modelling and consists of three layers, as proposed in [12]: First, the converter current waveforms are analyzed and key variables, such as for example RMS or ripple currents, are derived. Based on these, an analytical loss model of both active and passive components is developed. A model to estimate the weight of the main components is added, which, for example, links the converter losses to the weight of the required cooling system.

As the adopted models are fully analytical, there is no need to run time-consuming simulations in time domain. Hence, the major advantage of this technique is its speed in calculation whilst being able to assess a wide range of design configurations. This approach has some limitations, for example the high-frequency losses in the magnetics, which are difficult to assess analytically.

The paper is structured as follows: In section II, the synchronous buck converter topology and its variations are introduced. Sections III, IV and V demonstrate the modelling of the operating waveforms, the losses and the weight, respectively. Section VI presents the optimization procedure. In section VII, the results are summarized and the conclusions are presented in section VIII.

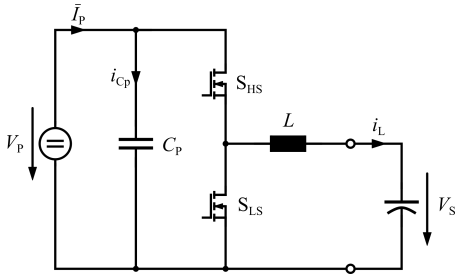


Figure 1: The generic synchronous buck converter topology

II. The Synchronous Buck Converter

In Fig. 1, the generic synchronous buck converter is shown. In the following, all current and voltage equations will be related to the directions introduced in Fig. 1. The supercapacitor system is modeled as an ideal voltage source V_S. A positive power transfer means charging the supercapacitor from the DC bus V_P and a negative power transfer means discharging the supercapacitor into the DC bus. The basic requirements and assumptions about this application are summarized as follows:

- The rated power of the converter is $P = 2\,\mathrm{kW}$
- The DC bus is the 270 V DC bus in aircraft, fulfilling the requirements of Mil-Std-704F [13]
- The supercapacitor stack consists of k cells connected in series. Each cell is assumed to be fully charged at $V_\mathrm{cell} = 2.50\,\mathrm{V}$. Additionally, the supercapacitor shall discharge to 50 % of the maximum voltage, which corresponds to a minimum cell voltage of 1.25 V, to avoid increasing the output current and hence, losses. This will guarantee an energy extraction of 75 % of nominal energy stored.
- Three supercapacitor stack configurations are analyzed, having a different number k of series-connected cells and thus, different rated voltage ranges V_S:
  1) $k = 24 \Longrightarrow V_\mathrm{S} = 30 \ldots 60\,\mathrm{V}$
  2) $k = 48 \Longrightarrow V_\mathrm{S} = 60 \ldots 120\,\mathrm{V}$
  3) $k = 96 \Longrightarrow V_\mathrm{S} = 120 \ldots 240\,\mathrm{V}$
- Interleaving of parallel converters is considered for $N = 1 \ldots 3$ half bridges
- Cascading series-connected converters is considered for $M = 1,\ 2,\ 4$ half bridges

A. Interleaving

Interleaving is a concept used in power electronic converters [9, 10]. The interleaved variant of the synchronous buck converter is shown in Fig. 2.

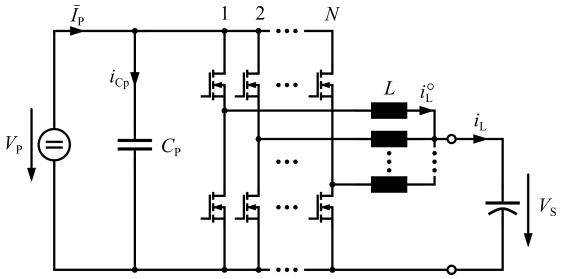


Figure 2: The interleaved synchronous buck converter topology

Instead of processing all of the supercapacitor current with only one converter, it is shared between N paralleled phases, which individually operate more efficiently. Additionally, the PWM patterns are phase-shifted in time. This way, the ripple currents of each interleaved phase, as seen from both the supercapacitor stack and the 270 V DC bus, partly cancel out. For the j'th phase, the time delay $t_\mathrm{d,j}$ is given as follows:

$$t_\mathrm{d,j} = \frac{j-1}{N} \cdot T_\mathrm{sw} \tag{1}$$

T_sw denotes the switching time period. The phase-shift also implies that the frequency $f_\mathrm{sw,eff}$ of the supercapacitor and the input capacitor ripple currents is increased by a multiple N compared to the switching frequency f_sw of the single phase:

$$f_\mathrm{sw,eff} = N \cdot f_\mathrm{sw} \tag{2}$$

At light load where usually efficiency drops, disabling some phases may facilitate an increase in efficiency as the remaining phases will operate at higher loading. This technique is called phase-shedding [5, 14].

B. Cascading

In addition to interleaving, also the series connection will be analyzed in this work. Fig. 3 shows the concept of cascading: The supercapacitor is split into M banks, which consist of

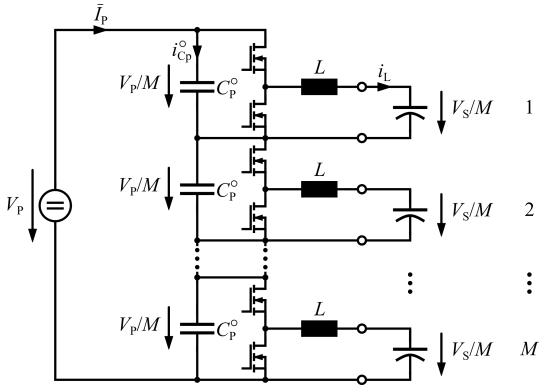


Figure 3: The cascaded synchronous buck converter topology

$1/M$ the cells of the single module version. Even though the current rating is the same, the voltage stress on each half bridge and each inductor is reduced. This way, the inductance can be reduced to $1/M$. By phase shifting the PWM patterns, the ripple voltages of each series input capacitor C_P° partly cancel out. Cascading is also useful in terms of redundancy as if one supercapacitor bank or converter cell fails, it could be bypassed externally. Also, independent control of power from each of the M stacks is possible which would lead to an enhanced management of voltage sharing in case a stack contains aged supercapacitor cells with imbalanced resistance or capacitance.

III. Model of the Operating Waveforms

This section analyzes the current and voltage waveforms in the synchronous buck converter. The converter is idealized, i.e. ohmic resistances and voltage drops across diodes or switches are neglected. This significantly simplifies the equations. After that, the losses are calculated separately. The philosophy of this approach also reflects in simulation software [15].

A. Interleaved Converter

First, the interleaved variant of the converter is analyzed. Each phase is operated with a PWM pattern, where d denotes the duty cycle. Quantities that relate to the individual phases are marked with a superscript circle, whereas quantities that relate to the common output which is connected to the

supercapacitor stack are unmarked. The current waveform in the inductor of each phase, $i_{\mathrm{L}}^{\circ}(t)$, is given in (3).

$$i_{\mathrm{L}}^{\circ}(t) = \begin{cases} \overline{I}_{\mathrm{L}}^{\circ} - \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ} + \frac{V_{\mathrm{P}}-V_{\mathrm{S}}}{L} \cdot t & \text{for } 0 \le t < dT_{\mathrm{sw}} \\ \overline{I}_{\mathrm{L}}^{\circ} + \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ} - \frac{V_{\mathrm{S}}}{L} \cdot (t - dT_{\mathrm{sw}}) & \text{for } dT_{\mathrm{sw}} \le t < T_{\mathrm{sw}} \end{cases} \tag{3}$$

The DC component of the inductor current, $\overline{I}_{\mathrm{L}}^{\circ}$, may be freely adjusted and does not depend on the duty cycle d. The peak-to-peak ripple component of the inductor current, $\Delta I_{\mathrm{pp}}^{\circ}$, is given as follows:

$$\Delta I_{\mathrm{pp}}^{\circ} = \frac{V_{\mathrm{P}} - V_{\mathrm{S}}}{f_{\mathrm{sw}} L} d = \frac{V_{\mathrm{S}}}{f_{\mathrm{sw}} L} (1-d) = \frac{V_{\mathrm{P}}}{f_{\mathrm{sw}} L} d\,(1-d) \tag{4}$$

The following assumptions are made: Steady-state operation is assumed and all N interleaved phases are assumed to share the total output current. For the duty cycle, this implies:

$$d = \frac{V_{\mathrm{S}}}{V_{\mathrm{P}}} = \frac{\overline{I}_{\mathrm{P}}}{\overline{I}_{\mathrm{L}}} = \frac{\overline{I}_{\mathrm{P}}}{N \cdot \overline{I}_{\mathrm{L}}^{\circ}} \tag{5}$$

The inductor current at the switching instants $t = 0$ and $t = dT_{\mathrm{sw}}$ is useful for calculating the switching losses. It is denoted I_{sw}° and given as follows:

$$I_{\mathrm{sw}}^{\circ} = \overline{I}_{\mathrm{L}}^{\circ} \pm \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ} \tag{6}$$

By squaring (3) and integrating, the RMS current in the inductor, I_{L}° and the RMS currents in the high-side and low-side switch, I_{HS}° and I_{LS}°, are derived, which are required for the calculation of conduction losses:

$$I_{\mathrm{L}}^{\circ} = \sqrt{\left(\overline{I}_{\mathrm{L}}^{\circ}\right)^2 + \frac{1}{12}\left(\Delta I_{\mathrm{pp}}^{\circ}\right)^2} \tag{7}$$

$$I_{\mathrm{LS}}^{\circ} = \sqrt{d} \cdot I_{\mathrm{L}}^{\circ}, \quad I_{\mathrm{HS}}^{\circ} = \sqrt{1-d} \cdot I_{\mathrm{L}}^{\circ} \tag{8}$$

In the following, the ripple cancellation effect of interleaving is analyzed. The phase-shift of the PWM patterns results in a lower ripple current of the common output, ΔI_{pp}, compared to the ripple current in the inductors, $\Delta I_{\mathrm{pp}}^{\circ}$. A sample PWM pattern of $N = 3$ interleaved phases at different duty cycles is given in Fig. 4.

The following rules, inspired from [6, 10, 11], are derived:

- The waveforms are periodic with the time period $\frac{T_{\mathrm{sw}}}{N}$
- For a duration of $\frac{T_{\mathrm{sw}}}{N}(Nd - \lfloor Nd \rfloor)$, the output of a number of $(\lfloor Nd \rfloor + 1)$ phases will be V_{P}, while the remaining phases will be zero;
- For the remaining duration $\frac{T_{\mathrm{sw}}}{N}(1 - Nd + \lfloor Nd \rfloor)$, the output of a number of $\lfloor Nd \rfloor$ phases will be V_{P}, while the remaining phases will be zero.

These rules are used for calculating ΔI_{pp} as also presented in [10, 11]:

$$\begin{aligned} \Delta I_{\mathrm{pp}} &= \int_0^{\frac{T_{\mathrm{sw}}}{N}(Nd - \lfloor Nd \rfloor)} \left(\sum_{j=1}^{N} \frac{\mathrm{d}i_{\mathrm{L,j}}^{\circ}(t)}{\mathrm{d}t} \right) \cdot \mathrm{d}t \\ &= \int_0^{\frac{T_{\mathrm{sw}}}{N}(Nd - \lfloor Nd \rfloor)} \frac{(\lfloor Nd \rfloor + 1)\,V_{\mathrm{P}} - N V_{\mathrm{S}}}{L} \cdot \mathrm{d}t \\ &= \frac{V_{\mathrm{P}}}{N f_{\mathrm{sw}} L} (Nd - \lfloor Nd \rfloor)(1 + \lfloor Nd \rfloor - Nd) \end{aligned} \tag{9}$$

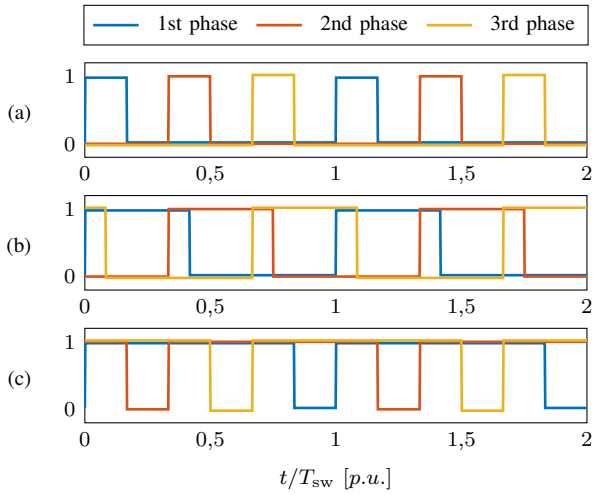


Figure 4: Sample PWM patterns for $N = 3$ interleaved phases. (a) $d = \frac{1}{6}$, (b) $d = \frac{5}{12}$, (c) $d = \frac{5}{6}$.

Similarly, this paper presents the calculation of the ripple of the primary DC bus capacitor charge ΔQ_{P} which is relevant for calculating the resulting DC bus voltage ripple. The current in this capacitor, $i_{\mathrm{C_P}}(t)$, is shown in Fig. 5 for $N = 1 \ldots 2$.

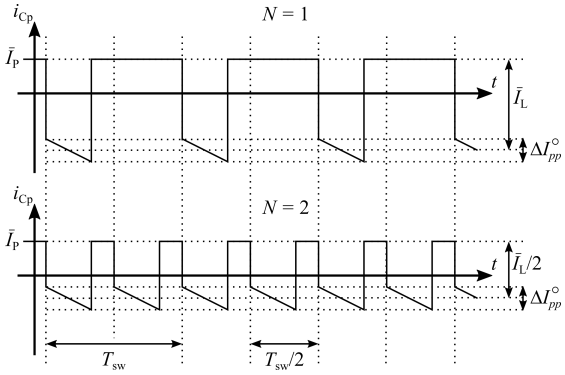


Figure 5: The DC bus capacitor current for different levels of interleaving

The trapezoidal shape of this waveform may be simplified to a square wave with an average current amplitude without any errors in the calculation of the ripple charge ΔQ_{P}. This situation is visualized in Fig. 6.

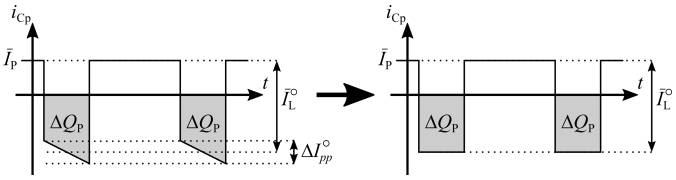


Figure 6: Simplification of the ripple charge calculation

Using the rules for interleaved phases, the capacitor current $i_{\mathrm{C_P}}(t)$ is expressed as given in (10).

$$i_{\mathrm{C_P}}(t) = \begin{cases} \overline{I}_{\mathrm{P}} - \overline{I}_{\mathrm{L}}^{\circ} \cdot (\lfloor Nd \rfloor + 1) \\ \qquad \text{for } 0 \le t < \frac{T_{\mathrm{sw}}}{N}(Nd - \lfloor Nd \rfloor) \\ \overline{I}_{\mathrm{P}} - \overline{I}_{\mathrm{L}}^{\circ} \cdot \lfloor Nd \rfloor \\ \qquad \text{for } \frac{T_{\mathrm{sw}}}{N}(Nd - \lfloor Nd \rfloor) \le t < \frac{T_{\mathrm{sw}}}{N} \end{cases} \tag{10}$$

By integration, the ripple charge ΔQ_P is calculated:

$$\begin{aligned}\Delta Q_\mathrm{P} &= \int_0^{\frac{T_\mathrm{sw}}{N}(Nd-\lfloor Nd\rfloor)} -i_{C_\mathrm{P}}(t)\cdot \mathrm{d}t \\ &= \frac{\overline{I}_\mathrm{P}}{f_\mathrm{sw}N}\left(1-\frac{\lfloor Nd\rfloor}{Nd}\right)(1+\lfloor Nd\rfloor - Nd) \end{aligned} \quad (11)$$

Fig. 7 shows a plot of the cumulated ripple quantities ΔI_pp and ΔQ_P for constant input voltage V_P and current $\overline{I}_\mathrm{P}$. The supercapacitor system has a variable secondary voltage V_S, depending on the number k of series connected cells. Therefore, a range of duty cycles has to be considered as represented by the shaded areas in Fig. 7. The largest ripples in that range of duty cycles need to be identified. Those worst case quantities will determine the required inductance L and capacitance C_P.

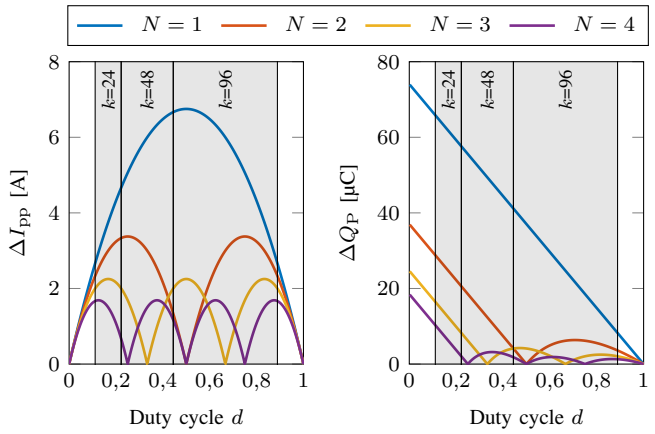


Figure 7: Output ripple current and capacitor ripple charge for $N = 1\ldots4$, $V_\mathrm{P} = 270\,\mathrm{V}$, $\overline{I}_\mathrm{P} = 7.41\,\mathrm{A}$, $L = 100\,\mu\mathrm{H}$, $f_\mathrm{sw} = 100\,\mathrm{kHz}$. Shaded: Range of duty cycles for the three investigated supercapacitor stack configurations.

From the input capacitor ripple charge ΔQ_P, it is possible to calculate the required capacitance for not exceeding a certain voltage deviation ΔV_P from the nominal DC voltage V_P:

$$C_\mathrm{P} = \frac{\Delta Q_\mathrm{P,max}}{\Delta V_\mathrm{P}} \quad (12)$$

For the 270 V DC bus in aircraft, it is the Military Standard 704F that limits the ripple amplitude to $\Delta V_\mathrm{P} \leq 6\,\mathrm{V}$ [13]. Additionally, the peak energy E_{C_P} that the primary capacitor has to carry can be easily calculated:

$$E_{C_\mathrm{P}} = \tfrac{1}{2}C_\mathrm{P}\left(V_\mathrm{P}+\Delta V_\mathrm{P}\right)^2 \quad (13)$$

B. Cascaded Converter

In addition to interleaving, cascading of M converter stages has similar benefits and in order to be able to compare these solutions, its analytical model will also be derived in this paper. The primary voltage is divided across M capacitors. If the capacitance of each individual capacitor is denoted C_P°, the total equivalent primary capacitance C_P is:

$$C_\mathrm{P} = \frac{C_\mathrm{P}^\circ}{M} \quad (14)$$

Cascading does not influence the output current ripple. On the DC bus side however, each half bridge creates a voltage ripple $\Delta V_\mathrm{pp}^\circ$ in each primary capacitor C_P°. By phase-shifting the PWM pulse patterns of the cascaded half bridges, the overall primary ripple voltage ΔV_pp can be reduced. To compare this situation with interleaved operation, an equivalent primary ripple charge ΔQ_P is derived which charges and discharges the equivalent primary capacitance C_P as given in (14):

$$\Delta V_\mathrm{pp} = \frac{\Delta Q_\mathrm{P}}{C_\mathrm{P}} = \int_0^{\frac{T_\mathrm{sw}}{M}(Md-\lfloor Md\rfloor)} \left(\sum_{j=1}^{M}\frac{-i_{C_\mathrm{P}}^\circ(t)}{C_\mathrm{P}^\circ}\right)\cdot \mathrm{d}t \quad (15)$$

Equation (15) is rearranged for the equivalent primary ripple charge ΔQ_P and solved as follows:

$$\begin{aligned}\Delta Q_\mathrm{P} &= \frac{C_\mathrm{P}}{C_\mathrm{P}^\circ}\int_0^{\frac{T_\mathrm{sw}}{M}(Md-\lfloor Md\rfloor)} \left(\sum_{j=1}^{M}-i_{C_\mathrm{P}}^\circ(t)\right)\cdot \mathrm{d}t \\ &= \frac{1}{M}\int_0^{\frac{T_\mathrm{sw}}{M}(Md-\lfloor Md\rfloor)} \left(\overline{I}_\mathrm{L}\left(\lfloor Md\rfloor+1\right)-M\overline{I}_\mathrm{P}\right)\cdot \mathrm{d}t \\ &= \frac{\overline{I}_\mathrm{P}}{f_\mathrm{sw}M}\left(1-\frac{\lfloor Md\rfloor}{Md}\right)(1+\lfloor Md\rfloor - Md) \end{aligned} \quad (16)$$

Comparing (16) with (11), it can be seen these are identical if substituting N by M. If either N converter phases are interleaved or M modules are cascaded, in both cases the same overall size of the DC bus capacitor will be needed. The interleaved topology, however, will result in smaller supercapacitor current ripple or equivalently, smaller inductors.

IV. Loss Model

This section focuses on the modelling of the converter losses. This is critical for power density optimization, as the converter losses have a direct impact on the weight of the cooling system.

A. Semiconductor losses

The semiconductor loss model that will be used is specific to MOSFETs. To calculate the conduction losses in the high-side and low-side device, the RMS currents as well as the on-state resistance R_DS are needed. Furthermore, for reducing conduction losses it might be useful to parallel multiple p MOSFETs to reduce the equivalent on-state resistance. In the high-side and the low-side MOSFETs, respectively, the following conduction losses occur, which are defined in a universal form, as valid for interleaved and cascaded structures:

$$P_\mathrm{cond,HS} = NMp\cdot R_\mathrm{DS}\cdot\left(\frac{I_\mathrm{HS}^\circ}{p}\right)^2 \quad (17)$$

$$P_\mathrm{cond,LS} = NMp\cdot R_\mathrm{DS}\cdot\left(\frac{I_\mathrm{LS}^\circ}{p}\right)^2 \quad (18)$$

As the supercapacitor current $\overline{I}_\mathrm{L}$ is shared by N phases, conduction losses are reduced for interleaving as the device current reduces. The same is achieved when p devices are paralleled as this will reduce its equivalent resistance. On the other hand, if M converter stages are cascaded, the current has to flow through a multiple M devices and the conduction losses will increase.

The power which is required to drive all $2NMp$ MOSFETs is derived using the total gate charge Q_G and the gate-drive voltage V_G:

$$P_\mathrm{G} = 2NMp \cdot f_\mathrm{sw} \cdot Q_\mathrm{G} V_\mathrm{G} \tag{19}$$

Calculating the switching losses is a more complex procedure. The device currents at the switching instants are known from (6). For obtaining the switching energies, there are several approaches [12]. In this work, it is assumed that information on the switching energies are available in the manufacturer's datasheets. The switching energies are given as a function of current and voltage $E_\mathrm{on}\{I, V\}, E_\mathrm{off}\{I, V\}$. Those graphs are digitalized and lookup tables are generated to calculate the losses during the switching transitions.

For the switching losses, three cases have to be distinguished, depending on the DC component of the inductor current $\overline{I}_\mathrm{L}^\circ$. For low DC current or high ripple, ZVS can be achieved, which is used in many designs [5, 7, 16]. The switching losses consist of three components: First, the losses during the actual switching transitions in the low-side and high-side MOSFETs are denoted $P_\mathrm{trans,LS}$ and $P_\mathrm{trans,HS}$. Second, during the dead-time t_d, the antiparallel diodes of the MOSFETs cause dead-time losses $P_\mathrm{dead,LS}$ and $P_\mathrm{dead,HS}$ due to their forward voltage drop V_F. Last, in hard-switching, the antiparallel diodes additionally cause reverse recovery losses $P_\mathrm{rr,LS}$ and $P_\mathrm{rr,HS}$. All of these loss components are summarized in Table I.

B. Losses in passive components

The losses in the inductors are difficult to calculate, as it is not possible to directly derive all geometry variables of an inductor from the given converter variables [17]. Therefore, another approach is chosen.

The so-called area product A_p of an inductor is used, which is defined as the product of core area A_c and winding window area A_w, as it relates to the inductor size. The window area in terms of the copper fill factor k_u, the current density J_max and the maximum RMS current I_L, and the core area depends on the peak flux linkage LI_max and maximum flux density B_max. Based on these, the area product is found [17]:

$$A_\mathrm{p} = A_\mathrm{c} A_\mathrm{w} = \frac{LI_\mathrm{L} I_\mathrm{max}}{k_\mathrm{u} B_\mathrm{max} J_\mathrm{max}} \tag{20}$$

The nominator $LI_\mathrm{L} I_\mathrm{max}$ of (20) only contains data which are available in the datasheets of most inductors. The quantity $LI_\mathrm{L} I_\mathrm{max}$, although having the unit of an energy, relates to the area product A_p. Therefore, data of inductors manufactured by several companies specialized in magnetics for switched-mode converters have been researched. As large inductors are capable of dissipating higher losses than small inductors, the correlation of the inductor losses P_L that result in a 40 K temperature rise with the quantity $LI_\mathrm{L} I_\mathrm{max}$ can be used to estimate the losses. In Fig. 8, a function to enable the loss estimation is derived.

If the maximum inductor temperature is denoted $\hat{T}_\mathrm{L}$ and the ambient T_amb, the losses of the inductors may be obtained via curve fitting as depicted by the red curve in Fig. 8. The temperature rise is scaled linearly:

$$P_\mathrm{L} \approx MN \cdot \frac{\hat{T}_\mathrm{L} - T_\mathrm{amb}}{40\,\mathrm{K}} \cdot 7.88 \,\frac{\mathrm{W}}{\mathrm{J}^{0.25}} \left(LI_\mathrm{L}^\circ \left(\left| \overline{I}_\mathrm{L}^\circ \right| + \tfrac{1}{2} \Delta I_\mathrm{pp}^\circ \right) \right)^{0.25} \tag{21}$$

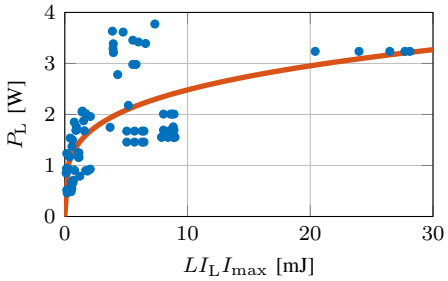


Figure 8: Inductor losses as a function of the area-product related quantity $LI_\mathrm{L} I_\mathrm{max}$. Manufacturer data and curve fit

One downside of this approach is that high-frequency loss components, such as skin and proximity effect related losses, as well as iron losses are not included. The skin and the proximity effect are not easily accessible analytically [17, 18].

The losses in the DC bus capacitor are assumed to be negligibly small. However, if those losses are to be considered, the RMS current in the DC bus capacitor $I_{\mathrm{C_P}}$ as presented in [6, 10] is needed. For the desired capacitor technology, the dissipation factor $\tan\delta$ may be researched to obtain the equivalent series resistance. Using the RMS current and the equivalent series resistance, the losses can be calculated.

V. Weight Model

This section attempts to calculate the weights of the converter components. For the losses, which influence the weight of the cooling system, the approach of [12] is chosen: Literature [19] states that for a cooling system, the thermal resistance R_th and the weight m_th of a heatsink are linked to a material constant, the thermal figure of merit FOM_th:

$$FOM_\mathrm{th} = \frac{1}{R_\mathrm{th} \cdot m_\mathrm{th}} = \text{const.} \tag{22}$$

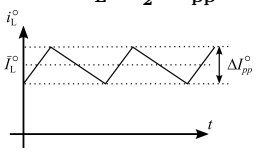
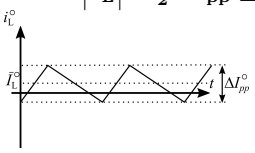
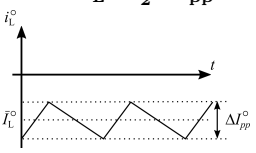
Attempting to optimize the geometry of a heatsink and a fan for minimum weight is a complex procedure which is given in [20, 21]. From the results, it is derived that a thermal figure of merit of $FOM_\mathrm{th} = 15\,\frac{\mathrm{W}}{\mathrm{kg\,K}}$ is a reasonable choice for aluminum.

The inductor weight is found by analyzing its correlation with the area product A_p, using the already collected inductor data. In Fig. 9, the weight m_L is plotted as a function of the area-product related quantity $LI_\mathrm{L} I_\mathrm{max}$. It is found that a linear relationship between $LI_\mathrm{L} I_\mathrm{max}$ and the weight can be assumed:

$$m_\mathrm{L} \approx MN \cdot 4.96\,\frac{\mathrm{kg}}{\mathrm{J}} \cdot \left(LI_\mathrm{L}^\circ \left(\left| \overline{I}_\mathrm{L}^\circ \right| + \tfrac{1}{2} \Delta I_\mathrm{pp}^\circ \right) \right) \tag{23}$$

Finally, for capacitors, the energy density is the central criterion to account for the weight [12, 22]. For ceramic capacitors, an energy density of $41\,\frac{\mathrm{J}}{\mathrm{kg}}$ is assumed [12]. Equation (13) should be used to calculate the capacitor energy.

Table I: Analytical model of the switching loss components, depending on the level of DC current $\overline{I}_{\mathrm{L}}^{\circ}$

	Case 1: $\overline{I}_{\mathrm{L}}^{\circ} - \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ} > 0$	**Case 2: $\left\lvert\overline{I}_{\mathrm{L}}^{\circ}\right\rvert - \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ} \leq 0$**	**Case 3: $\overline{I}_{\mathrm{L}}^{\circ} + \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ} < 0$**
			
High side Low side	Hard switching Synchronous rectification	ZVS ZVS	Synchronous rectification Hard switching
$P_{\mathrm{trans,HS}}$	$NMp \cdot f_{\mathrm{sw}} \cdot \left(E_{\mathrm{on}}\left\{ \frac{I_{\mathrm{L}}^{\circ} - \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}}{p}; \frac{V_{\mathrm{P}}}{M} \right\} \ldots + E_{\mathrm{off}}\left\{ \frac{I_{\mathrm{L}}^{\circ} + \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}}{p}; \frac{V_{\mathrm{P}}}{M} \right\} \right)$	$NMp \cdot f_{\mathrm{sw}} \cdot E_{\mathrm{off}}\left\{ \frac{I_{\mathrm{L}}^{\circ} + \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}}{p}; \frac{V_{\mathrm{P}}}{M} \right\}$	0
$P_{\mathrm{trans,LS}}$	0	$NMp \cdot f_{\mathrm{sw}} \cdot E_{\mathrm{off}}\left\{ \frac{\left\lvert I_{\mathrm{L}}^{\circ} - \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}\right\rvert}{p}; \frac{V_{\mathrm{P}}}{M} \right\}$	$NMp \cdot f_{\mathrm{sw}} \cdot \left(E_{\mathrm{off}}\left\{ \frac{\left\lvert I_{\mathrm{L}}^{\circ} - \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}\right\rvert}{p}; \frac{V_{\mathrm{P}}}{M} \right\} \ldots + E_{\mathrm{on}}\left\{ \frac{\left\lvert I_{\mathrm{L}}^{\circ} + \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}\right\rvert}{p}; \frac{V_{\mathrm{P}}}{M} \right\} \right)$
$P_{\mathrm{dead,HS}}$	0	$NM \cdot f_{\mathrm{sw}} t_{\mathrm{d}} \cdot V_{\mathrm{F}}\left\lvert I_{\mathrm{L}}^{\circ} - \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}\right\rvert$	$NM \cdot f_{\mathrm{sw}} t_{\mathrm{d}} \cdot \left(V_{\mathrm{F}}\left\lvert I_{\mathrm{L}}^{\circ} - \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}\right\rvert + V_{\mathrm{F}}\left\lvert I_{\mathrm{L}}^{\circ} + \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}\right\rvert \right)$
$P_{\mathrm{dead,LS}}$	$NM \cdot f_{\mathrm{sw}} t_{\mathrm{d}} \cdot \left(V_{\mathrm{F}}\left(I_{\mathrm{L}}^{\circ} - \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}\right) + V_{\mathrm{F}}\left(I_{\mathrm{L}}^{\circ} + \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}\right) \right)$	$NM \cdot f_{\mathrm{sw}} t_{\mathrm{d}} \cdot V_{\mathrm{F}}\left(I_{\mathrm{L}}^{\circ} + \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}\right)$	0
$P_{\mathrm{rr,HS}}$	0	0	$NMp \cdot f_{\mathrm{sw}} \cdot \left(\frac{1}{2} \cdot \frac{V_{\mathrm{P}}}{M} \cdot Q_{\mathrm{rr}}\left\{ \frac{\left\lvert I_{\mathrm{L}}^{\circ} + \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}\right\rvert}{p} \right\} \right)$
$P_{\mathrm{rr,LS}}$	$NMp \cdot f_{\mathrm{sw}} \cdot \left(\frac{1}{2} \cdot \frac{V_{\mathrm{P}}}{M} \cdot Q_{\mathrm{rr}}\left\{ \frac{I_{\mathrm{L}}^{\circ} - \frac{1}{2}\Delta I_{\mathrm{pp}}^{\circ}}{p} \right\} \right)$	0	0

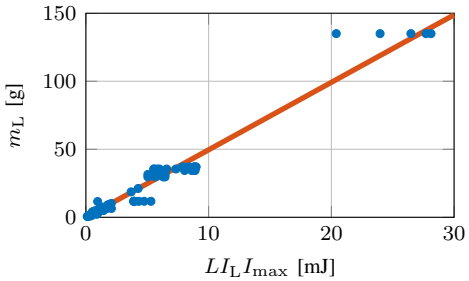


Figure 9: Inductor weight as a function of the area-product related quantity $LI_{\mathrm{L}}I_{\mathrm{max}}$. Manufacturer data and curve fit

In addition to the weights of these components which depend on design choices, a constant part to account for the power stage, PCB, driver circuitry, sensors, screws and connectors is assumed. These components are listed in Table II.

Table II: List of converter hardware components and their weight

Component	Weight each	Quantity needed
PCB material (FR4, 4 layers)	6 $\frac{\mathrm{kg}}{\mathrm{m}^2}$	160 mm x 100 mm
Gate driver circuitry	2.50 g	$2 \cdot M \cdot N$
Current sensors	7.50 g	M
Voltage sensors	2.50 g	$M + 1$
Mounting material	20 g	1

VI. Optimization Algorithm

In order to find a good initial design for the projected synchronous buck converter for the aircraft supercapacitor system, the analytical models presented in the previous sections are implemented in a MATLAB design algorithm. The parameters to this design procedure are shown in Table III. The goal is to obtain graphs of power density as a function of switching frequency for each of the preselected semiconductor

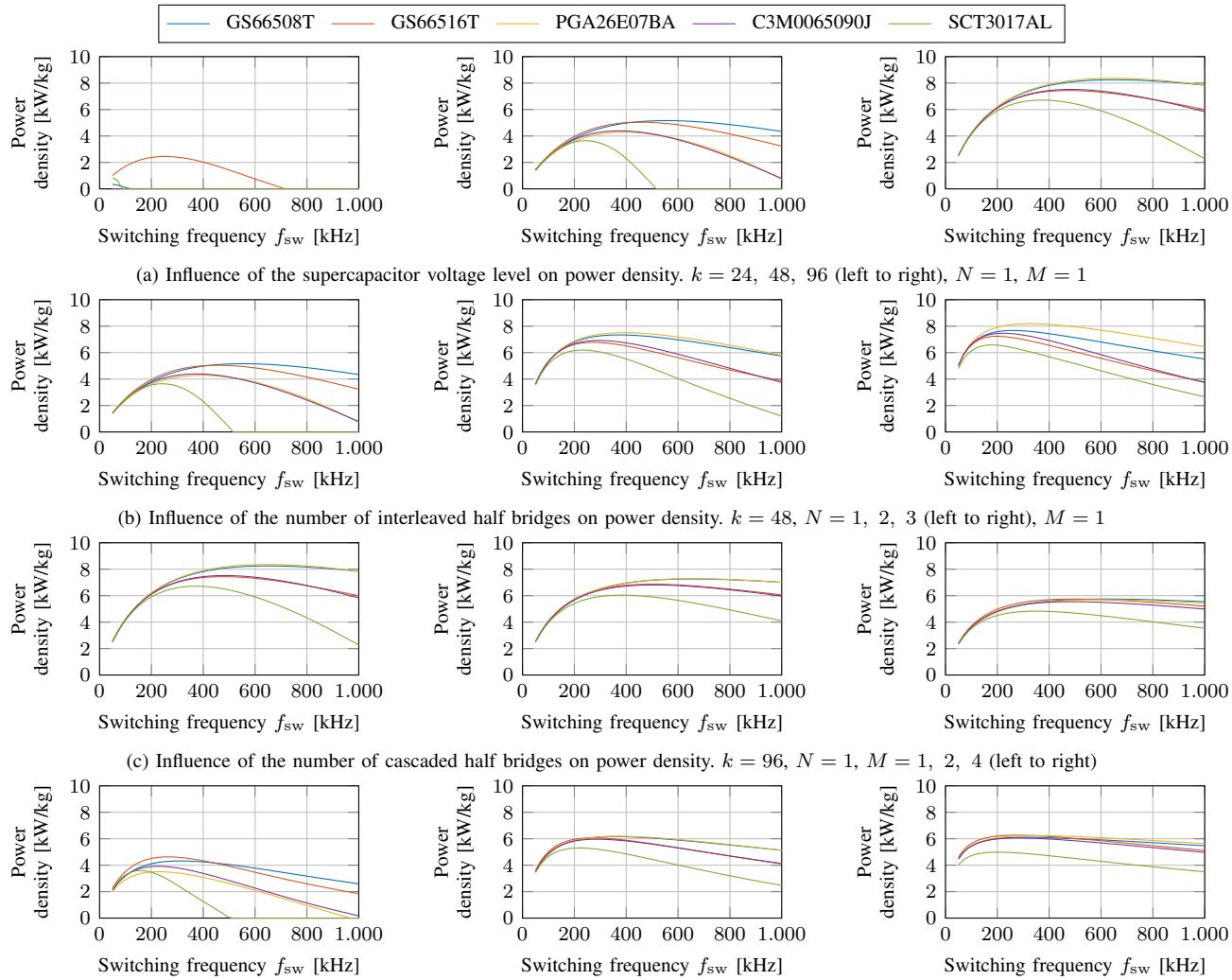
Table III: Simulation parameters of the proposed design algorithm

Parameter	Typical value
Rated input voltage	$V_{\mathrm{P}} = 270\,\mathrm{V}$
Rated power	$P = 2\,\mathrm{kW}$
Number of series-connected supercapacitor cells	$k \in \{32,\ 64,\ 96\}$
Simulation at different SOC	$V_{\mathrm{S}} \in \left[\frac{1}{2}kV_{\mathrm{cell}},\ kV_{\mathrm{cell}}\right]$
Range of switching frequency	$f_{\mathrm{sw}} \in [50\,\mathrm{kHz},\ 1\,\mathrm{MHz}]$
DC bus ripple voltage amplitude	$\Delta V_{\mathrm{P}} = 4\,\mathrm{V}$
Supercapacitor ripple current	$\Delta I_{\mathrm{pp}} = 10\,\% \cdot \frac{P}{\frac{1}{2}kV_{\mathrm{cell}}}$
Ambient temperature	$T_{\mathrm{amb}} = 30\,^{\circ}\mathrm{C}$
Thermal FOM	$FOM_{\mathrm{th}} = 15\ \frac{\mathrm{W}}{\mathrm{kg\,K}}$
Semiconductor devices	GaN Systems GS66508T, GaN Systems GS66516T, Panasonic PGA26E07BA, Wolfspeed C3M0065090J, Rohm SCT3017AL
Maximum inductor temperature	$\hat{T}_{\mathrm{L}} = 100\,^{\circ}\mathrm{C}$
Capacitor energy density	$w_{\mathrm{C_P}} = 41.3\ \frac{\mathrm{J}}{\mathrm{kg}}$
Number of interleaved half bridges	$N \in \{1,\ 2,\ 3\}$
Number of cascaded half bridges	$M \in \{1,\ 2,\ 3\}$
Range of inductance	$L \in [L_{\mathrm{min}},\ 5 \cdot L_{\mathrm{min}}]$

devices, primarily SiC and GaN power MOSFETs, mentioned in Table III. Therefore, the algorithm is organized as follows:

The design inputs are the supercapacitor voltage level k, the number of interleaved half bridges N and the number of cascaded half bridges M. All semiconductor devices are simulated on the whole range of switching frequencies to generate the power density plots as shown in Fig. 10. For each plot, the following procedure is carried out:

For a given semiconductor device and a given switching frequency, the maximum ripple charge is calculated to determine the required primary capacitance C_{P}, taking into account all possible voltages V_{S} of the supercapacitor system. Then, the required inductance L_{min} is calculated based on (9), which guarantees the ripple current ΔI_{pp} to stay below the desired



(a) Influence of the supercapacitor voltage level on power density. $k = 24,\ 48,\ 96$ (left to right), $N = 1$, $M = 1$

(b) Influence of the number of interleaved half bridges on power density. $k = 48$, $N = 1,\ 2,\ 3$ (left to right), $M = 1$

(c) Influence of the number of cascaded half bridges on power density. $k = 96$, $N = 1$, $M = 1,\ 2,\ 4$ (left to right)

(d) Effect of splitting and stacking low-voltage supercapacitor banks. $k = 24,\ 48,\ 96$ (left to right), $N = 2$, $M = 1,\ 2,\ 4$ (left to right)

Figure 10: Results of the optimization algorithm. Plots of power density as function of switching frequency for different power semiconductor devices.

value for all possible supercapacitor voltages V_S. Also higher inductances up to $5 \cdot L_{min}$ are simulated.

Additionally, different numbers of paralleled MOSFETs p are simulated. The minimum and maximum number p is individual for each MOSFET. In this study, a maximum number of 2 paralleled devices is assumed for SMD packages and 1 for bulky leaded packages.

This process is carried out for all possible secondary voltages V_S that correspond to the supercapacitor being fully discharged ($V_{cell} = 1.25\,V$) to fully charged ($V_{cell} = 2.50\,V$), for both positive and negative power flow and the lowest value of the power density is saved. This implies that power density is defined when processing the rated power (2 kW) at the most unfavourable operating condition (most likely when the supercapacitor is fully discharged).

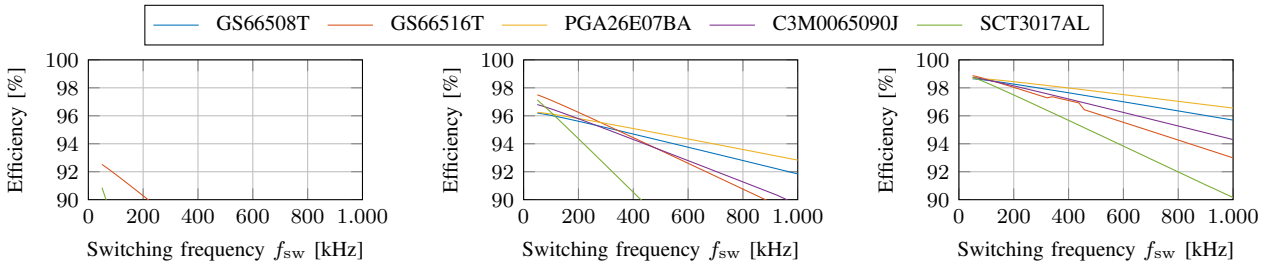
The parameters L and p, however, are selected to maximize the power density for a given switching frequency and semiconductor device. After simulating all combinations of switching frequencies and semiconductor devices, the results, such as power density and efficiency graphs, can be plotted.

VII. Results

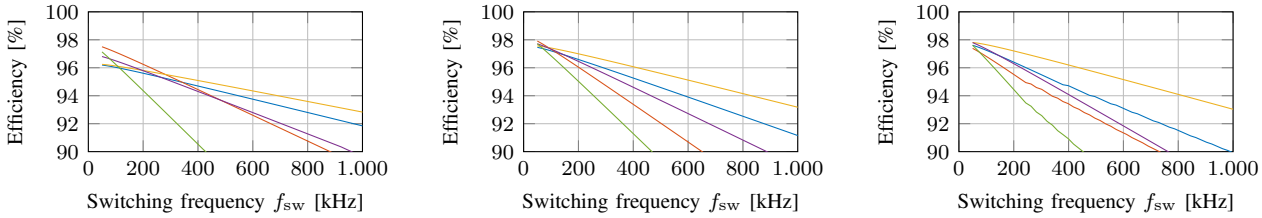
In Fig. 10 and Fig. 11, the results from running the design algorithm for the energy storage system specified in section II are presented. Fig. 10 presents the power density graphs and Fig. 11 the respective efficiency profiles. Due to using analytical modelling rather than detailed simulations in time domain, the computation time is significantly shorter. Generating one of the plots requires less than 3 minutes in MATLAB.

First, the influence of the supercapacitor voltage level is analyzed in Fig. 10a and Fig. 11a. The number of series-connected supercapacitor cells k is varied from 24 to 96 as introduced in section II. Interleaving and cascading is not regarded. It is clearly visible that higher supercapacitor voltage yields higher power density. This is obviously due to the fact that the current is reduced as voltage increases and therefore, conduction losses decrease. This reflects in the significant increase of the efficiency as seen in Fig. 11a.

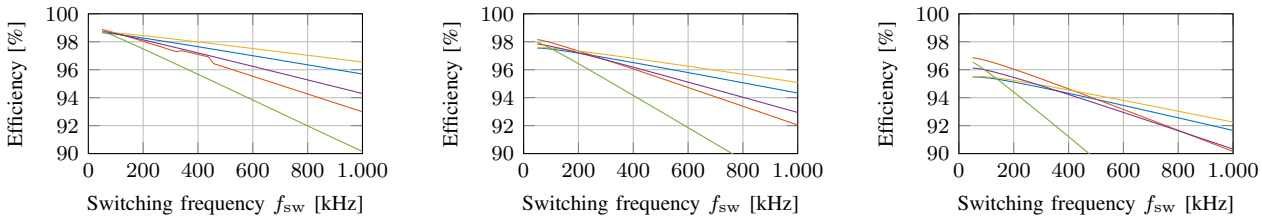
In Fig. 10a, it is observed that for the lowest voltage configuration ($k = 24$), most of the power density graphs are zero. In this case, the losses in the semiconductor devices,



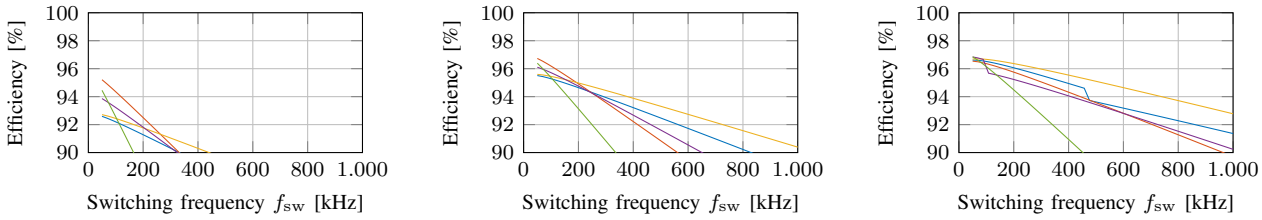
(a) Influence of the supercapacitor voltage level on efficiency. $k = 24,\ 48,\ 96$ (left to right), $N = 1$, $M = 1$



(b) Influence of the number of interleaved half bridges on efficiency. $k = 48$, $N = 1,\ 2,\ 3$ (left to right), $M = 1$



(c) Influence of the number of cascaded half bridges on efficiency. $k = 96$, $N = 1$, $M = 1,\ 2,\ 4$ (left to right)



(d) Effect of splitting and stacking low-voltage supercapacitor banks. $k = 24,\ 48,\ 96$ (left to right), $N = 2$, $M = 1,\ 2,\ 4$ (left to right)

Figure 11: Results of the optimization algorithm. Plots of efficiency as function of switching frequency for different power semiconductor devices.

multiplied with the junction-to-case thermal resistance, exceed the maximum allowable temperature rise from the ambient to the maximum junction temperature resulting in an infinite size of the heatsink. This demonstrates that in a low-voltage design, conduction losses are prohibitive.

The benefit of using interleaving can be analyzed at the medium voltage level ($k = 48$) as illustrated in Fig. 10b and Fig. 11b. The number of interleaved half bridges is increased from $N = 1$ to $N = 3$. It can be seen that the power density significantly increases as N increases, whereas the efficiency profiles only increase moderately. As the inductor ripple current $\Delta I^{\circ}_{\mathrm{pp}}$ can be significantly increased compared to the output current ripple ΔI_{pp} for $N > 1$, much weight is saved due to smaller inductors. The increase in efficiency, however, results from the fact that the current is shared between more semiconductors, which is beneficial for conduction losses.

Another interesting observation from Fig. 10b is that the peaks of the power density graphs move toward lower switching frequencies as N increases. This is due to the higher effective switching frequency in interleaved operation, see (2): As the effective frequency $f_{\mathrm{sw,eff}}$ of the output current ripple increases, the frequency f_{sw} of the individual phases can be reduced and hence, they operate more efficiently.

The effect of using cascaded cells is analyzed at the highest voltage level $k = 96$ in Fig. 10c and Fig. 11c. Cascading is analyzed for $M = 1,\ 2,\ 4$. For example, as $k = 96$ and $M = 4$, the system consists of 4 series-connected converter cells, each connected to a supercapacitor system working in the range of $V_{\mathrm{S}} = 30 \ldots 60\,\mathrm{V}$. As it was already suspected from equations (17) and (18), the power density decreases with increasing level of cascading. The supercapacitor current flows through more semiconductor devices and therefore, the conduction losses increase as it can be seen in Fig. 11c.

However, having multiple cascaded supercapacitor stacks may be beneficial in terms of redundancy, as already discussed. If a modular design of a supercapacitor bank of the lowest voltage level ($k = 24,\ V_{\mathrm{S}} = 30 \ldots 60\,\mathrm{V}$) is considered, it is interesting to investigate how the power density changes if more of these modules, e.g. two ($k = 48,\ M = 2$) or four ($k = 96,\ M = 4$), are connected in series. Additional

interleaving of $N = 2$ is considered. The results are shown in Fig. 10d and Fig. 11d. It can be seen that stacking modules helps to increase power density. In Fig. 11d on the right, abrupt changes in the efficiency profiles can be observed. This is a result from the automatic selection of the number of paralleled devices p. At these points, using less paralleled devices, thus saving the weight of the semiconductors, levels out with the increased cooling effort due to higher losses.

Naturally, more details on the losses and the weight of a specific design may be obtained from the algorithm. As an example, the design with the Panasonic GaN MOSFET PGA26E07BA at 400 kHz, $k = 48$, $N = 2$, $M = 1$ is chosen. This corresponds to the peak power density of Fig. 10b (middle). In Fig. 12, the weight and the loss breakdown are presented. The design reaches a power density of 7.51 $\frac{\text{kW}}{\text{kg}}$, which corresponds to a weight of 266 g. The total losses are 79 W, which corresponds to an efficiency of 96.1 %. Because of interleaving, the ripple current which flows into the supercapacitor is $\Delta I_{\text{pp}} = 6.67\,\text{A}$, while the ripple current in each inductor can be increased to $\Delta I_{\text{pp}}^{\circ} = 13.2\,\text{A}$. Two inductors of 12.7 µH each are needed.

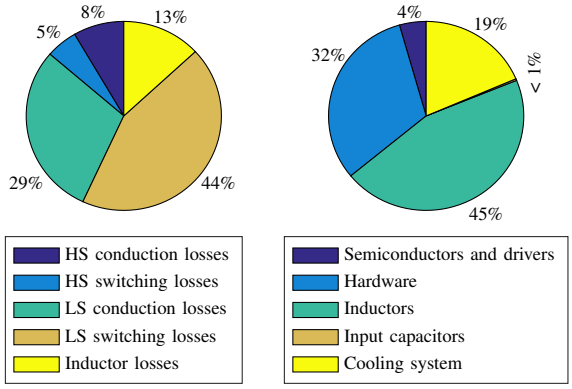


Figure 12: Left: Loss breakdown of the example design (79 W total losses, 96.1 % efficiency). Right: Weight breakdown (total 266 g, 7.51 $\frac{\text{kW}}{\text{kg}}$)

This design methodology can be further developed to implement a multidimensional optimization algorithm which sometimes exhibits contradicting effects such as lowering weight and maximising efficiency. If, in the example design, the switching frequency is reduced from 400 kHz to 200 kHz, it can be seen from Fig. 10b that the power density will decrease by 8 % (from 7.51 $\frac{\text{kW}}{\text{kg}}$ to 6.91 $\frac{\text{kW}}{\text{kg}}$). However, the converter efficiency improves by 1 % according to Fig. 11b. This improves the roundtrip efficiency of the energy storage system by 2 %, reducing fuel consumption by more than the added converter weight.

VIII. Conclusion

In this paper, a design procedure for a synchronous buck converter for an aircraft supercapacitor system is presented, which enables the maximization of power denstiy. Two topology variants of the converter that have the capability to increase power density and redundancy, essential in aircaft applications, are considered, namely interleaving and cascading. The proposed design procedure is based on fully analytical modelling of the electrical converter parameters, the losses and the weights of the converter components. This allows to implement this design algorithm very computationally efficient in MATLAB. The generated power density graphs are a useful basis for shortlisting the best converter design configurations.

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