Wide Bandgap Voltage Source Inverter Design for Automotive Electric Drivetrain

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***Abstract*—In this paper a high power, high frequency voltage source inverter for automotive traction application is reviewed. The main objectives of the design process is the maximization of power density, while keeping high efficiency and low weight. In this paper, the focus is placed on the peculiarities that differentiate this design from other ordinary machine drive. In particular several areas are explored, all equally important for the achievement of design goals. Starting from device choice to gate driving and current sensing circuits design.**

I. Introduction

Electrification of the transportation sector has been steadily increasing, both in terms of market presence, with hybrid and plug-in electric cars, and in terms of research, with an ever increasing interest in this topic. For electrical machines, the general trend is the increase in mechanical speed [1], [2], with designs currently on the market routinely above $10,000$ to $15,000$ rpm, while in the research space designs with even higher speeds are studied, as in [3]. This can be explained by the higher power density that high speed machines can achieve, a critical parameter in weight and volume constrained applications such as vehicular ones. This increase, coupled with the relatively high pole counts found in automotive traction machines leads to high fundamental frequencies, that can easily end up above 1 kHz. This can lead to a reduction in the ratio between switching and fundamental frequency,if no corrective steps are taken. It is thus very important to properly counteract this undesired effect, so as to not harm dynamic performances of the system and significantly increase current harmonics on the electrical machine, leading to higher losses and lower efficiency. Consequently the switching frequency of the motor's drive has to increase accordingly. Moreover other benefits can make higher switching frequencies desirable: keeping constant the nominal converter power rating, passive components size will be greatly reduced, improving even further the power density of the powertrain as a whole. An increased switching frequency has however also few disadvantages, in particular a big impact of the physical layout, through parasitic components, on several key performance metrics, and in particular overall dynamics and losses. In the first case the only valid countermeasure is a minimization of the parasitic components themselves, and in particular any unwanted loop inductance should be minimized, as they are the main offender both in terms of both signal integrity degradation, and electromagnetic emission problems. A possible solution that allows a definite increase in switching frequency is the use of wide bandgap devices, their higher breakdown strenght allows a reduction in die area while keeping constant the on state resistance The second problem can be avoided by using wide bandgap based devices, resulting in lower capacitance lowering losses at high frequencies [4], [5].

After having listed this design's specifications in section II, we will explain how power devices have been selected in section III, the choice and sizing of several important components and circuits will then be analyzed and in particular, we will talk about the gate driver in section IV and the current sensing circuit in section V.

II. Specifications and Requirements

The input system specifications are the following:

- **Input voltage:** 600 V_{DC}
- **Output power:** 80 kVA
- **Switching frequency:** 120 kHz
- **Nominal output current:** 180 A

The highest practical system voltage of 600 V has been specified in order to minimize resistive losses in the entire system, this is accordance with an industry wide trend of ever increasing system voltages in electric veichles [6], [7]. As already stated in the introduction a high switching frequency is needed to support high speed and high pole count motors, along with a considerable reduction in passive components size and weight.The minimum inductive power factor at which the nominal power can be transfered to the load is 0.85, and can be found by considering Equation (1), where P_{MAX} is the maximum output power, V_{DC} is the DC bus voltage, I_{MAX} is the maximum output current and k is constant and depending on the type of modulation can be either, $1/2$ for sinusoidal PWM (SPWM), or $1/\sqrt{3}$ for third harmonic injected PWM (THIPWM) and space vector modulation (SVPWM).

$$cos(\varphi) > \frac{2P_{MAX}}{3V_{DC}kI_{MAX}} \tag{1}$$

Due to peculiarities of the automotive field which is the main target of this design great emphasis is placed on the

maximization of power density, a low weight is also desired to achieve better vehicle performances and range.

III. Power devices Selection

The first big trade-off when it comes to the power section is a choice between module or paralleled discrete transistors based solutions. At first glance the module based approach seems much more convenient due to simpler power circuit and thermal designs, however, as opposed to the traditional silicon market, the wide bandgap devices space is much less mature and only few players in this field offer complete modules with a high enough power handling capability, this leads to undesirable side effects like higher prices and long lead times, this makes the use of integrated modules impossible in this context. Another important distinction is between through hole ande surface mount technologies, the first while making thermal design much easier, presents much higher parassitic inductances. A clear example of this are Wolfspeed's C3M0065090D and C3M0065090J devices, the same die is packaged in both a surface mount(TO263-7) and a through hole (TO247-3) package, by comparing the manifacturer provided SPICE models, the second component has inductances that can be as much as 10 times lower, due to shorter leads and in case of the source, multiple paralleled connections. The great impact of the single device characteristics on the performances of the whole design, means that the right device choice is necessary to reach the aforementioned goals. Thus a number of performance indices have been analytically evaluated for various Silicon Carbide MOSFET models listed below:

- C2M0040120D by wolfspeed
- C3M0065090D by wolfspeed
- SCT3030KL by rhom
- SCT3040KL by rhom
- SCT3080KL by rhom
- APT80SM120S by microsemi

A. Conduction losses

The instantaneous steady state conduction loss for a power MOSFET can be calculated with Equation (2) and (Equation (3)), by multiplying this expression by the duty cycle for the Sinusoidal PWM modulation, and then integrating over a period of the fundamental synthesized waveform, as also done in [8], the Equation (3a) and Equation (3b) describing mean power losses on upper and lower switching elements are found. When using MOSFET type devices the average power loss in a leg is independent from the modulation index (m), when neglecting higher order effects. This can also be shown by observing the two previously obtained equations, the first two terms are respectively a pure number and an expression not dependent on m while the third member of each equation can be summed to the result of $\pi/2$. thusly the conduction power losses for each half bridge section can be expressed with Equation (4); where P_C and $\overline{P}_C$ are the instantaneous and average conduction losses, $R_{DS(on),D}$ is the single device on state resistance, m is the modulation index and φ is the phase angle

$$P_C = R_{DS(on)} i^2 \tag{2}$$

$$\overline{P}_{C(HS)} = \left(\frac{2}{\pi} R_{DS(on),D} \frac{I_{OUT}}{\sqrt{2}}\right)^2 \left(\frac{1}{6} m(cos(2\varphi) + 3) + \frac{\pi}{4}\right) \tag{3a}$$

$$\overline{P}_{C(LS)} = \left(\frac{2}{\pi} R_{DS(on),D} \frac{I_{OUT}}{\sqrt{2}}\right)^2 \left(\frac{\pi}{4} - \frac{1}{6} m(cos(2\varphi) + 3)\right) \tag{3b}$$

$$\overline{P}_C = \frac{\pi}{2} \left(\frac{2}{\pi} R_{DS(on),D} \frac{I_{OUT}}{\sqrt{2}}\right)^2 \tag{4}$$

B. Switching losses

Due to the great dependence of the switching losses form the internal structure of each device, along with many other unknown parameters peculiar to the manufacturing process in use at each factory, it is not possible to evaluate analytically the switching losses, and either experimental or manufacturer supplied data must be used. In this paper the analysis is based on the performance provided in the datasheet of the different devices taken into account, in the form of turn on (E_{ON}) and turn off (E_{OFF}) energies, these figures incorporate both the losses due to the crossing of the transistor saturation regions and the diode's reverse recovery losses. Since the losses figures on the datasheets are stated at generally different operating points, linear interpolation has been used to estimate losses at the relevant operating point. Equation (5) is used to evaluate steady state switching losses for each device; where V_{TEST} and I_{TEST} are the voltage and current at which the energies have been measured, V_{op} and I_{op} are the operating voltage and current and f_{sw} is the switching frequency.

$$\overline{P}_{SW(ON)} = E_{ON} \frac{V_{op}}{V_{TEST}} \frac{I_{op}}{I_{TEST}} f_{sw} \tag{5a}$$

$$\overline{P}_{SW(OFF)} = E_{OFF} \frac{V_{op}}{V_{TEST}} \frac{I_{op}}{I_{TEST}} f_{sw} \tag{5b}$$

$$\overline{P}_{SW} = \overline{P}_{SW(ON)} + \overline{P}_{SW(OFF)} \tag{6}$$

IV. Thermal Design

The sizing and design of the cooling system is of paramount importance to both performances and lifetime of the devices, this aspect of the design is even more important in the automotive field where high power density and weight reduction requirements push towards the minimization of heatsinks and heat exchangers. A realistic estimation of the steady state power losses of the whole drive is therefore critical. The evaluation of conduction losses contribute as shown in Equation (7) is carried out multiplying **??** by 3, the number of legs in the bridge, and by the number of devices n used in each parallel, whose on state resistance is ($R_{DS(on),C}$).

$$\overline{P}_{C(drive)} = 3n\overline{P}_C = \frac{3}{2} n\pi (\frac{2}{\pi} R_{DS(on),C} \frac{I_{OUT}}{\sqrt{2}})^2 \tag{7}$$

Before calculating the average switching power loss for the drive, it should be noted that load current is presumed constant due to the load inductance. If the previous assumption holds during the dead time added to avoid cross conduction, one of the anti-parallel diodes will be turned on by the load's current and it will remain on until the complementary device has been

switched on. Due to this effect the turn on is a ZCS (zero current switching) transition and will incur in no losses. The average switching loss can be now calculated as shown in the following equation.

$$\overline{P}_{SW(drive)} = 3n\overline{P}_{SW} \tag{8}$$

Finally equations for the total average drive losses, and average per device losses, can be found in Equation (9) and Equation (10). The results for the final drive design can be found in table Table I.

Figure of merit	Value [W]
Drive Power loss	1050
Single device power loss	50

TABLE I: Final drive design average power losses at maximum power output

Several methods have been successfully employed over the years for cooling power electronics, in particular we can go from the cheapest and usually least capable natural and forced convection, to closed loop liquid coolers and finally, the most performant in terms of heat extraction, immersion cooling. The first method, natural convection, can be excluded since the amount of power to dissipate is too high and would result in impractically large heat-sinks; forced convection, in automotive applications, is quickly discarded due to its difficult system level integration, requiring specific ducting and bodyworks to guide air, to the heat exchanger, from the outside. Of the two remaining methods the most suited is by far is closed loop liquid cooling, among it's advantages are the lower weight, lower volume and compatibility with currently used design and manufacturing techniques.

$$\overline{P}_{drive} = \overline{P}_{SW(drive)} + \overline{P}_{C(drive)} \tag{9}$$

$$\overline{P}_{device} = \frac{\overline{P}_{drive}}{3n} \tag{10}$$

V. Gate Driver

Careful study of the gate driving circuit is required as the switching frequency increases due to two separate effects, the first is an increase in the average current that needs to be supplied by the driver's circuit since the number of times the gate capacitance has to be charged and discharged each second grows. The second effect is an increase in the peak current that the gate has to push/pull to/from the gate in order to make the device switch with the desired speed, that must be increased to both reduce switching losses and also achieve enough on time at high duty cycles.

The first major trade-off in the design process is the choice between an isolated and a non isolated gate driver, while the first one can simplify the design of the safety isolation system and also helps to decouple logic and power section, it requires the addition of several isolated power supplies for the high side devices' drivers, and can also lead to signal integrity problems at high switching frequencies if the isolator's CMTI (common mode transient immunity) is not high enough. To avoid these problems a non isolated approach has been used, it's advantages are his low cost and the immunity from signal integrity problems due to common mode noise and different ground voltages between logic and power side of the isolator.

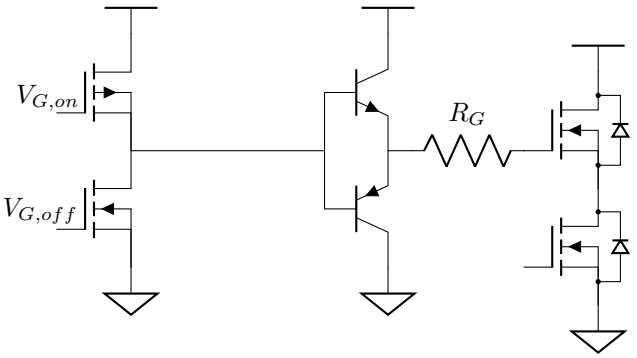

Fig. 1: Current boosted gate driver

The this choice effectively determines which type of power supply circuit to use for the high side devices, a bootstrapped gate driver is in fact the only topology that can be used without multiple insulated supplies.The C_{BOOT} capacitor is used to approximate a voltage source, that supplies the whole gate driving circuit, the charge on the capacitor has to be refreshed periodically. This can be done though D_{BOOT} when the output node is at ground potential. The minimum capacitance needed to avoid excessive voltage drop during high duty cycles can be calculated with Equation (11), where Q_{TOTAL} is the total charge that has to be provided from the capacitor, that is to say the sum of the overall gate capacitance Q_{GATE} and a charge originating from leakage and quiescent currents during the on time, and ΔV_{BOOT} is the maximum allowable voltage drop in a fwitching period.

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}} = \frac{Q_{GATE} + (I_{leak} + I_q) \cdot max(t_{on})}{\Delta V_{BOOT}} \tag{11}$$

The choice of bootstrapped gate driver power supply topology effectively also force the use of a unipolar gate waveform, the main drawback of this drive method, particularly at high speeds, is the potential vulnerability to dv/dt induced turn-on, to counteract this phenomenon, active miller clamping is used.

To switch the cluster of parallel transistors within the desired switching time of 15ns,a peak current of 14.2A has to be sourced or sinked by the gate driver at each switching event, as in Equation (12), after a brief market analysis it has been concluded that no currently available integrated gate driver can support such high currents, so a bipolar current boosting stage, as shown in figure 1 is used.

$$I_{Gon/off} = \frac{nQ_G}{t_{raise/fall}} \tag{12}$$

VI. Current Sensing

Another challenging design area in high power and high frequency machine drives is current sensing. A number of different sensing methodologies have been used over the years in this role [9], from hall effect based sensors and fluxgate

magnetometers to the simple shunt resistors. The first two methods allow to estimate the current flowing in a conductor at any given time by measuring the intensity of the magnetic field it generates these methods have the advantage of requiring no galvanic connection, maintaining isolation, between the power and sensing circuits. A big disadvantage of this type of sensors in the context of high switching frequency converters is the potential vulnerability to electromagnetic interferences due to hard switching transients. Another disadvantage of isolated current sensors is the higher cost compared to other sensing techniques.

Shunt voltage measurement are thus used in this converter, the advantages are, lower cost, lower vulnerability to EMI, at the expense of a higher bandwidth signal chain. With this method the low side current is indirectly sensed by measuring the ohmic voltage drop across the shunt resistors. It is critical that the shunts' resistance is high enough to generate an easily measurable voltage, but at the same time is needs to be low enough not to have excessive losses. To be able to support both normal operations and also over-current detection the current measurement range is from 0 to $200\mathrm{A}$. A $100\mu\Omega$ shunt resistor is used in order to limit the maximum power loss to $4\mathrm{W}$; yielding a full scale output voltage of $20\mathrm{mV}$. A fully differential signal path is used to maximize immunity from electromagnetic interferences.

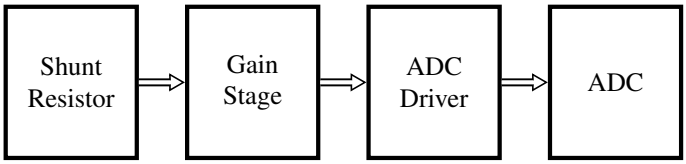

Fig. 2: Current measurement signal chain

The first component of this chain, as in figure 2 is a fully differential amplifier (FDA) that applies a gain of 50 to make full use of the analog to digital converter range. A problem with this type of components is the high input offset voltage, this is compensated by injecting a current on one of the two feedback paths, unbalancing it. This gain stage is placed as physically close to the shunt resistor as possible to minimize loop inductance, and thus magnetically couple noise induction. The next component in the chain is the wide bandwidth differential ADC driver, it is needed to provide a low enough impedance to the ADC input to quickly charge the internal sampling capacitor, as shown in figure 3. Another function of this component is the rejection of any common mode noise. Finally the last step in the chain is digitization if the resulting signals, with a 12 bits 2 Msps Simultaneous sampling analog to digital converter, this architecture while being generally more expensive than the more common multiplexed one, allows the detection of potential current leakages, caused by failure of the insulation system.

Even if the output current can be assumed constant over a switching period, due to the highly inductive load, the shunts, due to their position in circuit, are carrying it only for part of the period; the output voltage of the shunts will thus be

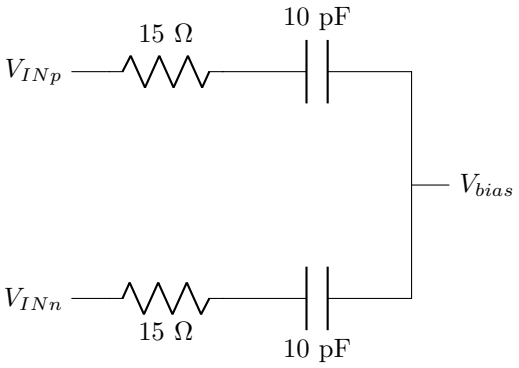

Fig. 3: ADC equivalent input circuit

a square wave of varying duty cycle. The bandwidth of such signal in not clearly defined and is strongly dependent on raise and fall times, which are influenced by a number of unknown variables, like parasitic inductances of the physical circuit's layout. Nonetheless an estimate is needed for the correct design of the gain stages and the choice of anti-aliasing filter cutoff frequency. Assuming a RC low pass type of response, a widely known approximation for the bandwidth of a square wave of known rise time is shown in Equation (13), for a signal with $10\ \mathrm{ns}$ edges, this results in a $35\mathrm{MHz}$ bandwidth.

$$BW[\mathrm{GHz}] = \frac{0.35}{t_r aise[\mathrm{ns}]} \tag{13}$$

VII. Conclusions

This paper presents an advanced high frequency and high power machine drive employing to the fullest extent possible the advantaged brought on by Wide bandgap class devices attaining high fast switching, while mantaining high efficiency. Detailing how the principal challenges, in term of power device selection, thermal, gate driver and current sensing design have been solved, in order to attain the desired specifications.

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