Effect of Parameters Variability on the Performance of SiC MOSFET Modules

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***Abstract*—This paper introduces a statistical analysis of the impact of devices parameters dispersion on the performances of parallel connected SiC MOSFETs. To this purpose, the statistical fluctuations of threshold voltage and current factor are evaluated on a set of 20 MOSFETs. In order to assess the effects of parameters spread in a real operating condition, the electrothermal simulation of a 200kHz synchronous buck converter is performed. Subsequently, an investigation of the switching energy unbalance, as a function of parameters distribution tolerances, is achieved through several sets of Monte Carlo electrothermal simulations. The results aim at aiding both the design of multi-chip configurations and the selection of appropriate fabrication process rejection boundaries.**

Keywords—electrothermal simulation, Monte Carlo simulation, multi-chip, power MOSFET, silicon carbide (SiC), SPICE.

I. INTRODUCTION

Driving circuits based on power semiconductor devices are essential to operate the electric motors utilized in a big variety of transportation systems, ranging from road and rail vehicles to vessels and aircrafts. Thus far, Si-based IGBTs represented the preferred choice for a wide range of applications and their reliability issues have been deeply investigated [1] [2]. However, the need for more compact, reliable and efficient converters pushed to seek better performing devices. Wide bandgap semiconductors, like silicon carbide (SiC) and gallium nitride (GaN), drew great attention thanks to superior material properties, such as higher critical electric field and thermal conductivity. In recent years, SiC power MOSFETs with excellent static and dynamic performances became commercially available [3] [4]. In addition to this, efforts were made in studying their short circuit ruggedness [5] [6] [7], which is a common automotive requirement. However, in order to exploit them in the transportation sector, it is necessary that they reach the current ratings required by the various application areas, which span from few hundred Amperes of road vehicles to several thousands of electric trains. Nowadays, the current rating of single die SiC MOSFETs is limited at 200 A [3], which restricts the range of application in which they can be adopted. A possible cost-efficient way to overcome this limitation consists in connecting in parallel several devices in order to reach a desired current capability. Nevertheless, paralleling two or more SiC MOSFETs can lead to unbalanced static and dynamic devices performances (Fig. 1) [8] [9] [10], thus resulting in poor long-term reliability. For these reasons, the design of parallel configurations (either as discrete components or as multi-chip power modules) needs to be carefully optimized.

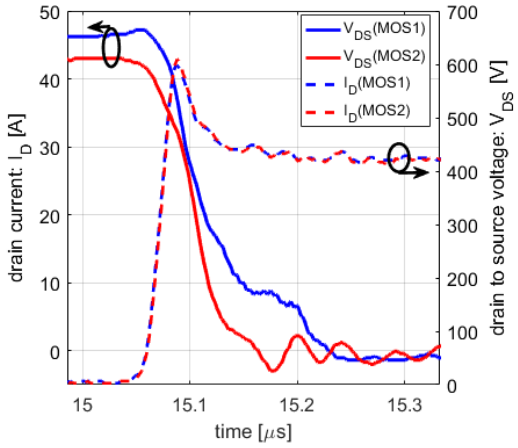

Fig. 1. Drain current (I_D) and drain to source voltage (V_{DS}) experimental turn-off waveforms of two parallel SiC MOSFETs under inductive load switching with L_{LOAD}=50 uH, I_{LOAD}=90 A, V_{DC}=400 V.

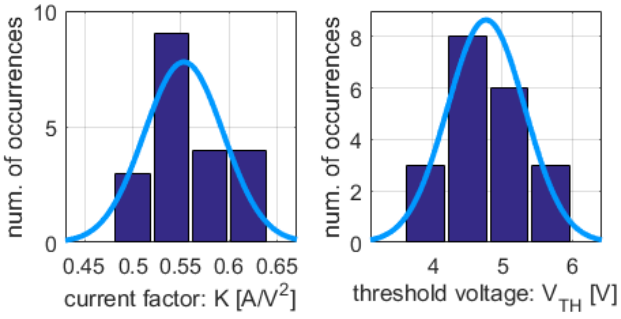

Fig. 2. Histograms of statistical distributions and fitting Gaussian functions (light blue lines) for both current factor (left) and threshold voltage (right), measured on 20 DUT samples at T=27°C,

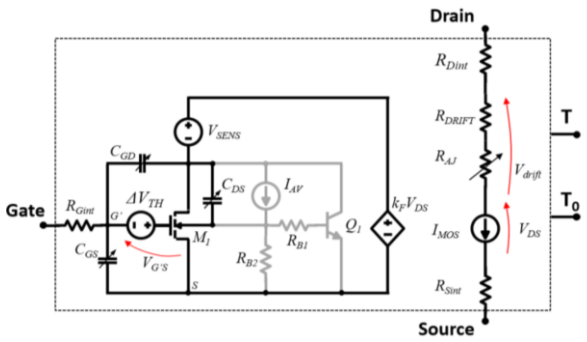

Fig. 3. Subcircuit implementing the SiC MOSFET model, with electrical and thermal nodes. Elements in gray model the out-of-SOA operation [14].

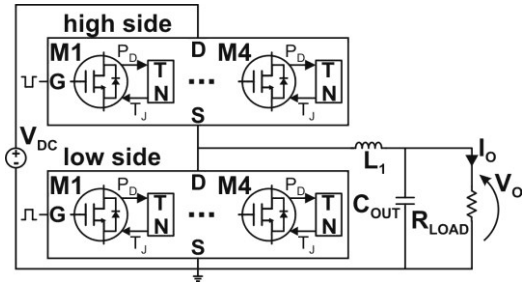

Fig. 4. Circuit schematic of the buck converter under test. Each MOSFET is connected to a thermal network (TN) provided by the manufacturer.

There are generally two root causes underlying uneven devices behaviors: devices parameters mismatches and asymmetrical circuit layouts [11]. This paper focuses on the effects of V_{TH} (MOSFET threshold voltage) and K (MOSFET current factor) dispersions on parallel SiC MOSFETs.

In order to investigate the uneven temperature rises among devices in a realistic operating condition, an introductory case-study of a DC/DC converter is simulated with arbitrarily selected V_{TH} and K values. Successively, the influence of devices mismatches is analyzed through electrothermal (ET) Monte Carlo (MC) simulations of four parallel MOSFETs under inductive load switching. Such analysis is systematically iterated by truncating the parameters distributions on intervals of increasing width. This allows quantifying the influence of process tolerance on the behavior of parallel devices.

II. DC/DC Converter Electrothermal Simulation

A. Parameters Statistical Distributions

In order to evaluate the effects of device parameters (V_{TH} and K) dispersions, a statistical description of their fluctuation is needed. Therefore, V_{TH} and K were extracted from the experimental characterization of a set of 20 virtually identical SiC MOSFETs. V_{TH} was measured through the quadratic extrapolation method from the steepest section of I_D-V_{GS} isothermal curves, while K was derived from I_D-V_{DS} characteristics at V_{GS}=20 V.

Afterward, the histograms of both parameters were evaluated (Fig. 2). These allowed quantifying spreads of about 0.15 A/V^2 and 3.5 V for K and V_{TH}, respectively. The distributions were found to be well fitted by Gaussian functions and these were used to describe devices parameters variations in the subsequent statistical analysis.

B. SiC MOSFET Compact SPICE Model

Thanks to the good trade-off between accuracy and computation time offered by ET compact device models, these represent a useful tool to support the design of several circuit solutions [12] [13]. In this paper, both the DC/DC converter and double pulse test (DPT) MC simulations relied on a previously developed ET compact SPICE model for SiC power MOSFETs presented in [14].

The model, whose sub-circuit is depicted in Fig. 3, was validated under a wide range of operating conditions at different temperatures, both in and out of safe operating area (SOA). It includes temperature dependences of the most relevant device parameters and it features two additional terminals (output - dissipated power and input - temperature rise) that allow it to be coupled to an equivalent thermal network to perform reliable ET analysis.

C. Buck Converter ET Analysis

In order to highlight the uneven temperature distribution that can develop among mismatched devices operating in parallel in a real circuit application, the ET analysis of a DC/DC converter was performed as a case-study.

The circuit (Fig. 4), designed and simulated via SIMetrix, consists in a 200 kHz - 800 V to 350 V - synchronous DC/DC buck converter. In it, two arrays of four parallel MOSFETs are arranged so that a half bridge (HB) configuration is implemented. The model introduced in the previous section is used to describe 1.2 kV - 20 A rated SiC devices manufactured by CREE. Each of them was coupled to a thermal network (TN), provided by the manufacturer, in order to enable the ET feedback.

Table I reports the K and V_{TH} values set for each MOSFET of both parallel arrays. The maximum and minimum values were chosen so that a 2σ-wide interval around the mean was spanned (i.e., their distance from the mean value is a standard deviation). This selection is meant to replicate a worst-case scenario of a technological process for which devices falling further than a standard deviation are rejected.

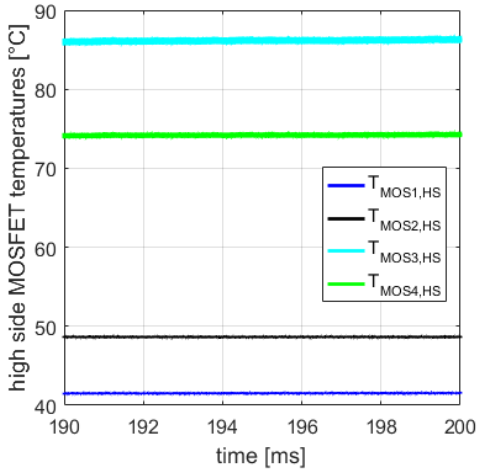

Fig. 5. Individual high side MOSFETs temperatures over the last 10ms of operation time.

TABLE I V_{TH} AND K VALUES SET FOR THE CONVERTER ET SIMULATION

	MOSFET#1	MOSFET#2	MOSFET#3	MOSFET#4
V_{TH} [V]	5.33	4.77	4.21	4.21
K [A/V^2]	0.59	0.59	0.55	0.51

The converter was simulated under constant load condition for 0.2 s of operation time. The temperatures reached by the high side MOSFETs are shown in Fig. 5. The MOSFETs withstanding the highest and lowest thermal stresses are #3 ($T_{MOS3,HS}$≈86.2°C) and #1 ($T_{MOS1,HS}$≈41.5°C), respectively. This is ascribed to the V_{TH} gap between the two transistors: a lower V_{TH} makes the MOSFET switch-on earlier and switch-off later than the other parallel devices. As overall effect, MOSFET #3 will sustain the highest transient current at each switching event, thus causing a higher switching power dissipation in that device. This, on the long run, can result in a premature failure of the component.

III. MONTE CARLO STATISTICAL ANALISYS

The analysis described in the previous section allowed quantifying the temperature unbalance between mismatched parallel MOSFETs employed in a real circuit application. However, in order to systematically relate performance non-uniformities of mismatched parallel devices to fabrication process rejection boundaries, the following MC analysis was conducted.

A. Monte Carlo Electrothermal simulations

The DPT on four parallel MOSFETs was adopted as the object of the MC campaigns conducted in this work. The schematic of Fig. 6 represents the circuit setup along with parasitic elements and test parameters.

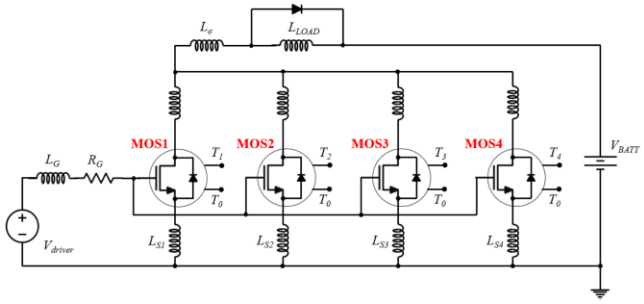

Fig. 6. Circuit model of the four parallel SiC MOSFETs employed for DPT Monte Carlo campaigns. V_{BATT}=800 V, L_{LOAD}=142 µH and R_G=2.5 Ω.

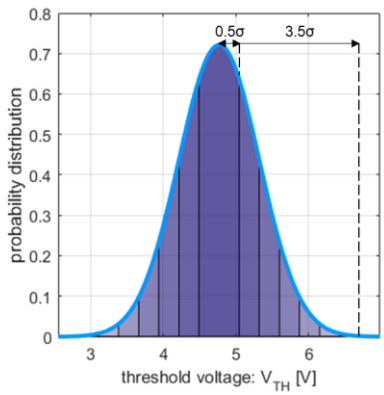

Fig. 7. Example of tolerance windows selected for the threshold voltage distribution.

Two test cases were considered. In the first one, the devices were switched at nominal current rating I_D=20 A (i.e., at load inductor current I_{LOAD}=80 A), while, in the second one, an out-of-SOA condition was investigated by switching at I_D=40 A (load inductor current I_{LOAD}=160 A). For each of those cases, seven sets of 1600 MC ET simulations were performed by varying the limits at which the normal distributions of K and V_{TH} were cut. In particular, as elucidated in Fig. 7, parameters intervals of increasing width were swept from µ ± 0.5σ to µ ± 3.5σ by steps of 0.5σ.

After each MC campaign, the histograms of turn-on (E_{on}) and turn-off (E_{off}) switching dissipated energies were evaluated. Examples of E_{off} histograms are reported in Figs. 8 and 9 for the conditions of µ ± 0.5σ and µ ± 2σ

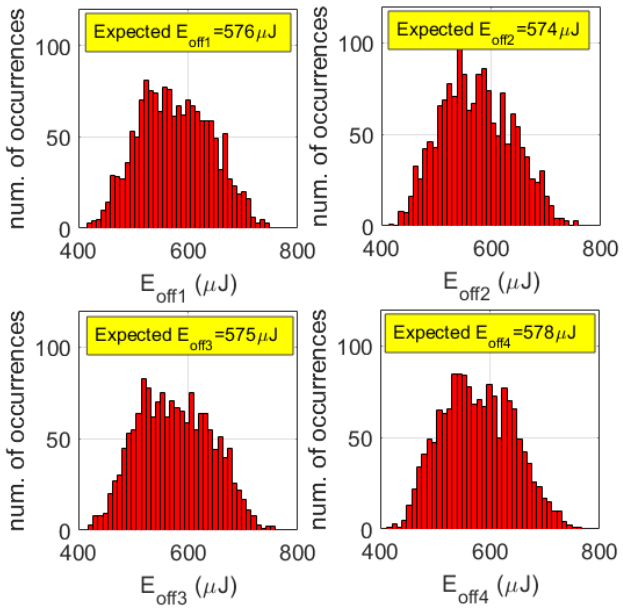

Fig. 8. Histograms of the turn-off dissipated energy evaluated over 1600 MC ET simulations for the four MOSFETs at I_{LOAD}=80 A and tolerance interval set at µ ± 0.5σ.

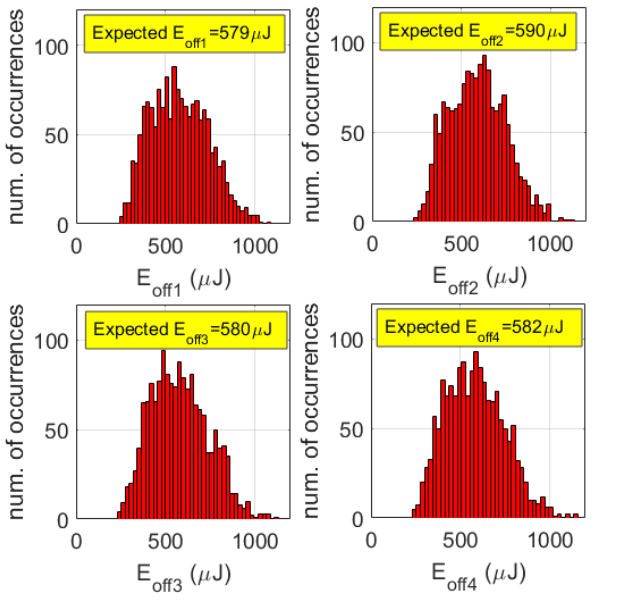

Fig. 9. Histograms of the turn-off dissipated energy evaluated over 1600 MC ET simulations for the four MOSFETs at I_{LOAD}=80 A and tolerance interval set at µ ± 2σ.

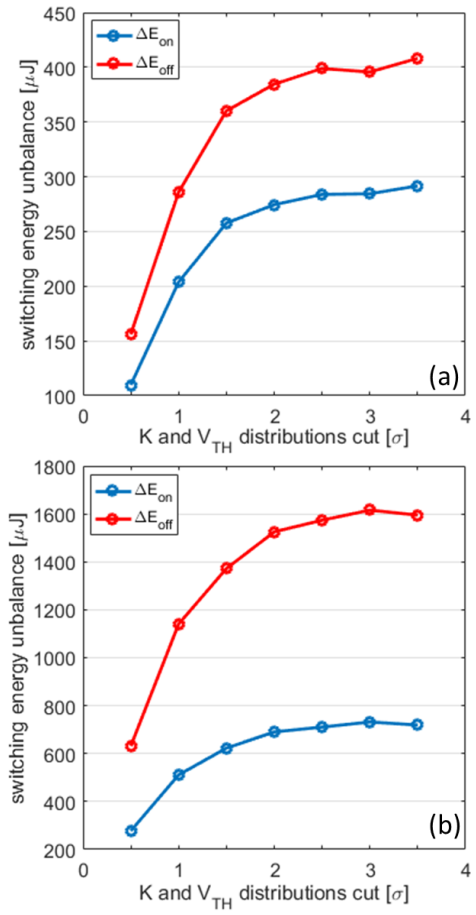

Fig. 10. Turn-on (blue) and turn-off (red) switching energy unbalances for both cases of I_{LOAD}=80 A (a) and I_{LOAD}=160 A (b).

distribution cuts, respectively. The resulting shape highlights a normal distribution. Moreover, while the mean value stays relatively unchanged at 579 µJ for both cases, the standard deviation increases from 65.1 µJ to 160 µJ as the parameters spread increases. Another quantity of interest for reliability purposes is the most likely maximum switching energy spread (ΔE). This was computed per each MC run, for both switching edges, as reported in (1) and (2).

$$\Delta E_{off}=\max(E_{off1}, E_{off2,...}, E_{off4}) - \min(E_{off1}, E_{off2,...}, E_{off4}) \quad (1)$$

$$\Delta E_{on}=\max(E_{on1}, E_{on2,...}, E_{on4}) - \min(E_{on1}, E_{on2,...}, E_{on4}) \quad (2)$$

ΔE_{off} and ΔE_{on} histograms were evaluated for all the considered parameter distribution cuts.

Fig. 10 relates the energy spreads mean values to the size of parameters distributions truncating windows, for both considered values of load current. These data can be used to draw guidelines for the design of multi-chip power modules or to select appropriate rejection boundaries for the devices technological process. For instance, considering only the power dissipation given by the switching energies, the unbalance in temperature rise can be estimated as in (3), where f_{sw} and R_{th} are the switching frequency and the power module thermal resistance, respectively.

$$\Delta T_{sw}=(\Delta E_{on} + \Delta E_{off})\times f_{sw}\times R_{th} \quad (3)$$

Assuming that the distributions were truncated at 1.5σ, and given an application like the converter described in this work, where f_{sw}=200 kHz and R_{th}≈0.6 K/W, (3) would provide a maximum temperature difference ΔT_{sw}≈74 K. Such estimation can be compared to the maximum allowable temperature spread that would ensure a desired power module lifetime.

IV. Conclusion

In this paper, a statistical analysis of parameters spread impact on parallel connected SiC MOSFETs has been presented. In particular, the attention has been focused on MOSFET threshold voltage and current factor, whose distributions have been extracted from a set of 20 devices. In order to highlight the effects of device parameters dispersions on a real application, a preliminary ET simulation of a synchronous buck converter has been performed. Consequently, the relation between maximum parameters tolerances and maximum expected switching energy unbalance has been analyzed through several MC ET campaigns. The resulting data have been used to give an example of how these can be employed to assist the design of multi-chip power modules or to select appropriate tolerance edges for the devices technological process.

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