Design and Evaluation of a Power Converter for an Energy Storage System for Aircrafts

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***Abstract*—This paper presents the design and evaluation of a power converter to be used in an energy storage system for aircrafts that is be able to control the 270V dc bus voltage during large load disturbances and regeneration. A study is conducted in order to enable the sizing of components and topologies according to the specifics of the application in order to reduce the weight of the components. Experimental results of a power converter demonstrator shows its performance.**

Keywords—EMI filter, energy storage, power converter.

I. INTRODUCTION

The "more electric aircraft" [1] is a concept that aims at employing more electrical technologies in the operation of aircrafts with the purpose of minimizing the overall weight of the systems and increasing the efficiency of energy conversion (electrical motors are significantly more efficient than hydraulic) that would ultimately reduce the fuel consumption and associated costs. Using more energy storage in the form of electrochemical energy storage devices such as supercapacitors and batteries is part of this concept with the aim of handling the power peak requirements so that the generators can be sized based on the average and not peak power requirement, whilst the availability of storing regenerated power from flying surfaces or propellers that is temporarily available, may further reduce fuel consumption.

This paper investigates the design of a 22.5kW power converter for an energy storage system (ESS) that would enable the optimisation of the ratings of the power generation, stabilisation of the DC power bus and will allow the regenerative operation of various loads power. The paper starts by discussing the design factors that influence the weight of a power converter, in the context of energy storage applications. The dependency of current ripple both on the energy storage (ES) side and the DC-bus of the aircraft as function of the topology of the battery stack that influence the weight of the filters are derived. A procedure for designing the filter for mitigating electromagnetic interference (EMI) in accordance with relevant standards is also presented. This procedure is then applied in the implementation of a power converter demonstrator which is experimentally evaluated and its performance discussed.

II. FACTORS THAT INFLUENCE THE POWER CONVERTER DESIGN

In this section the factors that influence the design of the power converter used in a battery/supercapacitor based energy storage system for aerospace applications, which impact the overall system weight, will be discussed. This will include the impact on design of both filters, on the battery/supercapacitor side to limit the current ripple that has to be handled by the energy storage components and on the 270V DC bus to provide compliance with maximum voltage disturbance specified in the power quality standards, and also the power losses since choosing a high switching frequency enables the reduction of magnetics but may increase the losses which would require increasing the size and the associated weight for the cooling.

For this ES application, a half bridge inverter topology as shown in Fig. 1 is suitable as interface between the constant 270V dc bus voltage and the variable battery/ supercapacitor stack voltage. A capacitor is required on the inverter DC-link to smooth the DC current ripple whilst on the ES side, an inductor is needed to limit the current ripple below a maximum limit, usually specified as percentage of the main ES current. It should be noted that once this inductor value is chosen, the current ripple is independent on the main ES current and is dependent on the switching frequency, the DC-bus voltage (typically constant) and the modulation duty-cycle which for this converter is dependent on the battery/supercap stack voltage. This means that for a given power that is needed to be processed by the ES stack, there will be an indirect interdependence of current ripple on the ES stack voltage and therefore the ES current but the relationship is not linear. On the other hand, the DC-bus current ripple and the resulting DC-link voltage ripple is directly dependent on the main ES current and the inverter duty-cycle and is very little influenced by the inductor current ripple. This means that the design of the ES side and DC bus side filters are not directly linked although the switching frequency, the DC-bus voltage and the dutycycle are common factors in their design.

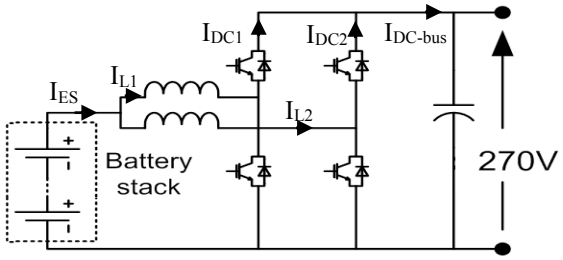

Fig. 1 Two-channel interleaved DC/DC converter topology relying on a half-bridge inverter cell to interface a battery stack to the 270V bus

A. Influence of the Battery Stack Voltage

Energy storage systems are designed to provide a specified amount of power, independent of the state of charge of the battery/supercapacitor stack. This means they need to operate in a "constant power" mode which means the design of the semiconductors and the filters needs to be done in the worst case operating condition (maximum current) which happens when voltage is near the minimum.

$$I_{ES\text{-}max} = P_N / V_{ES\text{-}min} \quad (1)$$

This means that in order to achieve the best utilisation of the power converter, the rated voltage of the battery/supercapacitor stack needs to be maximised which means using a large number of battery cells connected in series that have a smaller capacity, chosen in accordance to the required energy level W_{ES}.

$$V_{ES\_max} = N*V_{cell\_max} \leq 0.9*V_{bus} \quad (2)$$

$$C_{cell}[Ah] \geq W_{ES}/V_{ES\text{-}N} \quad (3)$$

However, when a system design of an advanced prototype demonstrator is implemented that requires the use of novel technology of battery/supercap cells and semiconductor devices, it is expected that the diversity of available sizes will be limited which means some of the subsystems will be suboptimal.

B. *Influence of interleaving*

Interleaving is a technique that enables several advantages: the implementation of power converters rated at currents multiple times higher than the rating of a single power semiconductors; by staggering the gating pulses for the switching devices in the different legs by 360/N, it is possible to obtain partial harmonic cancelation in both the cumulated inductor current seen by the energy storage devices (I_{ES}) in conjunction with increasing the frequency of the remaining current ripple and this has been modelled for both independent and coupled inductors as reported in [2]-[6]; the cancelation of resulting currents is also obtained in the DC link side of the converter that may enable a reduction of the 270V bus voltage filter which is significantly more critical in this system as the power quality standards are very tight in aircraft applications especially in the presence of a large power rated converter (tens kW). Fig. 2 shows the typical cumulated DC-bus current waveforms ($I_{DC\text{-}bus}$) and resulting voltage ripple across a 100µF smoothing capacitor that result in converter topologies with 1-4 interleaved channels. It can be seen that employing multiple interleaved channels enables the reduction of the current steps seen in the unfiltered DC-link currents to I_{ES}/N which is beneficial in reducing the voltage ripples. Another observation is that the frequency of the equivalent ripple is multiplied by $N*f_{sw}$. However, the resulting dutycycle changes which means that for a given ES stack voltage, the resulting DC-link voltage ripple for a higher number of interleaved legs may not always be smaller. This can be seen above in the ripple of the 3- and 4-chanels DC-link voltage which is very similar in terms of peak-to peak ripple, even though the current step for 4-ch interleaved would have been 25% smaller and the equivalent switching frequency would have been 25% larger. However these advantages have been lost due to the dutycycle which causes a similar ripple in the charge capacitor ($duty*I_{ES}/(N*f_{sw})$).

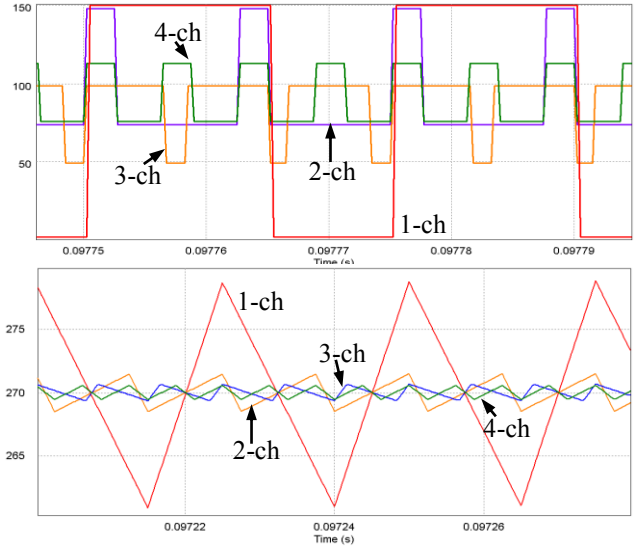

Fig. 2 Resulting unfiltered DC-bus current ripple (top) and voltage ripple across a 100µF smoothing capacitor for a converter with 1-2-3-4 interleaved channels.

Fig. 3 shows the mapping of the resulting normalized current ripple (this is the average of the pulse over the switching period, suggestive for the amount of electrical charge/voltage ripple seen by the DC-link capacitor) as function of dutycyle for 2-3-4 channel interleaved converters. Since the battery stack voltage is expected to be approx. 75% (discharged) to 100% fully charged, the dutycycle (horizontal) axis can be splitted into three ranges ($1:0.75:0.75^2$), each corresponding to a particular battery stack design: 100-75-56 series connected cells. Whilst the shape resembles the typical shapes of the DC-link current ripple curves already published in literature [2]-[6] that assume constant load current, these shown in Fig. 3 are assuming a constant power type of load which means that as no of cells reduces, stack voltage reduces which causes an increase of the overall current.

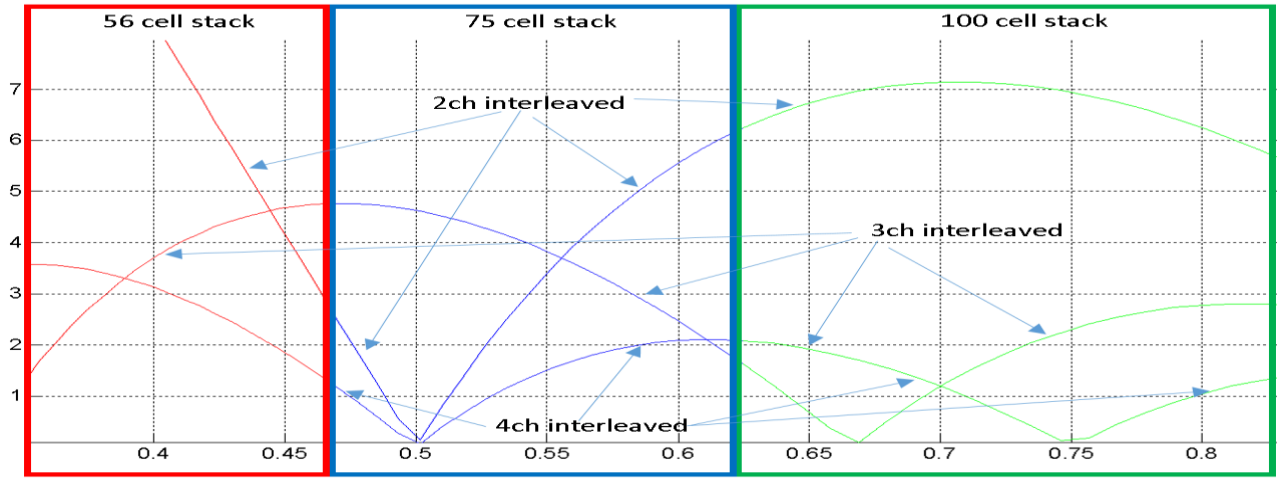

Fig. 3. Assessment of the normalised DC-link current ripple as function of duty-cycle when mapping the fully charged to fully charged voltage range of three Li-Ti battery stack designs consisting of 56 cells (left), 75 cells (middle) and 100 cells (right)

For a given no of cells in a stack, larger currents will appear as a result of the device discharging (lower voltage) which makes the ES currents to be larger on left side (ES discharged) compared to right side (ES charged). This is the reason why these particular curves are no longer fully symmetrical around the maximum point, although the dutycycle at which the cumulated ripple cancels out fully remains the same (i.e. at 50% for a 2 &4 channel interleaved and 33% and 66% for the 3-channel). This leads to some interesting results. For example, the resulting DC-link current ripple produced by a 2-channel interleaved converter is smaller when the battery stack uses 75 cells compared to 100 cells. For the 3-channel interleaved, the maximum current ripple reaches a maximum of 4.8A average of the pulse current for both the 50 cell at fully charged and the 75 cell stack at fully discharged condition whilst the 100 cell stack produces a maximum DC link current ripple of 2.8A average of the pulse current at fully charged condition;. The 4 channel interleaved converter has a similar maximum current ripple of 2.5A for both the 100-cel (at fully discharged) and 75 cell stack at fully charged condition.

C. *Influence of the power quality standards vs capability of the semiconductor technology*

The switching nature of the converter results in generation of high frequency electromagnetic energy to the DC grid in a form of current ripples having relevant harmonics at multiple the switching frequency, of magnitudes proportional to the power processed by the converter and dependant on duty ratio of the resulting current pulses. Both conducted and radiated noise is usually generated but in this study, the filter is designed to limit only the conducted (differential mode) disturbance. In order to ensure that various equipment powered from the same DC bus do not disturb each other, standards regulating the amount of EM interference (EMI) generated by a given load are imposed. In aircraft applications, the following two standards are in place: MIL-STD-704F that describes the maximum voltage disturbance with frequencies below 500 kHz that can be caused to the bus voltage and RTCA/DO-160G which refers to the maximum level of EMI generated within the 0.15-30 MHz frequency range. Although traditionally in power electronic conversion, the 0.15MHz is usually seen as the limit of a frequency range where EMI is generated by ringing due to parasitics of the switching circuit, the use of fast switching which is need to minimise weight will lead to the generation of high level of harmonics of the main switching current ripple that can easily exceed the limits imposed by the standards.

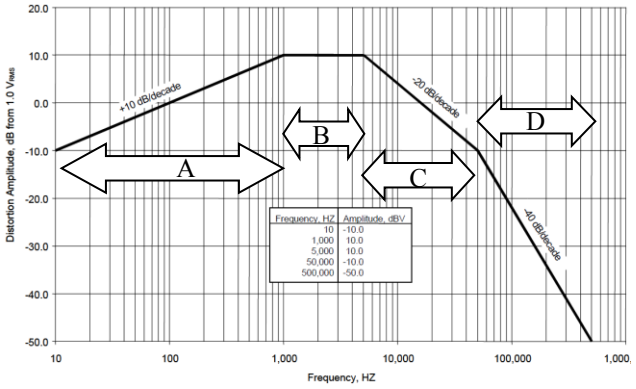

Fig. 4. Maximum voltage distortion spectrum caused on the 270V DC bus as specified in MIL-STD-704F [7]

MIL-STD-704F standard [7] includes a detailed specification for the maximum voltage distortion that can be induced by an equipment connected to the 270V bus, as function of frequency which will be used to design the DC-link distortion filter and this is shown in Fig 4.

It can be noted that the envelope for the allowed voltage ripple as imposed by the MIL-STD-704F standard has four regions, with region C (5-50kHz) and D (>50kHz) that would correspond to the disturbance caused by the main switching of the converter as processing the rated power. The limits are highly dependent on the frequency of the ripple which makes the design of the filter even more challenging. Whilst region C is characterised by a -20dB/decade slope, which is typical for a 1st order filter, region D requires -40dB/decade which means that a higher order filter is needed. In addition, if an LC filter is considered that usually provides same attenuation (-40dB/decade), it means that for a given converter, switching faster the same battery current will require the same cut off frequency (same size of the filter) as the advantage of having a significantly higher frequency of the DC-link current ripple will be lost as the filter attenuation and the slope of the allowed limit are the same. For this reason, in addition to using wide bandgap devices (SiC or GaN) which due to fast switching and low loss are an obvious choice when designing a high power converter for low weight application, considering a standard silicon switch technology makes also sense.

In order to comply with the RTCA/DO-160G standard [8], the designed EMI filter for conducted emission level has to fulfil the requirement of Category B conducted emission for power lines set as specified in RTCA/DO-160G Section 21, “Emission of Radio Frequency Energy” and the profile is shown in Fig. 5.

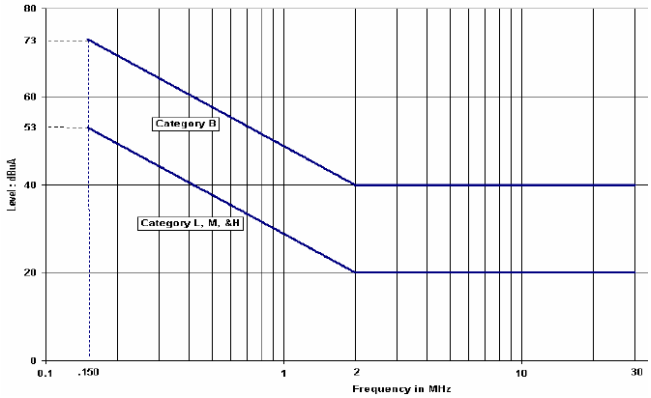

Fig. 5. Maximum level of cconducted RF interference for power lines as specified in RTCA/DO-160G standard [8]

III. Selecting the Power Converter Topology

In the current paper, the need to handle a large amount of charging power required the use of a very specific battery Lithium-Titanate chemistry that resulted in a very limited choice of available cell sizes, with the smallest available cell being the 2.26V/13Ah [9]. This resulted in a battery stack of 75 series connected cells that fulfilled the stored energy required by the application and gave a rated battery stack voltage of 170V. The selection process is detailed in [10].

Fig. 3 already compared the resulting DC-link capacitor charge/voltage ripple produced by interleaved converters with 2-3-4 channels as function of the dutycycle/voltage ratio for different configuration of battery stacks of 100-75-56

cells. The conclusion of that study was that from the DC-link ripple point of view, the 75-cell design is actually causing smaller ripples than the 100-cell design for a 2-channel interleaved topology, whilst the smallest ripples are obtained by a 4-chanel interleaved. Although a 3-channel interleaved topology would result in less complexity compared to a 4 channel, it can be seen that is not a significantly better solution for a 75 cell topology compared to the 2-channel. For this reasons, since the stack design is limited by the availability of the battery cell, it was considered that the 2-channel interleaved using larger device ratings and the 4 – channel interleaved topologies requiring smaller current ratings would be two options for which the weight of the converter should be evaluated.

It should be noted that at the time of this initial assessment was made, the availability of power modules with wide bandgap devices was limited only a few SiC devices options, whilst the most compact silicon switching device was available at a relatively low power rating. This led to the final selection where the evaluation of the power integration potential of a 2-channel interleaved SiC design versus a 4-channel interleaved Silicon design was conducted. Two power modules have been identified: the Infineon H-bridge 600V/75A IGBT [11] using a low weight Econopak package containing the Trench/Fieldstop IGBT3 and the Emitter Controlled 3 diode that will be required to switch at 20kHz versus the first generation Cree 1.2kV/100A SiC MOSFET [12] using a fairly bulky/standard power module packaging that embeds a single half bridge, but operating at 40kHz. In order to estimate the weight of the various converter components, first an analytical model to determine the variation of switching ripple versus dutycycle has been implemented to identify the worst case operating points which would then be used in sizing the battery side inductance needed by the two converters. Fig. 6 exemplifies the current ripple vs dutycycle characteristic typical for a 4-channel interleaved DC/DC converter with coupled inductors required by the silicon implementation. The stresses in the key operating points can then be validated by simulation (not shown). This approach enabled the choice of the inductance needed for both converters and to identify the current stresses (peak current which is relevant for the choice of the switches and the airgap of the inductors to avoid saturation and current ripple in inductors) which was later used to design the inductors (selecting the core geometry, calculate no. of turns etc) which then can be used in estimating the weight of the magnetics and the losses. The weight of the DC-bus filter is not considered yet at this stage.

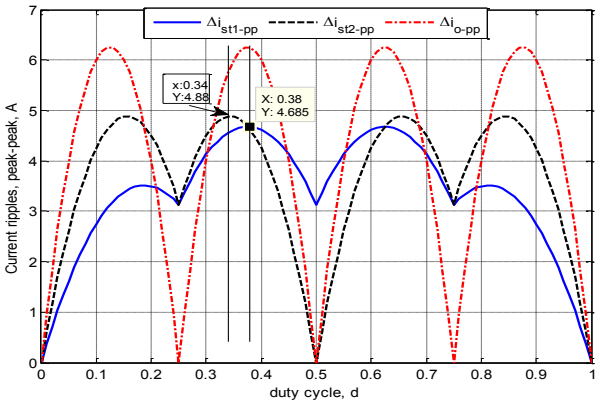

Fig. 6. Peak-peak current ripples for the various coupled inductor stages of the 4-channel interleaved converter, at different duty cycles

A PSIM simulation model was also used to determine the semiconductor power losses of both converter implementations in the key operating points (maximum current) to estimate the size/weight of the heatsink (forced air cooling was assumed). This enabled the estimation of the total converter loss at rated power conditions and maximum current (ES almost discharged) which is needed in the design of the cooling and the associated weight of main components and these details are shown in Table I.

The semiconductor power losses have similar levels (320W for Silicon and 376.6W for SiC) but it should be noted that the SiC converter handles 50% more power 22.5kW and is implemented in a 2-channel interleaved topology compared to 15kW implemented in a 4-channel interleaved topology. The derating in current power for the Silicon converter is needed in order to make sure that the relatively large losses encountered by the switches commutating in are switching mode at 20kHz are safely dissipated (device temperatures were estimated to reach 132°C for the transistor and 122°C for the diode chip when the heatsink temperature was assumed to be kept at 80°C by appropriately choosing the heatsink size). It should be noted that the maximum admissible temperature for these Silicon devices as stated in the datasheet is 175°C. In terms of distribution of losses, the conduction vs switching split is fairly equal share.

TABLE I. COMPARISON OF POWER LOSSES, WEIGHT AND POWER INTEGRATION POTENTIAL OF SILICON VERSUS SIC

	15kW/20 kHz Silicon IGBT, Infineon	22.5kW/40 kHz SiC MOSFET, Cree
Loss Magnetics	109.2 W	170.8
Semiconductor W	320.2	376.6
Total losses, W	429.4	547.4
Losses in %	2.86 %	2.43 %
Heatsink $\Delta T_{h\text{-}a}$	20K	41.8K
$R_{th\text{-}h\text{-}a}$ of heatsink	0.0625 K/W	0.111 K/W
Mass of heatsink	2.13 kg	1.2 kg
Mass of magnetics	3.16 kg	3.14kg
Power module mass	0.048kg	0.8kg
Electronics, g	0.3kg	0.3kg
Total weight, g	5.37kg	5.44kg
Specific power	2.78kW/kg	4.17kW/kg

It should be noticed that due to the need to minimise weight, both converters will operate with a similar level of loss percentage (2.4-2.9%) and although the commercially available SiC power module is clearly not optimised for high power density (the module is 18 times heavier than the Infineon package whilst processing only 50% more load current), the system implementation with SiC provides 50% more specific power (kW/kg) than the Silicon mainly due to the weight savings in the inductor (weights are similar but SiC module provides 50% more power) and significantly smaller heatsink, as the SiC module can work with almost twice temperature differential which . This is the reason why the choice was made to implement the power stage using SiC power modules in a 2-channel interleaved implementation.

IV. Design of the EMI Filter

In this project, the need to handle a large amount of power (22.5kW) resulted in a large amount of current harmonics. The frequency spectrum of the injected current ripple into the EMI filter from the converter at different values of dutycycles/voltage transfer ratios as expected from the voltage range of the 75 cell battery stack is calculated and plotted in Fig. 7. It should be noted that Dt is the dutycycle of the current pulse seen in the DC-link and for a 2-channel interleaved converter this is given by:

$$Dt = 2V_{ES}/V_{bus} - 1 \quad (4)$$

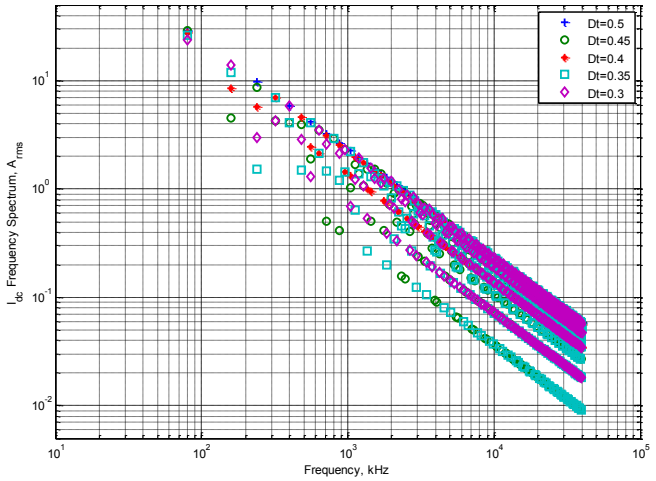

Fig. 7. Frequency spectrum of the DC-link current ripple injected into the EMI by the DC/DC converter ($I_{ch}=I_{ES}/2=65A$)

It can be seen that the largest current harmonics are generated at Dt=0.5 (equivalent to $V_{ES}/V_{bus}=0.75$ which may happen when the battery is near fully charged and charging so that the voltage drop across internal resistance adds up to back EMF) and therefore this operating point was used in the design of the EMI filter: $V_{ES}=202.5V$, $I_{ch}=65A=I_{ES}/2$, $I_{DC\text{-}bus\text{-}av}=97.5A$, $I_{dc\_rip}=32.5A_{rms}$.

In order to establish the required attenuation and therefore the order/ topology of the filter, a calculation of the required minimum attenuation is carried out considering a simplified model. Initially it is assumed that each power module is decoupled by 5µF low inductance snubber capacitors giving a total DC-link capacitance of 10µF. From Fig. 4, the maximum allowed voltage ripple at 80 kHz ($f_{noise}=2fsw$) as seen on the DC bus is 125mVrms (-18dB is 1/8 of 1Vrms). This is produced by the 80 kHz (2fsw) DC-link current ripple generated by the converter in worst case condition which is 28Arms as extracted from Fig. 7. In the simplified assumption, it is assumed that all this current ripple to be fully handled by the 10µF decoupling capacitors and therefore the resulting voltage ripple at the power module DC terminals is 5.7Vrms (@80kHz). This means that the filter that should stand between the 10µF DC-link decoupling capacitors and the main 270V DC bus of the aircraft should have an attenuation of at least 45.6 (33.2dB) at 80kHz. One should note that whilst the 80 kHz harmonic may be considered predominant, multiples of this harmonics can also create problems because of the 40dB/decade slope that defines the limits above 50 kHz.

Fig. 8 illustrates how a given attenuation can be achieved with different order/topologies of filters. It should be noted that the behaviour shown is a simplified representation where the resonance points have been removed for simplicity. It can be noted that in order to achieve a particular level of attenuation (-A) at a given frequency of the main disturbance f_{noise}, a reduced order filter will require a significantly lower cut off frequency than a higher order filter. In case the high order filter cannot be implemented in a symmetrical way, multiple cut off frequencies exist and the highest attenuation is only achieved above the highest of these frequencies.

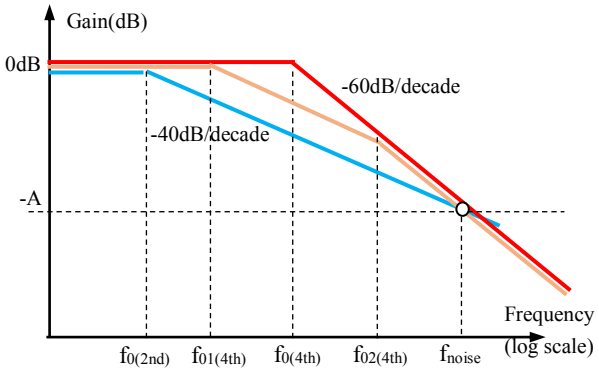

Fig. 8. Typical gain versus frequency characteristics for 2nd and 4th order filters in relationship to the required attenuation –A @ f_{noise}.

For example, a second order LC filter (blue curve) will provide an attenuation of -40dB/decade. In the case considered, in order to achieve an attenuation of 45.6 (33.2dB) at 80kHz, the cut off frequency should be 80kHz/√45.6 = 11.8kHz. Unfortunately, the application required the installation of a large capacitor (730µF /film) to act temporary power buffer during the time interval that the voltage controller reacts (1-2ms) and to limit voltage overshoots caused by sudden changes in the load power. This capacitor however is characterised by a significantly larger stray inductance compared to the decoupling snubber capacitors installed with the power modules and for this reason, it cannot play a positive role in the operation of the EMI filter, however the full equivalent model parameters should be included in any EMI filter validation model of the converter to make sure any unwanted interactions are detected. For this reason, a 3th order LCL filter is connected between the 10µF decoupling capacitor of the power modules and the 730µF power buffer capacitor connected on the DC-bus.

To validate these choices, a full model of the converter system as seen from its DC-link including the LCLC filter, the Line Impedance Stabilisation Network (LISM) as specified in the EMI emission standards is modelled and this is shown in Fig. 9. To assess as realistically as possible the characteristic of the filter, the parasitics of all passive components have been accounted for and these details are shown in Table II.

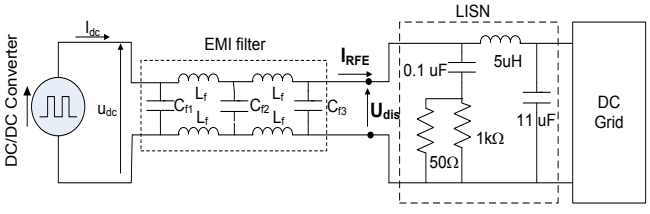

Fig. 9. Current ripple circuit model of the converter, EMI filter and LISN

TABLE II. PARAMETERS OF EMI FILTER COMPONENTS

	C_{f1}	C_{f2}	C_{f3}	L_f
Capacitance (μF)	10	5	730	
Series inductance, (nH)	50	80	127	2x6000
Series resistance (mΩ)	3	6	3	2x5
$I_{rip\text{-}Max}$(A_{rms}@100kHz)	49	24.5	70	
Weight	2x80g	80g	1.3kg	230g for 2xLf on one AMCC6.3 metglas core
Observations	MKP386M Snubber Vishay		Cornell-Dubilier	

It should be noted that although the overall weight of the EMI filter is 2kg, 65% of this is represented by the weight of the power buffer capacitor (1.3kg) which has very limited role in dealing with the residual switching ripple of the converter (>80kHz) due to its large stray capacitance.

The DC/DC converter is modelled by a current source that injects the current ripple component of I_{dc} current waveform which was shown in Fig 7, into the aircraft's DC bus, via the EMI filter and the LISN. This circuit model will be used for the design and validation of the EMI filter. The LISN input impedance should comply with the impedance profile as specified in RTCA/DO-160G (Fig. 10a). The impedance of the LISN network shown in Fig. 9 is illustrated in Fig. 10b and it can be concluded that there is a good match between model and the limits specified in the standard.

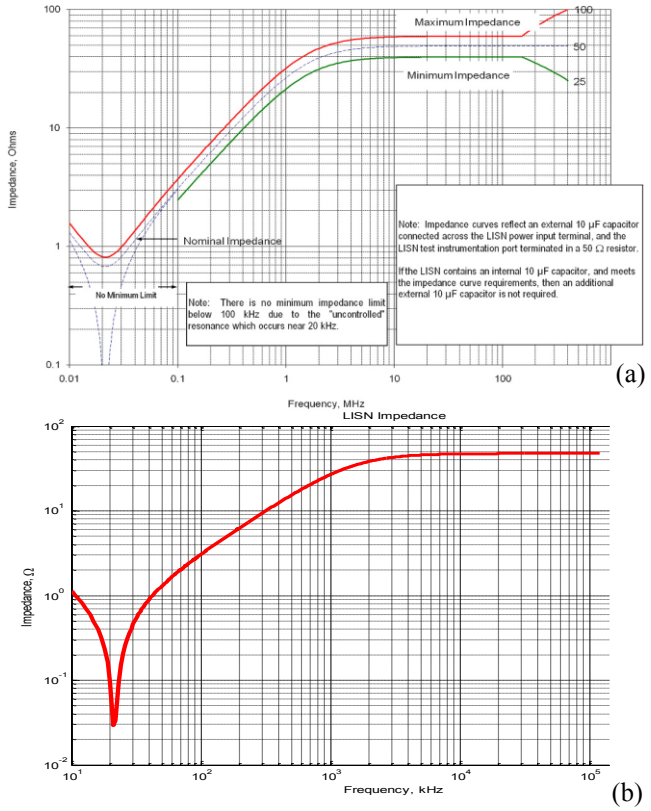

Fig. 10. LISN Impedance Stabilisation Network input Impedance as specified in a) RTCA/DO-160G standard and b) as modelled by Fig. 8

The calculated frequency components of the current ripple at different values of Dt shown in Fig. 7 are applied to the EMI+LISN circuit shown in Fig. 9 and the RF conducted emission current I_{RFE} is calculated and compared with the Category B limit specified in RTCA/DO-160G. The results are shown in Fig. 11. It can be noted that all I_{RFE} harmonics are well below the Category B limit for the whole frequency range although the smallest margin (20dB) is at 80 kHz.

The voltage distortion U_{dis} as defined in Fig. 9, is also calculated for each current harmonic defined in Fig 7 and compared with the maximum distortion spectrum as specified by MIL-STD-704F for a 270V DC system. It is found that the designed EMI filter also complies with the MIL-STD-704F standard for distortion spectrum and this is illustrated in Fig. 12. The closer to the envelope limit are the 80 kHz harmonic where the margin is approx. 32dB and the upper >1MHz where the margin is approx 18dB. It should be noted that the compatibility with the upper limit will be significantly affected by the parasitics of the decoupling capacitors, the cabling, the power switches and the DC-link power plane.

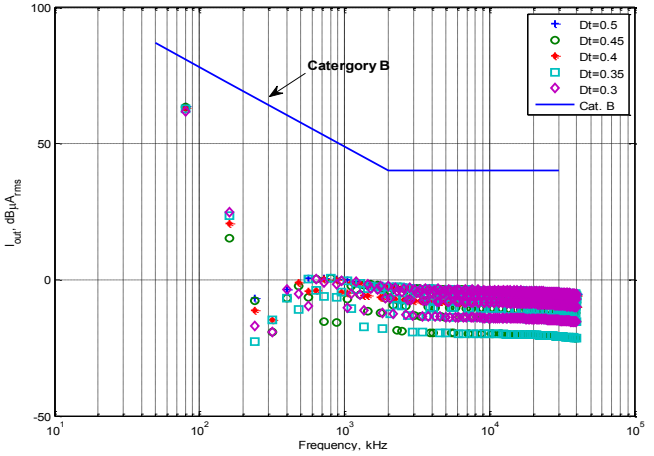

Fig. 11. Radio Frequency conducted emission of the designed EMI filter versus the limits as specified by the RTCA/DO-160G standard

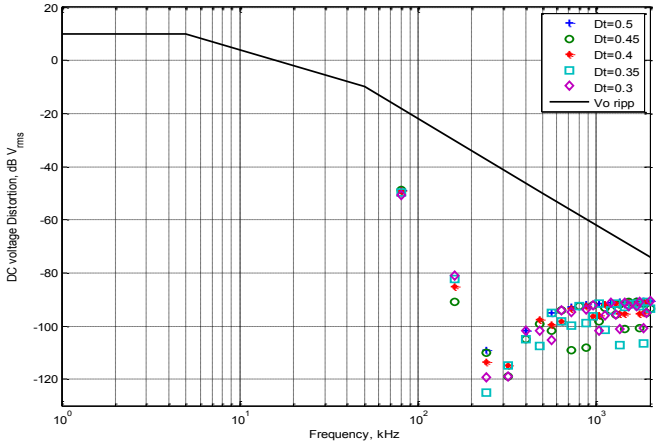

Fig. 12 Distortion spectrum of the designed EMI filter versus the voltage harmonics limits specified by MIL-STD-704F

V. EXPERIMENTAL EVALUATION OF THE ESS

The ESS control system block diagram is shown in Fig. 13. It consists of a DC bus voltage control loop followed by two DC/DC converter current control loops controlling each of the converter legs. The ESS is able to take care of the DC bus voltage regulation maintaining it at the desired voltage reference u^*_{dc}, which is set by a supervisory controller. The output of the PI voltage controller which is the reference current for the ESS is fed as an input to the PI current controllers of the DC/DC converter phase currents which allows handling of imbalances between the two interleaved phases which enables adjustment of individual leg loading in order to manage different heating and component degradation. The reference current I^*_{ph1} and I^*_{ph2} are limited

according to the value of I_{lmt} (up to 85A/phase) that can also be set by the supervisory controller. The independent outputs of the two PI current controllers are added to the measured battery stack voltage to produce the reference voltage u^*_{ph1}, u^*_{ph2} of the DC/DC converter phases which are fed to the PWM generator to produce the interleaved switching pulses for the DC/DC converter semiconductor switches. This control algorithm is implemented in a digital control platform using a commercial C6713 floating point DSP and a custom designed FPGA.

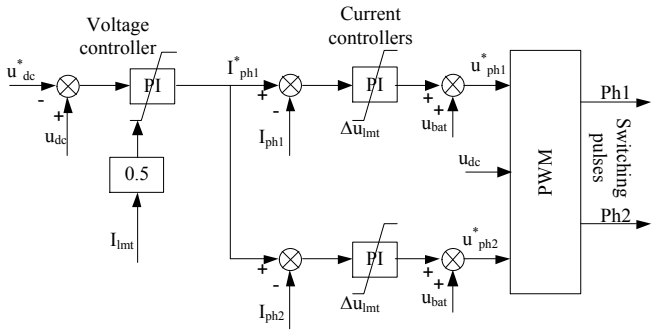

Fig. 13. The control diagram of the Energy Storage System

Fig. 14a shows the detailed schematic of the actual implementation of the full energy storage system, including the battery stack formed of five 15 cell LTO modules, the inrush circuit, the interleaved DC/DC converter, the EMC filter (that includes also a modified LISN to provide decoupling from a 15kW DC power supply used during testing) and the associated switchgear and overcurrent protections that are needed to provide safe operation of the system. Fig. 14b shows the actual implementation of the power converter.

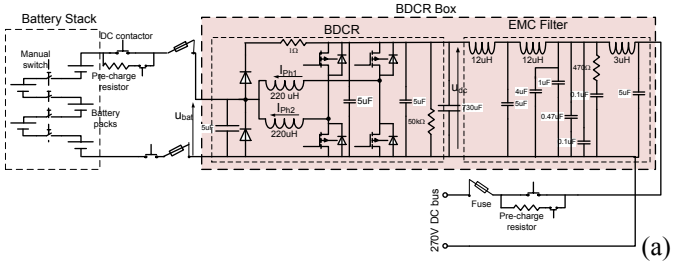

Fig. 14. a) Schematic of the battery energy storage system as connected to a 15kW power supply for testing ; b) Actual implementation of the converter system in a 19" rack enclosure (675x600x200mm) including the EMI filter, cooling, sensors and control boards

First, the validation of the EMI filter is evaluated and due to the power limitation of the power supply used to provide charging power, is done at 15kW which is 67% of the rated power. Fig. 15 shows the spectrum of the voltage ripple as seen on the 270V bus, which in the test circuit is measured at the connecting point between the 3μH which is part of the modified LISN and the 12μH inductor which is part of the EMI filter. Due to the lack of a professional EMI measurement equipment, the spectrum has been obtained by using a 12-bit oscilloscope to acquire the 270V bus voltage and post-processing it, therefore it is possible to be affected by errors larger than what would be obtained with a professional EMI test equipment. Also, the use of an electronic switched mode power supply that has internal filters and fast control may also be a source of unwanted interaction with the converter under test, which may justify some of the discrepancies found. The voltage spectrum in Fig. 15 is shown in relation to the allowed voltage ripple limit specified in MIL-704F and is clear that the 80 kHz voltage ripple is very close to the allowed limit, which is not what was expected from the EMI filter design shown in Fig. 12. Also, above 300 kHz, the resulting harmonics are exceeding the limit but since these levels are very small (<10mV), it is considered that these may not be representative as these are near the sensitivity margins of the oscilloscope fitted with the differential voltage probes .

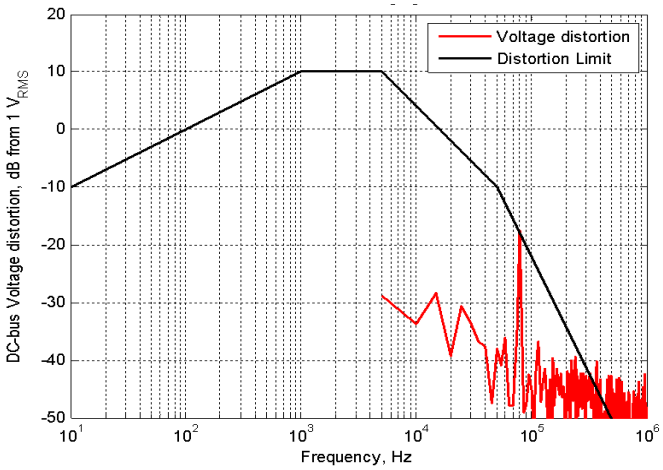

Fig. 15. The resulting DC-bus voltage harmonic spectrum in relation to the MIL-704F limits for 15kW operation

The testing of the efficiency of the power converter has been done in an arrangement involving two identical power converters connected in a back-to-back topology that allows circulation of the electrical power. A DC power supply is connected to the low voltage (ES) port and supplies the system losses which are then very easy to measure. Fig. 16 shows the converter efficiency versus loading and the measured temperature of the heatsink. The efficiency level is significantly better than predicted in Table I (these were absolute maximums in worst case operating conditions calculated only for the selection of the correct cooling equipment) due to higher battery port voltage used in this test (200V) which led to lower current. It should be noted that the efficiency during discharging has been found to be smaller.

The DC grid voltage controller dynamic performance is tested by using a DC power supply to suddenly inject a constant current into the DC-bus whilst the ESS is required to keep this voltage constant by directing the excess/deficit of power into the battery. The response of the DC-bus

voltage, the battery voltage, battery current and the input dc current to the converter from the 270Vbus/power supply are recorded. The results are shown in Fig. 17. It is noted that the input current from the DC-bus into the converter is stepped from 0 to nearly 51.5A. The ESS is sensing this by a the small DC bus voltage overshoot and is immediately reacting by absorbing the injected power into the DC bus and directing it into the battery, where the battery current is increased to 71A. The DC grid voltage has been disturbed during the injection reaching a peak of 275.6V and then settled down to the desired value in approx. 8ms. It should be noted that a significantly faster response is possible to be obtained by feedforwarding to the converter channel current references, a direct measurement of the current absorbed by significant load from/into the DC bus, therefore removing the delays imposed by the much slower voltage controller. This is feasible if it is assumed that in the design of an aircraft's power system, the ESS will be integrated within the distribution box that has accessible the terminals of all loads.

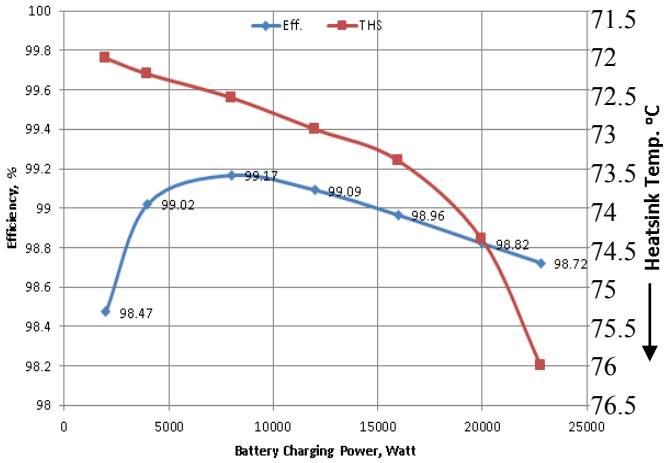

Fig. 16. Efficiency of the main converter and heatsink temperature in charging mode of operation

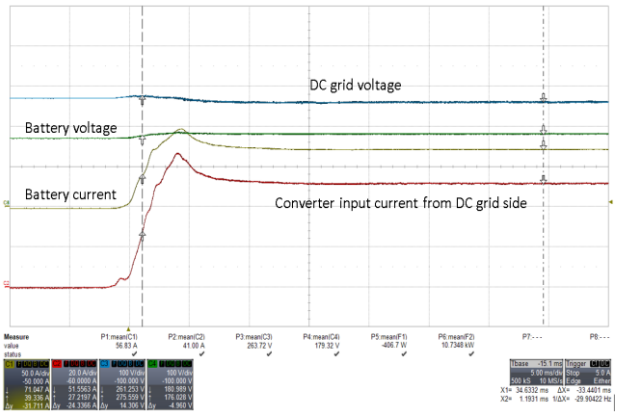

Fig. 17 Transient test of the DC grid voltage control following a 13 kW DC-bus power injection. Ch1: battery current, 50A/div; Ch2: input current to the BDCR from the DC grid side, 20A/div; Ch3: DC grid voltage, 100V/div; Ch4: Battery voltage, 100V/div. Time: 5ms/div

CONCLUSIONS

This paper presents the design and evaluation of a power converter for an aircraft energy storage system. The paper discussed the factors that are affecting the design of passive components in the context of energy storage applications that include the choice for the number of cells in the battery stack and also the design of the EMI filter. The sizing of the passive components enables the identification of maximum current stresses of the semiconductor devices which lead to an estimation of maximum losses and a selection of the cooling system. Once these are known, the weight of the passive components, the heatsink and the power modules leads to the estimation of the total mass of the system and of the power density. Although the power density of the current system is found to be not very high (<5kW), it should be noted that at the time this work has been done, a very limited selection of wide bandgap power module devices was available.

ACKNOWLEDGMENT

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