Single pulse short-circuit robustness and repetitive stress aging of GaN GITs

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***Abstract*—Short-circuit withstand capability is a key requirement for semiconductor power devices in a number of strategic application domains, including traction, renewable energies and power distribution. Indeed, though clearly a non-intentional operational mode, sort-circuit can be nonetheless a relatively frequent event. Due to its associated considerable electro-thermal stress levels, a thorough analysis of both single pulse withstand capability and device aging as a result of repetitive stress are mandatory before widespread deployment of new device technologies. In this paper, the focus is on latest generation commercial gate-injection GaN transistors, in the 600 V rating class. Extensive experimental analysis is presented, putting forward an interpretation of the underlying degradation and failure mechanisms, supported by coupled electro-thermal device models, incorporating both the functional and structural characteristics of the devices. The findings highlight a remarkable robustness of a specific type of p-gate GaN HEMTs, referred to as gate injection transistors (GITs), against short-circuit stress, making them a potentially very attractive and competitive technology in the voltage class of relevance.**

Keywords—GaN HEMT; GIT; short-circuit; transient robustness; SOA; repetitive stress; aging.

I. INTRODUCTION

A typical system requirement for semiconductor devices used in power electronic applications is to withstand a short-circuit (SC) event with duration of at least 10 µs, in order to enable detection and perform removal of the faulty operation to prevent catastrophic failure. Also, devices are required to withstand the short-circuit with at least 50% of its nominal breakdown-voltage, although 80% is a more common test condition. In this operational condition, the bias voltage is constant and the current is limited only by the device characteristic. So the event is associated with very consistent power dissipation and heat generation within the semiconductor chip, typically reached already within the 10 µs of very high transient temperature values in the crystal. So, next to the transistors single pulse robustness for prevention of catastrophic failure due to hitting of an excessive temperature value at some critical location within the chip, the aging that they undergo as a result of repetitive stress is also an important aspect of study. In particular, it is important to identify some monitors of degradation to be used as precursors of failure, in the form of measurable variation of some electro-thermal parameters, to enable preventive maintenance and enhanced availability at system level.

Though clearly non-intentional and by definition outside the safe operating area (SOA) of the transistor, short-circuit can be nonetheless a frequent operational condition. Requirements for repetitive pulse withstand capability vary greatly in the application from one domain to another: the minimum can be a few pulses only, the maximum can be well in the several hundreds or thousands. In some applications, no statistics exist whatsoever of the frequency with which the event can occur during the intended operational lifetime of the equipment. The problem has received ample attention in the past for the case of silicon (Si) MOSFETs and IGBTs [1-5]. More recently, the short-circuit performance of silicon-carbide (SiC) MOSFETs has also been investigated, pointing out some specificities and differences with the case of Si transistors [6-8]. In this work the focus is on GaN HEMTs, still largely a developing technology, but one that has been proven already to have significant relevance and application interest in the voltage class 600 V, in particular for a number of upcoming strategic domains, such as electric transport and renewable energies [9, 10]. Next to a higher efficiency and switching frequency, some studies have specifically pointed out the forecast of a higher reliability by replacing Si with GaN due to reduced electro-thermal stress during switching [11]. Specifically, the focus here is on commercial late generation gate injection transistors (GIT) [12], which have been recently shown to possess very interesting features in relation to SC withstand capability [13, 14]. In the following, first the device structure and gate drive requirements are presented; then, the single-pulse short circuit robustness is thoroughly investigated and an interpretation of the observed failure mechanisms is proposed, based on a mix of experimental and simulation study. Finally, repetitive stress

aging is explored, discussing some realistically viable degradation monitors to be used as precursors of failure and proposing an interpretation of the underlying degradation mechanisms.

II. Device Characteristic

The investigated device is a lateral 600 V AlGaN/GaN HEMT, manufactured in a GaN-on-Si substrate technology. A simplified cross-section of the device is depicted in Fig. 1: the device is characterized by the presence of a p-doped AlGaN-layer on a p-gate structure, introduced to ensure enhancement mode operation along with preventing current-collapse phenomena [12]. The current-collapse is prevented by hole-injection from the gate in the on-state, effectively neutralizing electron-trap states. Additionally, a hole-injection close to the drain-contact (hybrid-drain) is provided in the latest device generation to ensure this behavior up to very high bias voltages [15].

Specifically, the device considered here (PGA26E07BA) has nominal current rating of 13 A and is tested as sold, packaged [16]. Fig. 2 reports some key static characteristics of the transistor: a) and b) are the output characteristics at 275 and

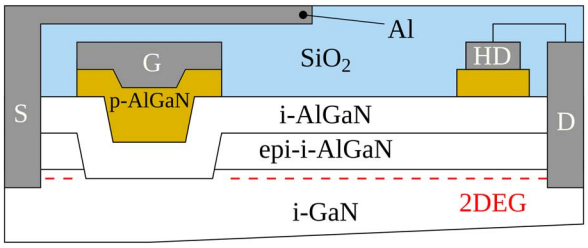


Figure 1: Simplified cross-section of the investigated p-gate GaN HEMT.

400 K, respectively; c) is the on-state resistance as a function of gate-source bias voltage for the two different temperatures; d) is the gate-source p-i junction forward characteristics. From these curves it can be seen that the device is essentially current driven in the linear region, but features a threshold-voltage (knee voltage of the forward bias p-i junction characteristics), below which conduction is immediately reduced. Above threshold, no significant gain in on-state performance is achieved by increasing either gate-source voltage or current, even in response to temperature changes. However, in short-circuit operation, characterized by very large values of applied drain-source voltage, V_{DS}, the value of V_{GS} and correspondingly I_G, are key in determining the drain current value, I_D, and thus the electro-thermal stress associated with the event.

The above discussed transistor characteristics are at the basis of the corresponding gate-driver design, for which a schematic circuit diagram is depicted in Fig. 3. It consists of an isolated gate-driver in conjunction with a network modulating the gate-source voltage and current waveforms, so that: the transistor is turned on and off with some current and voltage overshoot to ensure fast and low dissipative switching, by properly setting the values of R_{RC} and C_{RC}. After switching, the bias current and voltage are reduced to a nominal on-state and

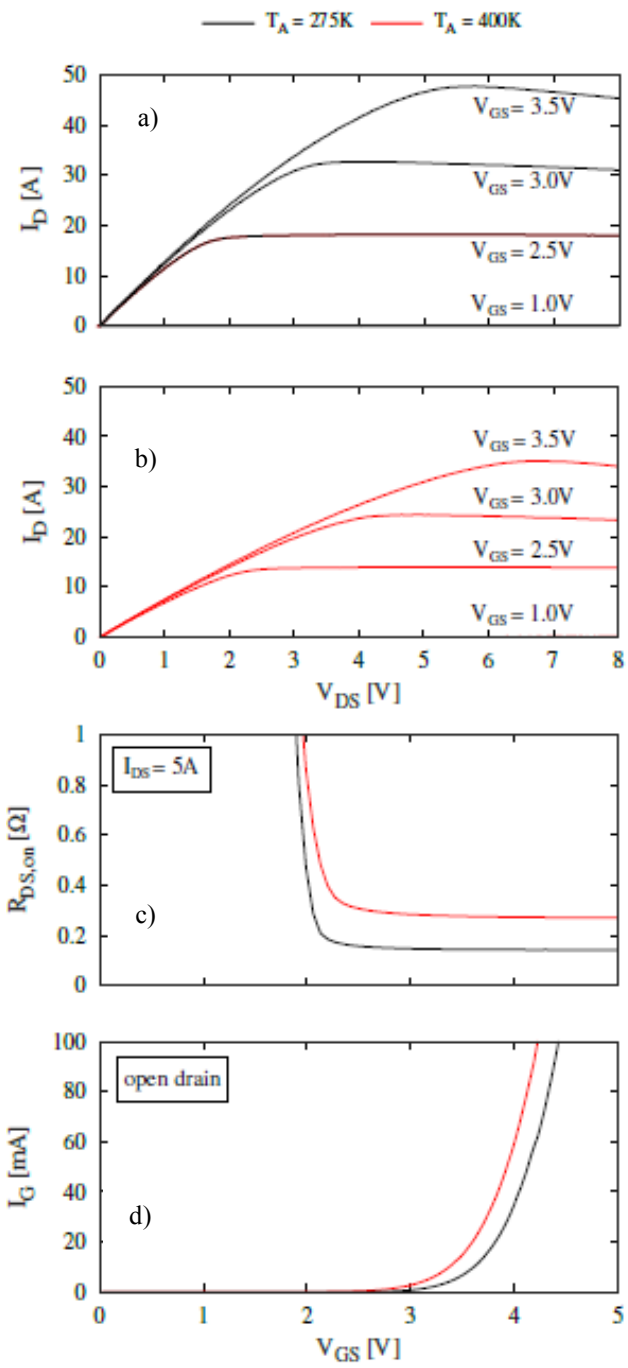


Figure 2 Measured output characteristics at 275 and 400 K, a) and b), respectively; measured on-state resistance at 275 and 400 K, c); measured on-state gate-source *p-n* junction type characteristics at 275 and 400 K, d).

off-state bias level to enable satisfactory on-state performance with minimum power consumption on the gate driver side, by properly choosing the value of R_G.

A representative transient profile of typical V_{GS} is shown in Fig. 4. During the off-state, the device could be well kept off by a constant negative value of V_{GS}. However, recent investigations have clearly shown the need to rapidly return towards zero both to optimize the efficiency associated with current free-wheeling (third-quadrant operation of the

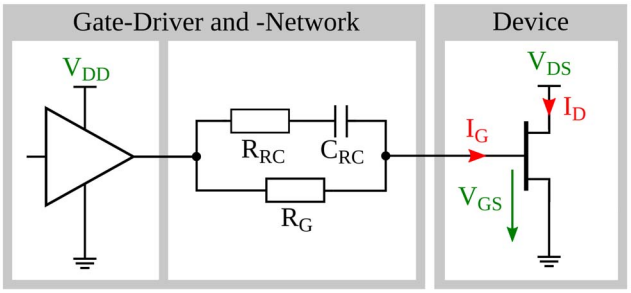


Figure 3: Schematic of the device driver circuit, typically implemented in applications using p-gate HEMTs.

transistor) and with the following turn-on transition [17]. In the negative portion of V_{GS}, the return towards zero can be controlled by the relative values of R_{RC} and C_{RC} or by the insertion of dedicated additional circuitry [18].

Given the above representative driving waveform, the

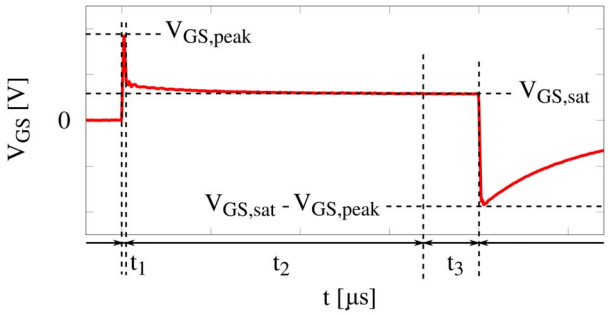


Figure 4: Qualitative transient gate-source voltage profile for optimum transistor switching operation.

corresponding short-circuit I_D profile is as shown in Fig. 5. During the first time interval (t_1) of an SC event, a steep rise of I_D occurs. Here, the slope of I_D is mainly determined by the parasitic inductances of the switching loop along with the applied V_{DS} and the slew-rate of the gate-drive circuit. Since the p-gate structure features a significantly reduced capacitive nature, compared for instance with the MOS structure, the initial V_{GS} value approaches rapidly the maximum, set at the output of the gate driver. Subsequently, as the gate-source junction gets properly forward biased and C_{RC} gets charged, V_{GS} tends towards a saturation value, determined essentially by R_G. Accordingly, I_D tends to decrease in the second time interval (t_2), also as a result of self-heating and electron mobility decrease with temperature [19]. Depending on the particular bias conditions, and assuming the device has not failed earlier, a third time interval (t_3) can be identified, during which the temperature within the device has reached a stationary value and the current saturates to a constant value.

In the following, a parametric study of the influence of bias conditions and gate-driver design options on single pulse short-circuit robustness is presented first. After that, using optimized

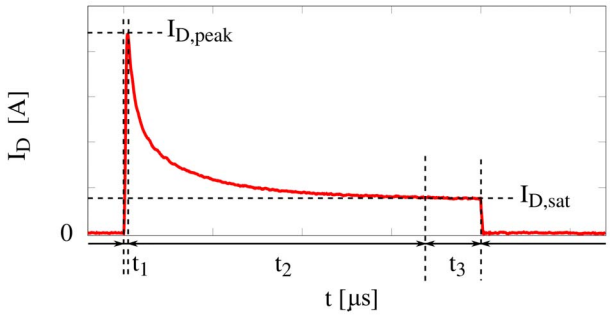


Figure 5: Typical drain-current profile during a short-circuit event.

values of driving network parameters, an extensive test campaign on repetitive stress aging is carried out.

III. Single-Pulse Robustness

Recent studies have shown that the value of $I_{D,peak}$ (see Fig. 5) is crucial in determining the device single pulse robustness and that even extremely high V_{DS} values can be safely tolerated if the gate driver design is modified so as to limit $I_{D,peak}$ below a critical value [14, 18]. In particular, two distinct failure mechanisms have been pointed out: one of a merely electrical nature, tightly related to the value of $I_{D,peak}$ and corresponding to a virtually instantaneous failure of the device; one which is thermally related and intervenes after significant heat generation and time withstand capability. For illustration, Fig. 6 summarizes a series of safely completed short-circuit pulses, for three different values of applied V_{DS}. As can be seen, no significant difference from 270 to 350 V, the device withstands all pulses, whereas an overall decrease in the current level with higher applied voltage occurs. Here, as a result of a greater heat generation rate, the appearance is more pronounced in the saturation value due to the temperature distribution.

On the other hand, Fig. 7 shows the measured drain current for different values of V_{DS} and different values of $I_{D,peak}$, the latter obtained by intervening on the gate-driver circuit components values. As can be seen, in this case the device fails

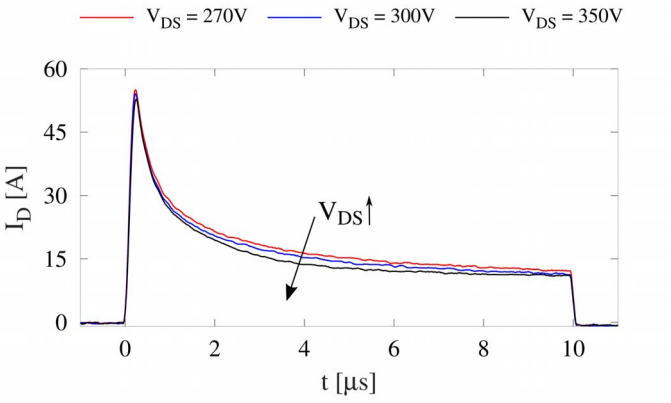


Figure 6. Measured short-circuit current waveform, for three different values of the applied drain-source voltage.

for the lower values of V_{DS} (360 and 450 V, respectively) immediately after the peak in I_D, whereas it is able to withstand the short for a value of V_{DS} as high as 490 V when the value of $I_{D,peak}$ is sufficiently reduced. The failure affected waveforms are not compatible with any significant heat generation and self-heating of the semiconductor chip. The underlying mechanism is interpreted on the basis of purely electrical considerations.

In support of the hypothesis put forward, a detailed functional and structural 3D electro-thermal model of the device was developed. The model features are described in detail in [20]. Fig. 8 shows experimental current and simulated temperature profiles for conditions similar to those discussed in relation to the results of Fig. 7. As expected, the maximum temperature for the case of failure is well below what is achieved when the device withstands the pulse safely, motivating the elaboration of an entirely different interpretation of the failure. In the case of the safe SC, if the power dissipation and heat generation rates are further increased, a critical temperature value is eventually reached, which also leads to destruction of the device.

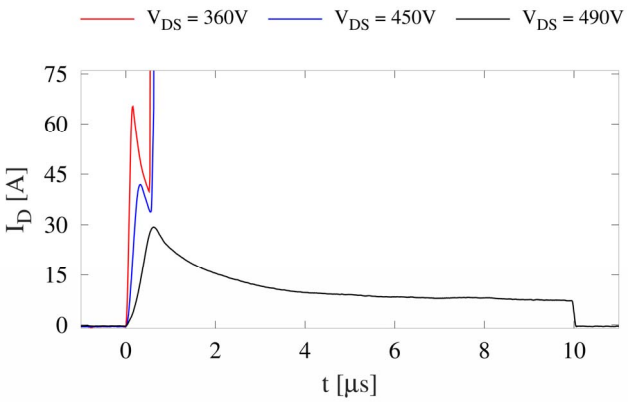


Figure 7. Experimental results, investigating the maximum voltage withstand capability for a defined short-circuit event. The lowest waveform (black) depict a measurement previous to destruction, while the other two show the response for a destructive short-circuit event.

A. Electrical Type of Failure

For the investigation and interpretation of the electrical type of failure, a single pulse measurement is carried out. The short-circuit duration is set to $t_{SC} = 10\,\mu s$ and the applied drain-source voltage is increased, starting from $V_{DS} = 300$ V, in steps of $\Delta V_{DS} = 10$ V until a failure occurs. It is observed that the device is capable to withstand the required minimum duration until a certain voltage ($V_{DS} > 300$ V), at which point a further increase leads within a few hundred nanoseconds to a breakdown in the drain-sour
ce path. As soon as the failure occurs the drain-current (I_D) rises steeply which leads to a catastrophic destruction of the device. Furthermore, as mentioned above, the withstand capability is dependent on the height of the drain-current peak ($I_{D,peak}$), which appears in the early stage of the SC event. Basically, the height of $I_{D,peak}$ can be adjusted by the design of

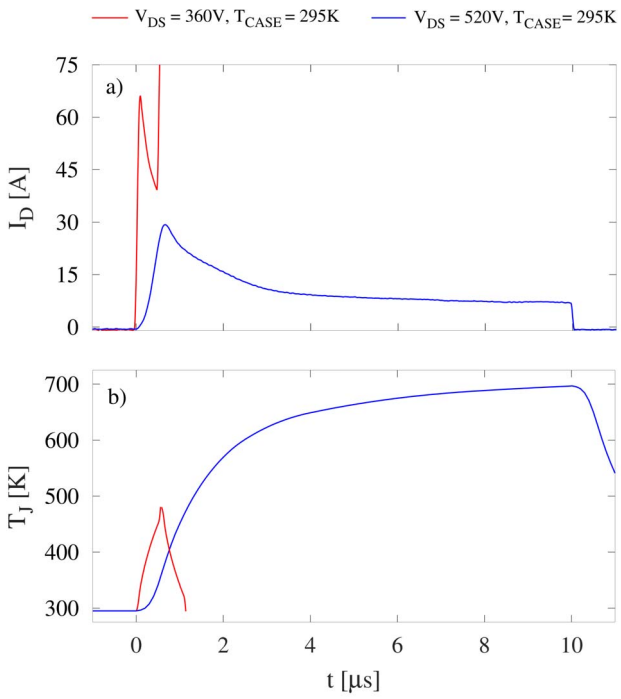


Figure 8. Experimental results of the short-circuit current waveforms, relevant regarding the electrical type of failure (a), along with the simulation results estimating their respective junction-temperature (b).

the gate-drive circuit [13, 14, 18]. When $I_{D,peak}$ is reduced below a given critical value, in the bias conditions described above, no failure is observed anymore.

As a first approximation, it can be considered that the carrier density in the transistor channel influences the magnitude of the electrical field. Indeed, this becomes more of an issue for higher $I_{D,peak}$ as a result of rising carrier densities and local concentrations, respectively. The hypothesis is made that the achievement of a localized critical electric field strength eventually causes avalanche carrier generation leading to an electrical breakdown. Assuming an approximately homogeneous distributed carrier density in the channel, the electrical field peak occurs on the drain-side of the gate-edge due to the applied drain bias during SC (see Fig. 1) [21]. An electrical breakdown through the AlGaN-layer of the gate-structure causes a non-recoverable loss of control leading to catastrophic device failure.

During the SC event, the device structure experiences a superposition of an on- and off-state condition. In the on-state the current flow in the device can be described in accordance to the gate-bias condition (V_{GS}, I_G); the off-state involves the inclusion of the blocking-voltage, V_{DS}. The HEMT structure is, apart from the p-gate, only intrinsic and flooded by the charge carriers during normal operation or short-circuit. So, for determining the electrical field distribution the on-state carrier density needs to be also taken into account in addition to the effect of V_{DS}.

In order to determine the electrical field strength, a physics-based compact model is used. The model predicts the sheet-carrier density in the channel according to the respective surface-potential, based on the fermi-level [22]. With this

approach, the region below the gate, that is, the channel region, can be described quite accurately. For devices used in power electronics applications high breakdown-voltages are required. Therefore, the area between the gate- and drain-terminal (access-region) is typically about an order of magnitude larger than the channel-region, aiming to absorb the blocking-voltage. Since the gate-structure is only able to control the sheet-carrier density of the channel-region, the access-region has a tremendous impact on the accuracy of the electrical field determination.

Assuming a constant threshold of the device, the applied gate-source voltage (V_{GS}) defines the fermi-level and the free states in the channel. According to this, the sheet-carrier density can be adjusted with V_{GS} which defines I_D and $I_{D,peak}$, respectively. The gate-structure of the device forms a Schottky-interface along with a subsequent pin-diode. When a forward gate-bias ($V_{GS} > 0$ V) is applied, the conduction of the pin-diode leads to a current flow through the Schottky-barrier, which is reverse biased. For the determination of the electrical field strength, the additional carriers injected from the gate through the thin AlGaN-layer (epi-i-AlGaN) need to be considered along the concentration in the channel.

So, to also cover the influence of the gate on the overall resulting electrical field, the carrier density associated with the gate current in forward bias is also considered. Fig. 9 shows measured V_{GS} and I_G for different values of the gate driver circuit components. The effect of hole injection into the channel occurs in the p-gate structured HEMT in accordance to [23]. These holes are injected from the p-AlGaN layer into or through the two-dimensional electron-gas (2DEG), when the bias voltage V_{GS} exceeds the bandgap energy of the GaN-layer [24]. Furthermore, it is assumed that the holes accumulate close to the gate-area, as long as they are able to exceed the GaN-bandgap. The amount of accumulated carriers is considered as the injected hole density, indicated as N_h in Fig. 9, which corresponds to the integral of I_G during the overshoot of V_{GS}. The total carrier density, N_{2DEG}, resulting from drain-current along with the injected holes is responsible for the appearance of localized field peaks close to the gate edge.

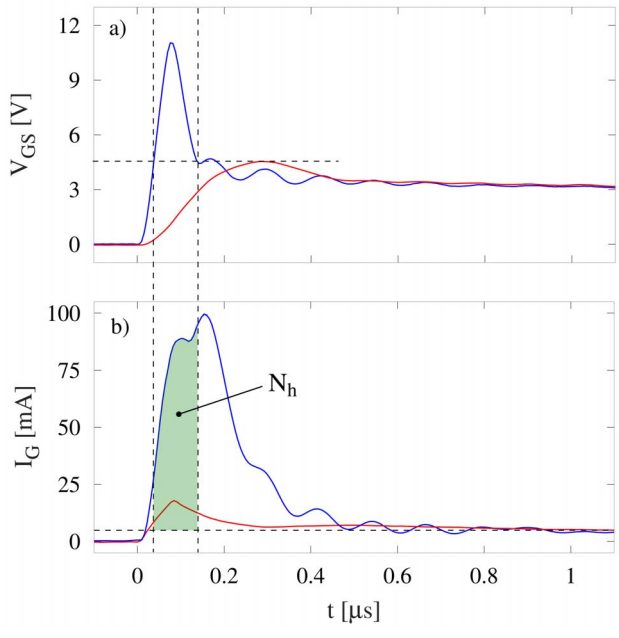


Figure 9. Representative transient waveforms showing experimental results at VDS = 300 V. Here, the gate-source voltage, V_{GS}, waveforms (a) for different parameters of the gate-driver design and corresponding gate-current, I_G, profiles (b).

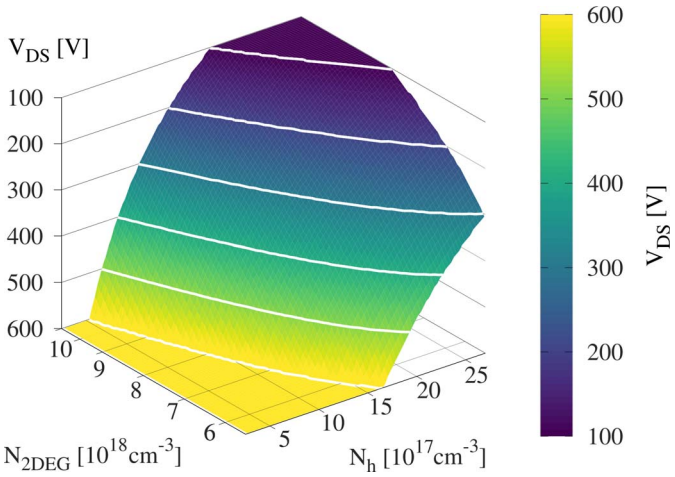


Figure 10. A 3-dimensional view of the short-circuit safe operating area (3D-SCSOA) for p-gate HEMTs. The maximum achievable drain-source voltage (V_{DS}) for the given carrier densities through the channel (N_{2DEG}) and the gate (N_h) are depicted. Furthermore, the dependency of the SCSOA on the gate-bias is shown for V_{GS} = 3.5 V .

In accordance with this interpretation, a short-circuit safe operating area (SCSOA) can be defined, as shown in Fig. 10. The SCSOA defines the maximum achievable V_{DS}, as a function of carrier densities associated to both the drain and gate currents, which obviously depends on the gate-bias voltage (V_{GS}). For the determination of the maximum V_{DS} the reference critical field strength value of AlGaN is used, E_{crit} = 5.5 MV/cm [21]. The parameterization of the model geometric for the SCSOA accord to [12] and has been proven to be valid along the output- and transfer-characteristic of the investigated device. The validity of the formulated SCSOA has been experimentally verified for several measurements under different bias conditions covering a broad range of short-circuit events involving the electrical type of failure.

B. Thermal Type of Failure

For the investigation of the thermal type of failure, a single pulse measurement is carried out similarly to the procedure adopted for the electrical type. In these trials, the occurrence of an electrical failure is avoided by keeping the carrier densities and short-circuit voltage below the critical conditions defined by the SCSOA by intervening on the gate-driver parameters. The failure is determined by applying a short-circuit condition for pulse durations in excess of 300 µs and increasing the device case temperature, T_A, starting from T_A = 295 K, in steps of ΔT_A = 10 K, until a failure occurs. On the other hand, to ensure the integrity of the die attach material, T_A is always kept below 500 K.

Fig. 11 (a) shows results for two slightly different bias conditions: in one case, V_{DS} = 460 V and T_{CASE} = 465 K; in the

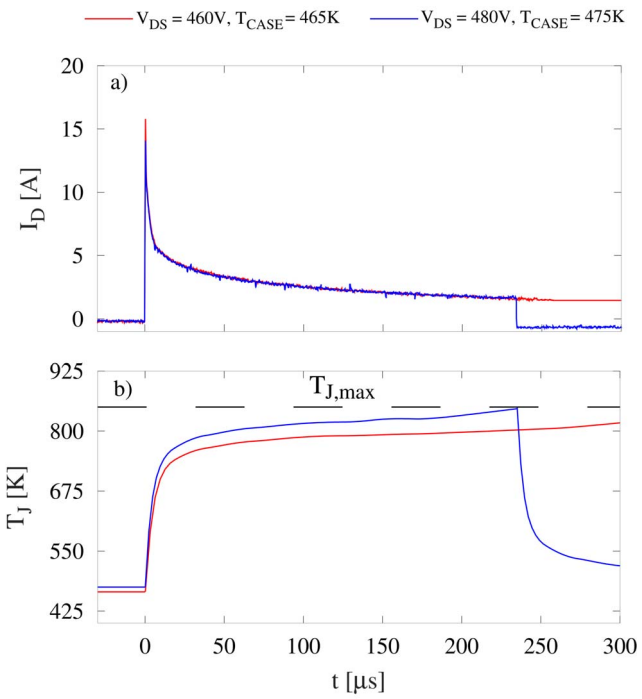


Figure 11. Experimental results showing the drain-current waveforms (a) along with a simulation based estimation of their appropriate junction-temperature (b), in the event of a defined short-circuit condition. The waveforms imply the appearance of the thermal type of failure.

other, V_{DS} = 480 V and T_{CASE} = 475 K. In both cases, the pulse duration is the same, that is, slightly longer than 300 µs, as mentioned above. The appearance of the thermal type of failure is manifest in the waveform with the higher V_{DS} and T_{CASE} values, in the form of a sudden decrease of I_D, prior to the end of the pulse duration, that is, with a positive drive voltage still applied. Although the failure leads to destruction of the device, the appearance and behavior are completely distinct from the case of the electrical failure. In the moment the device fails and the drain-current drops, an increase of the gate-current is registered [14]. The extraordinary increase of I_G causes a corresponding decrease of V_{GS} and the device consequently shuts down. Afterwards, a permanent short of the gate-source path is observed.

This failure may be interpreted as the result of the temperature reaching beyond a critical. The temperature increase corresponding to the applied bias conditions is estimated using the 3D electro-thermal model and is plotted in Fig. 11 (b). On the basis of these results and additional similar tests, the critical temperature value causing a thermal type of failure is determined to be in the range 850 K - 900 K. A critical temperature within this range has also been proven to be significant for Schottky-gate HEMTs [25, 26]. The melting point of aluminum, used as metallization-layer, is about 935 K, also close to the estimated critical temperature.

However, a recent study exploring the thermal limit of GaN power devices showed the failure not to be caused by melting of the metallization [27], but rather by microscopic crack formation in the silicon-dioxide (SiO_2) inter-level dielectric (ILD), with subsequent aluminum extrusion [28]. Mainly localized in sharp edges of diverse material interfaces, high thermo-mechanical overstress is a possible cause of crack formation. The crack tends to grow from the source-sided edge of the gate-metallization towards the source-metallization, consequently piercing the ILD. Since no evidence of either local or plane melt up in the crystallographic structure of the metallization is discovered, the intergrowth of aluminum in the crack is mostly attributed to extrusion. Here, the single pulse overstress condition favors a complete intergrowth of aluminum through the crack, consequently permanent shorting the gate-source path, in alignment with the experimental findings presented.

IV. Repetitive Stress Aging

The aim of aging studies is to investigate cumulative stress effects, which mirror device degradation and potential loss of functionality. Next to the understanding of the device, the interest lies also in the possibility at system level to predict imminent failures and intervene on degraded devices prior to catastrophic failure and loss of system functionality. This helps greatly reduce downtime of equipment and increases system availability, with significantly reduced maintenance effort.

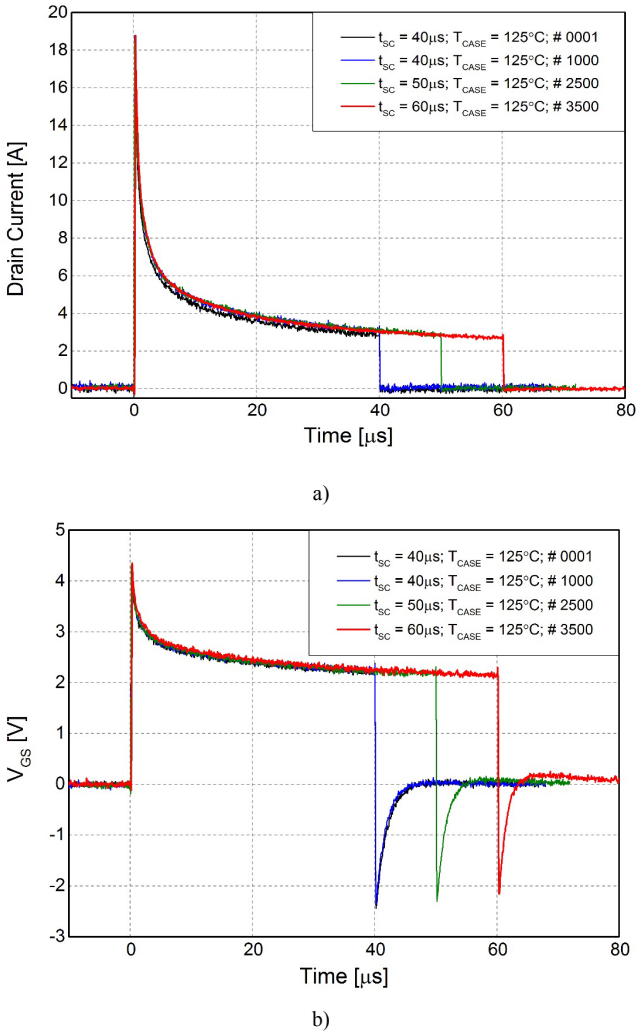
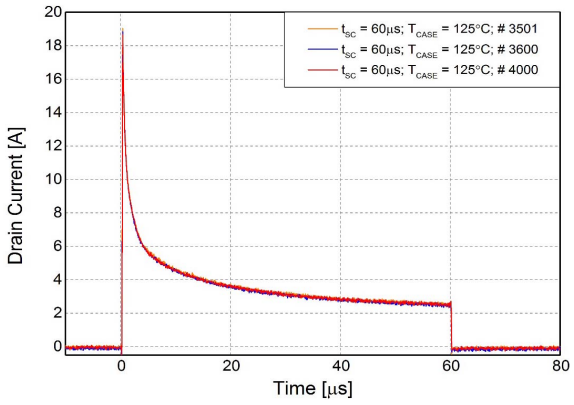
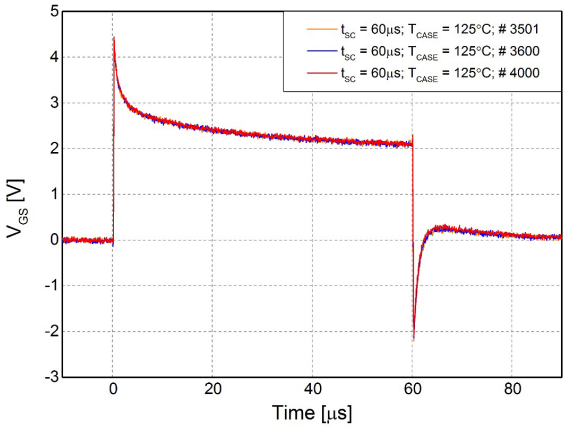


Figure 12. Initial repetitive SC stress aging I_D, a), and V_{GS}, b), profiles.

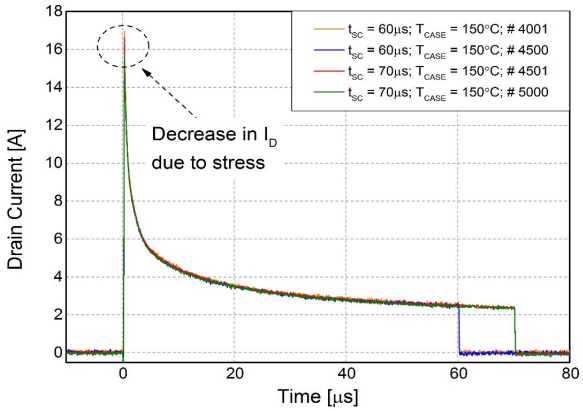


a)



b)

Figure 13. Increased repetitive stress level profiles between 3500 and 4000 pulses.



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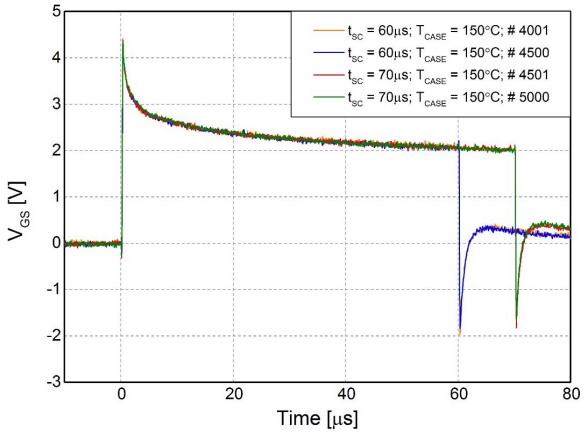


b)

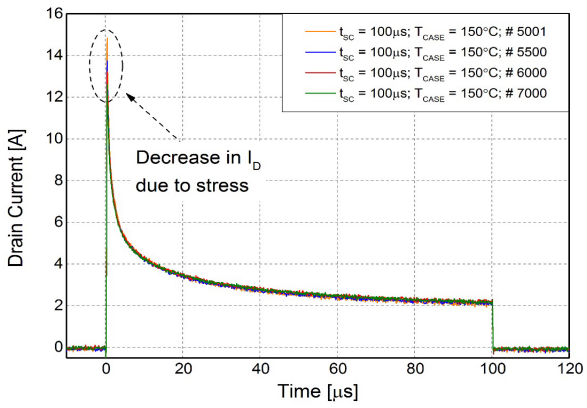
Figure 14. Further increased repetitive stress level profiles between 4000 and 5000 pulses showing first signs of degradation in the form of an $I_{D,peak}$ decrease.

Thus, the goal is not only to highlight degradation mechanisms to design more robust devices in subsequent generations, but also in detecting suitable precursors of failure, which can be used during actual operation within power converters as monitors of the device health.

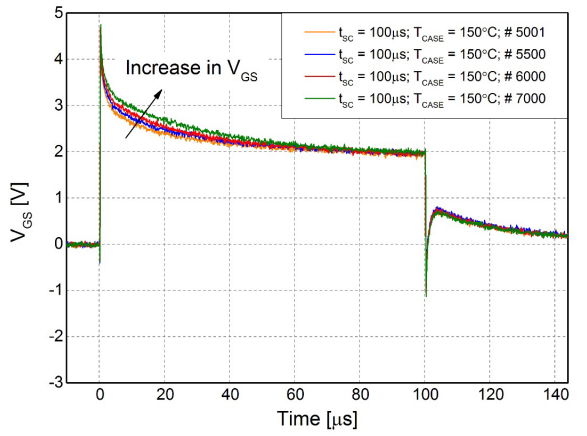
Requirements for repetitive short-circuit withstand capability vary greatly depending on the application, ranging from a few to several thousands. In some applications, no exact statistics of the occurrence of the event exist, making the availability of indirect degradation monitors a great asset. For the envisaged goals, clearly, only the thermal type of failure discussed above is of interest and in particular, with stress levels applied far away from the maximum single pulse withstand capability. Also, a 1 s repetition rate between pulses is chosen to ensure that no temperature build-up effects take place during the tests. To begin with, in this study, realistic bias conditions of existing applications were chosen: Fig. 12 shows the SC current waveform and corresponding V_{GS} for a device biased with V_{DS} = 270 V and T_{CASE} =400 K; initially, the pulse duration was set to 40 µs and progressively increased as no signs of degradation were evident up to over a thousand pulses. In the results of Fig. 13, the pulse duration has been extended to 60 µs and V_{DS} increased to 300 V; where the device still does not show signs of degradation up to 4000 pulses. Beyond that, the temperature was increased to T_{CASE} = 425 K with a pulse duration of 70 µs, wherefore the device showed first signs of changes in its characteristics in between 4500 and 5000 pulses. The corresponding results are shown in Fig. 14 and the mentioned changes are manifest mainly in the form of a slight reduction of $I_{D,peak}$, while the saturation value remain constant, comparing with the observation depicted in Fig. 6.

Further tests were carried out with pulse duration increased to 100 µs, which lead to more pronounced signs of accumulated stress, between 5001 and 7000 pulses, this time not only in the form of a decrease of $I_{D,peak}$, but also in a significant change of the V_{GS} waveform. The results are shown in Fig. 15: the more stressed the device, the higher V_{GS} remains after the initial pulse, indicating a reduction of I_G in the gate-source p-n type forward characteristics and thus some degradation at the level of the gate structure. After 7000 pulses, a sudden failure of the DUT was registered (within the subsequent 2000 pulses), without the possibility to acquire the waveforms at the time of failure.

As shown in Fig. 16, under these bias conditions (last set of experiments), the device temperature was estimated to reach up to 670 K, which is well below the critical temperature identified for single pulse thermal failure. Moreover, the temperature increases in the device very rapidly and reaches a nearly steady-state value already in the first 20 to 30 µs, so that increasing the pulse width further has only very minimum



a)



b)

Figure 15. Repetitive SC stress aging I_D and V_{GS} showing clear signs of degradation between 5000 and 7000 pulses.

impact on the robustness of the device. Recent investigations have shown crack formation with aluminum extrusion for power cycling of Si integrated circuits [29]. In that condition the thermal stress during test was also kept around 50 to 100 K below the maximum limit. Here, the hypothesis is put forward that the observed degradation may be caused by a similar kind of phenomenon: the degradation mechanism bears resemblance to the single pulse thermal type of failure discussed above, but in this case the crack forms and grows gradually as a result of the accumulated stress. A final set of tests carried out on a new device, with V_{DS} = 300 V, T_{CASE} = 425 K and pulse-width varied between 100 and 140 µs, gave signs of pronounced degradation over a set of 9500 pulses. The results are plotted in Fig. 17, zooming in in the initial portions of the pulse, and indicate the same degradation signature as discussed previously, that is, change of the gate-source forward characteristics, with reduction of I_G for a given V_{GS} and corresponding reduction of the $I_{D,peak}$ value.

CONCLUSION

GaN HEMTs of p-gate GIT type have been investigated for their single pulse and repetitive short-circuit robustness. The findings highlight that, subject to the optimization of the gate-driver network design, the devices are extremely robust to this type of overload transient event. The ability to withstand SC

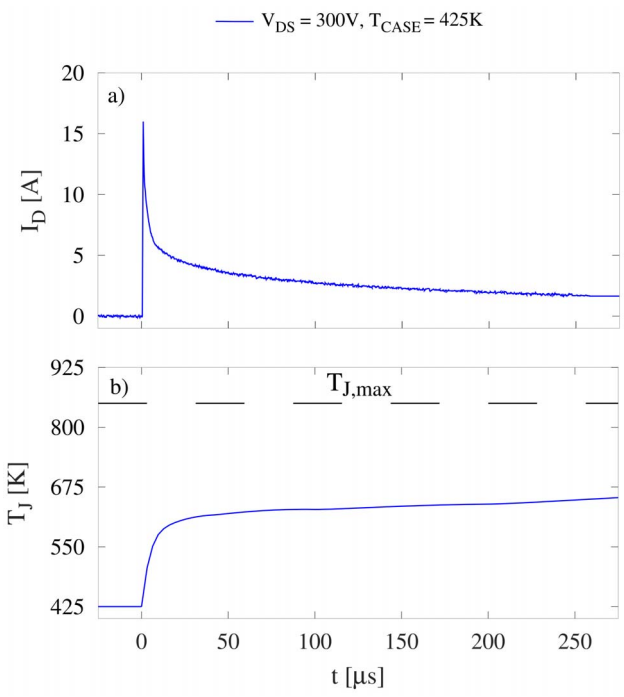
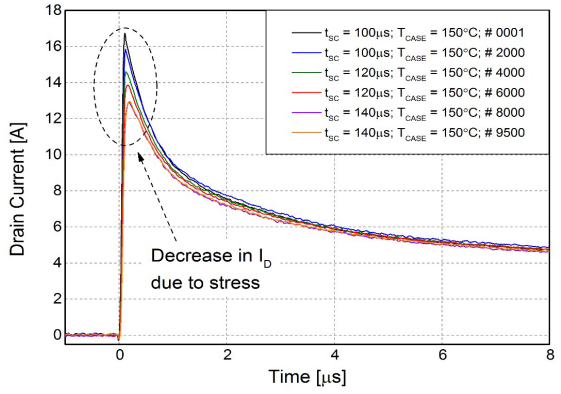


Figure 16. Waveform of the SC test condition (a) as applied in the repetitive stress aging, along with its estimated maximum device temperature profile (b), implicating a reduction of the thermal stress around 200 K.

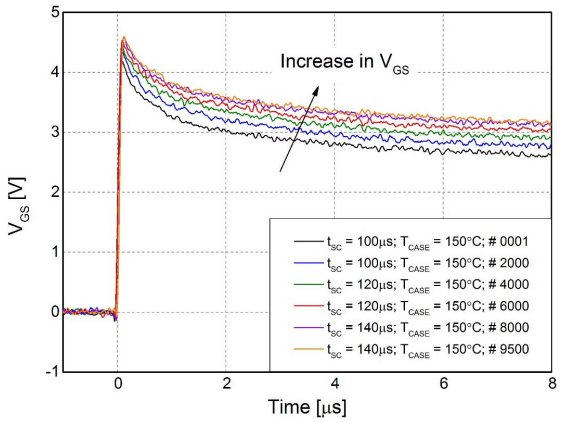
durations largely in excess of few tens of microseconds up to more than 80% of their maximum rated voltage, makes them extremely interesting for a number of large volume applications requiring high robustness towards operation in harsh environments, albeit without resorting to expensive fast failure removal circuits. The results presented here complement a recent set of studies, which have already highlighted the extremely high performance of the technology, which is capable of operating at extremely high frequencies and temperatures, delivering major system level benefits even as a drop-in replacement of established Si alternatives. In the particular voltage class considered here, that is, 600 V, the type of GaN HEMTs under investigation offer a significant edge in SC robustness over counterpart SiC MOSFETs, too.

As regards single pulse robustness, a fully electrical failure mode and a thermal failure mode have been identified. If sort-circuit robustness is required, the device bias conditions need to ensure that no electrical failure intervenes in the very initial portion of the event. The modifications in the gate-driver design required to obtain SC robustness are not in conflict with the need of high switching and on-state performance during nominal system operation. Moreover, dedicated concepts can be developed, which allow for a modification of the gate-driver parameters only upon detection of the occurrence of the short-circuit condition, with minimum additional circuitry to the basic circuit schematic discussed here [18]. As regards thermal failure, two different critical temperature values have been pointed out: a lower threshold around 650 K which is relevant for stress accumulation and damage build-up in repetitive stress and a higher one, around 850 K, which is responsible for immediate device soft failure. The underlying degradation

mechanisms are thought to be related to formations of damage in the gate structure playing a major role.



a)



b)

Figure 17. Repetitive SC stress aging representative waveforms for a second device, stressed from the onset with maximum reached temperatures as estimated to cause degradation. Clear signs of degradation are evident here already in the first few thousand pulses.

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