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TEM studies of multilayer ohmic contacts to n-type AlGaN/GaN

M W Fay, G Moldovan, I Harrison[1], R S Balmer[2], D E J Soley[2], K P Hilton[2], B T Hughes[2], M J Uren[2], T Martin[2] and P D Brown

School of Mechanical, Materials, Manufacturing Engineering and Management, University of Nottingham, University Park, Nottingham NG7 2RD, UK
[1]School of Electrical and Electronic Engineering, University of Nottingham, University Park, Nottingham NG7 2RD, UK
[2]QinetiQ Ltd, St Andrews Rd, Malvern, Worcs WR14 3PS, UK

ABSTRACT: Ti and Pd barrier layers between the Al/Ti diffusion couple and the Au capping layer of multilayer ohmic contacts to n-type AlGaN/GaN field effect transistors were found to be ineffective in preventing the diffusion of Au to the AlGaN following high temperature rapid thermal annealing. The formation of a band of TiN grains at the contact/AlGaN interface is responsible for the activation of the contact. The presence of interfacial Au and threading dislocations are implicated in the formation of additional Ti-nitride inclusions into the AlGaN, although these do not appear to disrupt the Ti-nitride layer at the original contact/nitride interface, nor significantly influence the contact resistance.

1. INTRODUCTION

Devices based on AlGaN/GaN heterostructures are of interest in the area of high power, high frequency applications. For such devices to become commercially viable, ohmic contacts must fulfil the requirements of reproducibility, low resistance and good thermal and mechanical stability.

The standard Al/Ti diffusion couple may be used to contact n-type AlGaN/GaN. As Al and Ti layers are both susceptible to oxidation Au is then used as an oxidation resistant capping layer. The Au also acts to planarise the contact and thereby assist with wire bonding. The large number of variables that affect the characteristics of a metal diffusion couple contact, not least the nature of the nitride wafer complicates the comparison of results published in the literature. However, it was considered undesirable to have Au diffusing to the contact/nitride interface, hence diffusion barrier layers were incorporated into the Au/*x*/Al/Ti contact scheme where *x* corresponds to materials such as Ti, Pd, Ni or Pt. [Fan *et al* 1996, Cai *et al* 1998, Mohammad *et al* 1996, Chor *et al* 2001]. While the mechanism of interfacial reaction to form a Ti-nitride and a nitrogen depletion layer at the AlGaN surface to activate the contact is now accepted, a full understanding of the role of all the materials used within such multilayer contacts is not yet complete. TEM investigations have indicated that such barrier layers are ineffective at preventing the diffusion of Au through to the semiconductor under the condition of rapid thermal annealing needed to activate the contact. The choice of diffusion barrier elements and thickness appears to affect the optimum Ti:Al diffusion couple ratio which may be used. It is also suggested that the presence of Au at the contact/AlGaN interface may not actually be detrimental [Bright *et al* 2001].

In this work, complementary TEM techniques have been used to investigate the effect of varying the metallic layer construction, the annealing temperature, and the substrate on which the nitride layers are grown, on the development of the contact microstructure and the evolution of the contact/nitride interface in particular.

2. EXPERIMENTAL DETAILS

Three contact schemes to AlGaN/GaN are appraised, typical of multilayer contacts reported in the literature. Firstly, a 300nm Au / 60nm Ti / 100nm Al / 20nm Ti contact to AlGaN/GaN grown by metal organic chemical vapour deposition (MOCVD) on an (0001) oriented sapphire substrate, rapid thermal annealed (RTA) at temperatures from 650 to 950°C. Secondly, a 100nm Au / 100nm Pd / 160nm Al / x nm Ti contact scheme, where x is 30, 60, 100 or 160nm, to an AlGaN/GaN/sapphire sample, RTA at 950°C. Thirdly, a 100nm Au / x nm Al (x = 60 or 100nm) / 20nm Ti contact scheme without a diffusion barrier to AlGaN/GaN/SiC, RTA at 950°C.

Characterisation was performed using a Jeol JEM-2010F field emission gun TEM operating at 200keV equipped with a Gatan Imaging Filter (GIF) and an Oxford Instruments Energy Dispersive X-Ray (EDX) detection system, and a Jeol-4000FX operating at 400keV equipped with a GIF.

3. RESULTS AND DISCUSSION

Ohmic characteristics for the various contact schemes are presented in Table 1. The AuTiAlTi samples become ohmic after annealing at 750°C, with the optimum performance achieved by ~850°C. For the AuPdAlTi contacts, an anneal of 850°C is required before the onset of ohmic behaviour, while the schemes with thinner Ti layers require an anneal temperature of 950°C to achieve optimum performance.

Annealing Temp	R_C (Ω-mm)						
	AuTiAlTi	AuPdAlTi				AuAlTi	
		30nm Ti	60nm Ti	100nm Ti	160nm Ti	60nm Al	100nm Al
650°C	not ohmic	not ohmic	not ohmic	not ohmic	not ohmic	-	-
750°C	18.5	not ohmic	not ohmic	not ohmic	not ohmic	-	-
850°C	3.44	12.45	not ohmic	1.54	2.83	-	-
950°C	3.2	1.86	2.73	2.86	1.35	0.82	0.84

Table 1 – Contact resistance as a function of annealing temperature and deposited layer composition. Ohmic characteristics for AuAlTi contacts were only measured after RTA at 950°C.

TEM images of all the contacted samples annealed at 950°C show similar features, as illustrated by Fig. 1. The original metal layers have significantly intermixed. A thin ~10nm wide layer, largely comprised of TiN grains of 5-10nm diameter is always identified in samples that show ohmic behaviour, centred on the original contact/nitride interface. TiN inclusions into the AlGaN are observed, and these are associated with the presence of emerging threading dislocations. In the absence of inclusions the surface of the AlGaN layer is uniformly consumed to a depth of ~5nm by the formation of the TiN band. Increasing the thickness of the original interfacial Ti layer within a contact scheme is associated with an increase in the size of the inclusions, but this does not appear to alter the position, width, or composition of the TiN band initially formed. Samples with low levels of interfacial Ti and/or low dislocation densities exhibit isolated inclusions after annealing at 950°C, with the AlGaN/GaN layer remaining intact on either side (Fig. 2a). With increasing thickness of interfacial Ti, the inclusions eventually merge to form a diffusion front parallel to the original contact/nitride interface (Fig 2b). Inclusions of varying sizes and densities were observed in all the samples annealed at 950°C, but were not observed in any of the samples annealed at 850°C.

The TiN inclusions are related to the location of threading dislocations and associated with the presence of interfacial Au/Al. Elemental analysis by both EDX (Fig. 3) and Energy Filtered TEM indicates that the inclusions have a thin Al/Au metallurgical layer separating them from the GaN. Elemental analysis also indicates that Au is present at the contact/nitride interface in all the samples that show ohmic behaviour (Fay *et al* 2002). Furthermore, there is no discernible difference in the interfacial concentration of Au between samples with and without a diffusion barrier layer.

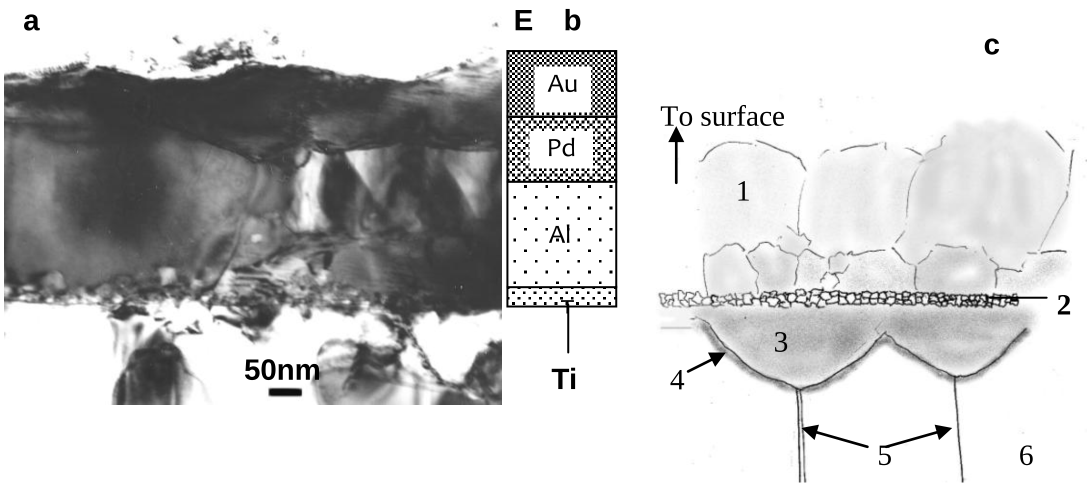

Fig. 1 (a) Bright field image showing an AuPdAlTi (30nm Ti) contact annealed at 950°C. The original metal layers have intermixed significantly. Small grains can be observed at the interface with the nitride layer. The schematics show (b) the pre-anneal layer thicknesses to the same scale, and (c) the post anneal structure, illustrating (1) intermetallic grains; (2) TiN rich layer at the original contact/nitride interface; (3) TiN inclusions; (4) an Al/Au rich interfacial region; (5) threading dislocations; and (6) GaN.

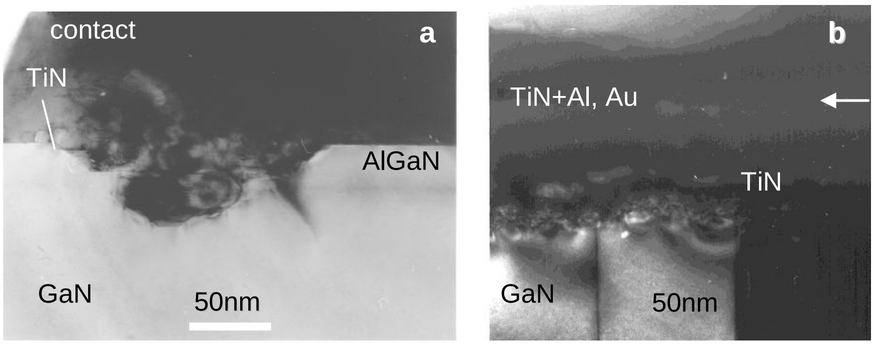

Fig 2 AuPdAlTi contacts annealed at 950°C: (a) 30nm Ti thickness and (b) 160nm Ti thickness. The AlGaN layer remains largely intact in the sample with the thinnest interfacial Ti layer. Increasing the Ti layer thickness results in the complete consumption of the AlGaN layer and GaN to the depth of ~100nm. A thin TiN layer is identified at the original contact/nitride interface in both samples, arrowed in (b).

These combined results indicate that the inclusions have no discernible effect on the electrical characteristics of the contact. Hence it can be concluded that such structures are not necessary, nor detrimental, for ohmic behaviour. Although thicker interfacial Ti layers are required to produce ohmic behaviour at 850°C for the AuPdAlTi scheme, annealing temperatures of 950°C only require an interfacial Ti layer of 20nm at most. It is clear that use of Ti as a barrier layer somewhat complicates the development of the contact. It is evident from the size of inclusions formed beneath the AuTiAlTi contacts annealed at 950°C that much of the diffusion barrier layer Ti has gone to form TiN in the inclusions. Nevertheless, AuTiAlTi contacts became ohmic at lower temperatures than the AuPdAlTi contact containing similar amounts of Ti in the overall scheme. This suggests that the Pd diffusion barrier does inhibit the evolution of the contact scheme to some extent. Finally, the variation in Al content does not appear to have had a significant effect on the development on the contact ohmic behaviour.

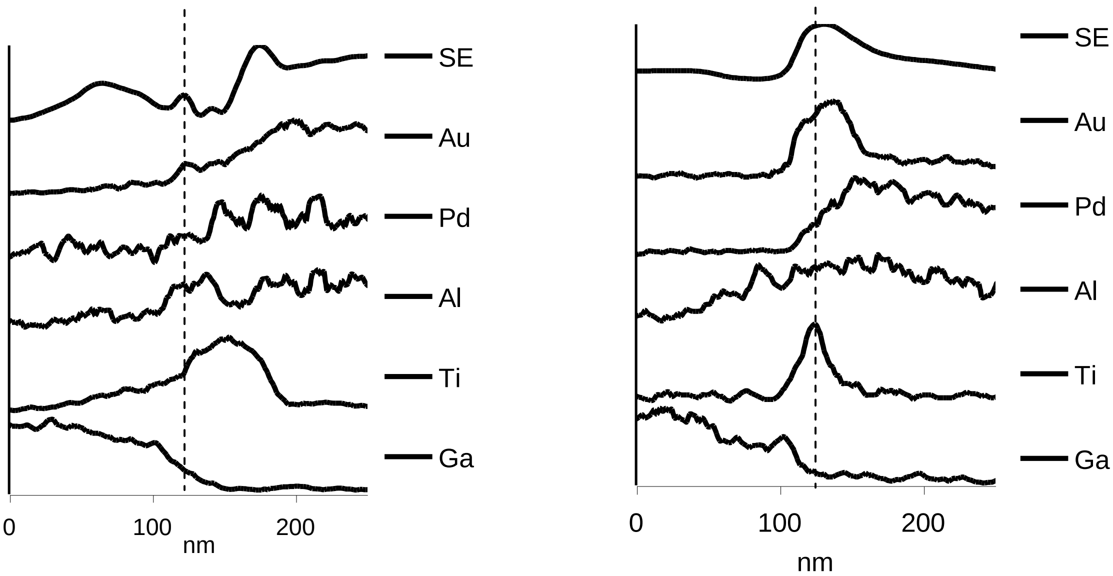

Fig 3 – Typical EDX profiles obtained from AuPdAlTi contacted samples showing ohmic behaviour across an interfacial region with (a) inclusions and (b) no inclusions. The presence of Au at the contact/nitride interface in both profiles demonstrates that the Pd layer does not present a diffusion barrier to Au at a temperature of 950°C. A thin Al and Au layer can be observed at the boundary of the Ti-rich inclusion and the GaN layer, indicated by the dashed line in (a). Au is also clearly present at the contact/nitride interface in regions with no inclusions (b)

4. SUMMARY

The onset of ohmic behaviour of AuTiAlTi and AuPdAlTi diffusion couple contacts to n-type AlGaN/GaN is related to the formation of a thin TiN band at the original contact/nitride interface, which is not disrupted by the formation of additional Ti-nitride inclusions into the AlGaN. Thin (~20nm) Ti layers are adequate to produce an ohmic contact at annealing temperatures of 950°C, while thicker Ti layers are required at lower annealing temperatures. Pd and Ti barrier layers do not prevent the diffusion of Au to the contact nitride interface, although Pd is slightly more effective as a diffusion barrier. Although the presence of Au/Al is implicated in the formation of the Ti-nitride inclusions, electrical characterisation indicates that such inclusions have no discernible effect on the device contact resistance.

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