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## Analysis and implementation of power management and control strategy for six-phase multilevel ac drive system in fault condition



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### ABSTRACT

This research article exploits the power management algorithm in post-fault conditions for a six-phase (quad) multilevel inverter. The drive circuit consists of four 2-level, three-phase voltage source inverter (VSI) supplying a six-phase open-end windings motor or/impedance load, with circumstantial failure of one VSI investigated. A simplified level-shifted pulse-width modulation (PWM) algorithm is developed to modulate each couple of three-phase VSI as 3-level output voltage generators in normal operation. The total power of the whole ac drive is shared equally among the four isolated DC sources. The developed post-fault algorithm is applied when there is a fault by one VSI and the load is fed from the remaining three healthy VSIs. In faulty conditions the multilevel outputs are reduced from 3-level to 2-level, but still the system propagates with degraded power. Numerical simulation modelling and experimental tests have been carried out with proposed post-fault control algorithm with three-phase open-end (asymmetrical induction motor/R-L impedance) load. A complete set of simulation and experimental results provided in this paper shows close agreement with the developed theoretical background.

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### 1. Introduction

AC power converters are affected by mechanical, thermal, and electrical stresses. These stresses lead to component and system failures [1,2]. Failures include DC-link capacitors, voltage sensors, semiconductor switches and control/gate driver circuits [3–6]. Hence, fault tolerance is mandatory in ac drives power conversion, which ensures fault detection, localization and isolation, allowing continuous propagation [7–10]. Recently, the multi-phase ac machines proved their arrival by the redundancy in configuration, system reliability, and fault tolerance [11–15]. Further, for multiphase ac motor, a minimum of two phases are sufficient to create a rotating field under circumstances when all other phases have failed [11,13].

Multilevel inverters are the prominent alternatives for classical three-phase VSI [16,17], but still the reliability remains lower which is the major drawback [18,19]. Still, the classical three-phase VSI

remains the most reliable choice, hence by properly arranging the multiple VSIs, both multi-phase [20,21] and multilevel configuration can be easily constructed [15,22–24].

A novel ac drive structure for six-phase (asymmetrical) open-end winding asymmetric induction machine is proposed with the capability to generate multilevel outputs [25]. But the PWM strategies are adopted by the complex space vector modulation (SVM) by the nearest three-vector approach to generate multilevel output voltages and complex to implement with real time digital signal processors (dsps). In this research paper, the same ac drive configuration is exploited for the developed post-fault condition with a simplified multi-level (level-shifted PWM) modulation applied to regulate each pair of 2-level VSIs to behave similarly to 3-level outputs. Moreover, the PWM scheme is easy to implement in industrial standard dsp [25,26].

The power circuit consists of four standard 2-level VSIs with four isolated DC sources and hence, the system is absolutely free of zero-sequence components as shown in Fig. 1(a). Equivalent circuit in terms of the three-phase space vectors are shown in Fig. 1(b). Benefit of the topology includes the reduction of construction cost by its conventional structure; high reliability and reduced total harmonic

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distortion (THD) with lower  $dv/dt$  at the outputs; and the reduction of stress in the switches. In particular, topology is a viable solution for the applicability of multiphase-phase ac motor/generator (6-phase, 9-phase, etc.) and renewable energy systems integration for more electric aircraft systems and high-power utilities [12].

Complete ac drive system along the post-fault control strategy algorithm with simplified multilevel PWM scheme is numerically modelled in Matlab/PLECS simulation software. For experimental verifications, the hardware prototype version is implemented with two dsp TMS320F2812 processors and impedance load in open-winding configuration. Set of simulation and experimental results are provided in this paper under different designed testing conditions. Both the simulation and experimental results are always shown in close agreement with developed theoretical background.

This paper is organized as follows: analysis of asymmetrical six-phase open-winding induction motor drive circuit is illustrated in section 2; simplified level-shifted multilevel modulation along with theoretical background and power sharing principles are discussed in section 3; designed post-fault control strategies and predictions are elaborated with theoretical developments in section 4; numerical simulation and experimental implementation results are described with theoretical validation in section 5. Finally, section 6 concludes this research investigation.

## 2. Analysis of the proposed asymmetrical, six-phase, open-winding induction motor drive

Fig. 1(a) shows the dual three-phase (six-phase asymmetrical) open-winding induction motor fed from four three-phase VSIs with isolated DC sources. Fig. 2(a) correspondingly represents the orthogonal rotating multiple space vectors equivalent circuit [21,27,28]. Complete behavior of the dual three-phase induction machine can be written in stationary reference frames as:

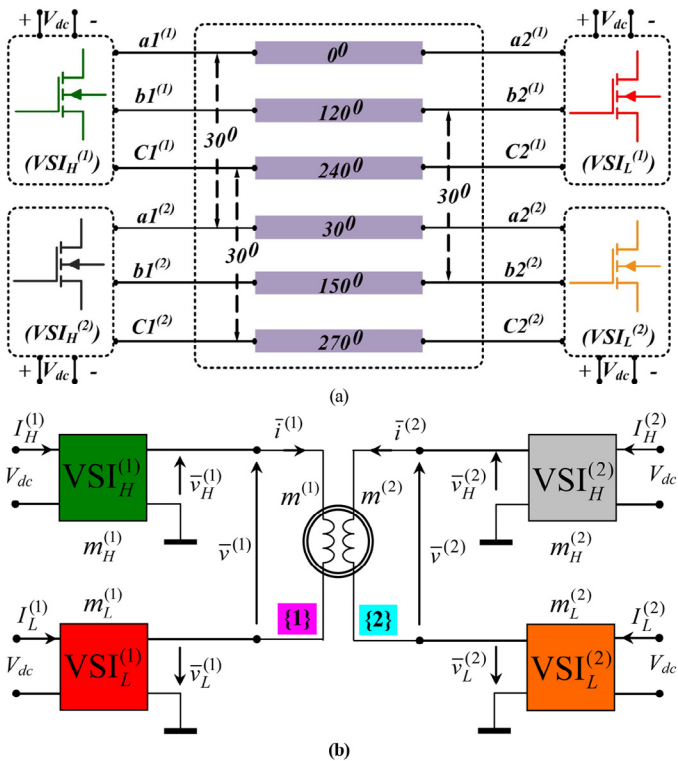


Fig. 1. (a) Investigated configuration of six-phase (quad) asymmetrical open-end windings ac drive. (b) Equivalent three-phase space vectors circuit. (Healthy state.)

$$\bar{v}_{S1} = R_S \bar{i}_{S1} + \frac{d\bar{\varphi}_{S1}}{dt}, \bar{\varphi}_{S1} = L_{S1} \bar{i}_{S1} + M_1 \bar{i}_{R1} \quad (1)$$

$$0 = R_R \bar{i}_{R1} - j\omega_m \bar{\varphi}_{R1} + \frac{d\bar{\varphi}_{R1}}{dt}, \bar{\varphi}_{R1} = M_1 \bar{i}_{S1} + L_{R1} \bar{i}_{R1} \quad (2)$$

$$\bar{v}_{S5} = R_S \bar{i}_{S5} + \frac{d\bar{\varphi}_{S5}}{dt}, \bar{\varphi}_{S5} = L_{S5} \bar{i}_{S5} \quad (3)$$

$$T = 3pM_1 \bar{i}_{S1} \cdot j \bar{i}_{R1} \quad (4)$$

Since all DC sources are isolated, it is understood that the proposed system is free of zero-sequence components. Now, the total power  $P$  of the ac motor can be written as the sum of power of the two three-phase open-windings  $P^{(1)}$ -{1} and  $P^{(2)}$ -{2} as [25]:

$$\begin{cases} P^{(1)} = \frac{3}{2} \bar{v}^{(1)} \cdot \bar{i}^{(1)} \\ P^{(2)} = \frac{3}{2} \bar{v}^{(2)} \cdot \bar{i}^{(2)} \end{cases}, \quad (5)$$

$$P = P^{(1)} + P^{(2)} = \frac{3}{2} [(\bar{v}_H^{(1)} + \bar{v}_L^{(1)}) \cdot \bar{i}^{(1)} + (\bar{v}_H^{(2)} + \bar{v}_L^{(2)}) \cdot \bar{i}^{(2)}] \quad (6)$$

The stator windings voltages  $\bar{v}^{(1)}$  and  $\bar{v}^{(2)}$  are the sum of individual inverter voltages ( $VSI_H^{(1)}$ ,  $VSI_L^{(1)}$  and  $VSI_H^{(2)}$ ,  $VSI_L^{(2)}$ ), expressed as:

$$\begin{cases} \bar{v}^{(1)} = \bar{v}_H^{(1)} + \bar{v}_L^{(1)} \\ \bar{v}^{(2)} = \bar{v}_H^{(2)} + \bar{v}_L^{(2)} \end{cases} \quad (7)$$

There are three degrees of freedom, which allows the total power to be shared equally between the two three-phase open-end windings [25]. By first degree of freedom  $k_i$ , sharing of power (current) between two three-windings {1} and {2} is predicted as follows:

$$\begin{cases} \bar{i}^{(1)} = 2k_i \bar{i}_{S1} \\ \bar{i}^{(2)} = 2\alpha^{-1}(1-k_i) \bar{i}_{S1} \end{cases} \quad (8)$$

$$\begin{cases} P^{(1)} = P_H^{(1)} + P_L^{(1)} \equiv k_i P \\ P^{(2)} = P_H^{(2)} + P_L^{(2)} \equiv (1-k_i) P \end{cases} \quad (9)$$

By second  $k_v^{(1)}$  and third  $k_v^{(2)}$  the degree of freedom that allows the sharing of power (voltages) between the inverters ( $VSI_H^{(1)}$  and  $VSI_L^{(1)}$ ) and ( $VSI_H^{(2)}$  and  $VSI_L^{(2)}$ ) of windings {1} and {2} is predicted as follows:

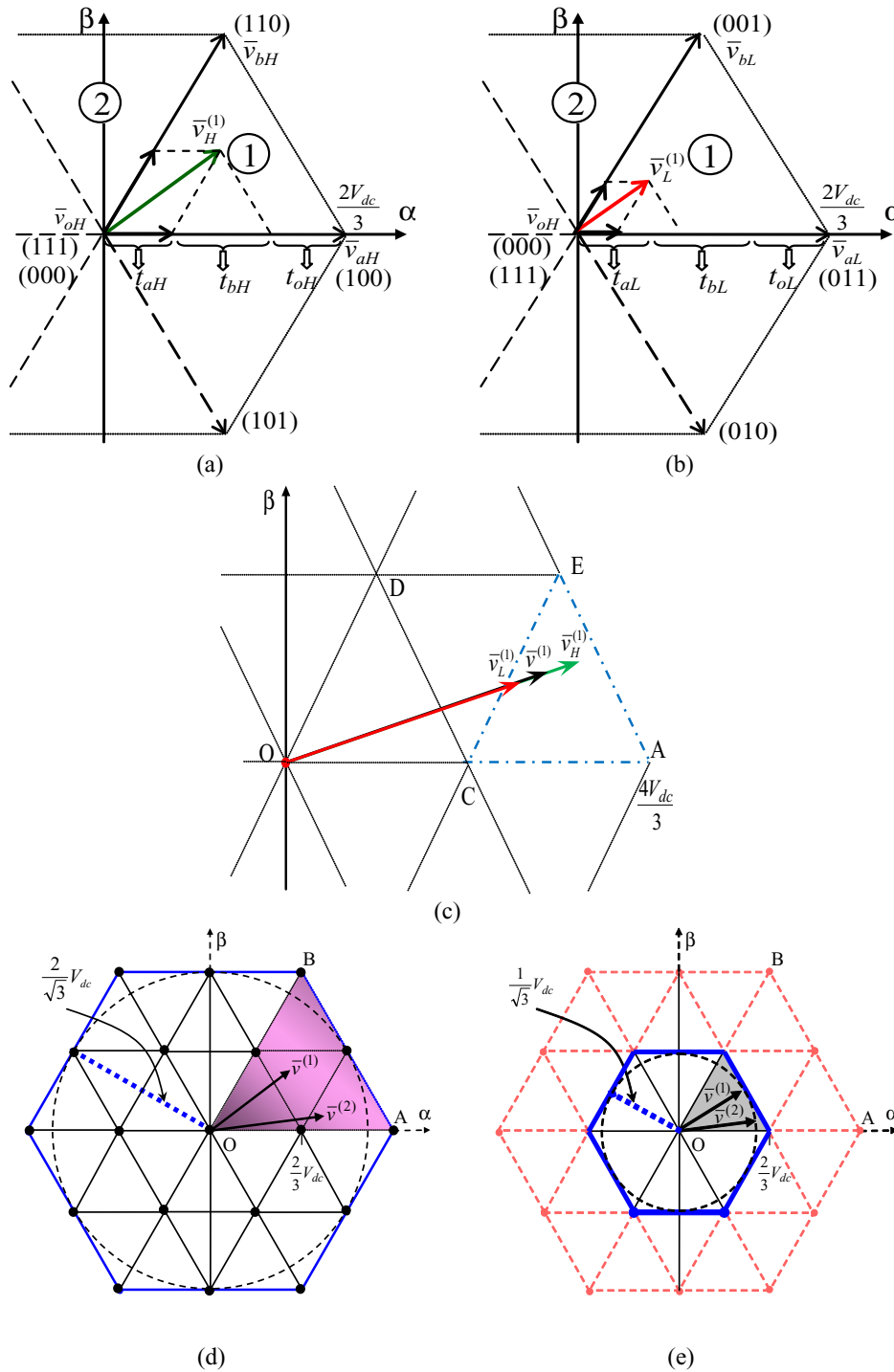
$$\begin{cases} \bar{v}_H^{(1)} = k_v^{(1)} \bar{v}^{(1)} & \bar{v}_H^{(2)} = k_v^{(2)} \bar{v}^{(2)} \\ \bar{v}_L^{(1)} = (1-k_v^{(1)}) \bar{v}^{(1)} & \bar{v}_L^{(2)} = (1-k_v^{(2)}) \bar{v}^{(2)} \end{cases} \quad (10)$$

$$\begin{cases} P_H^{(1)} = k_v^{(1)} P^{(1)} & P_H^{(2)} = k_v^{(2)} P^{(2)} \\ P_L^{(1)} = (1-k_v^{(1)}) P^{(1)} & P_L^{(2)} = (1-k_v^{(2)}) P^{(2)} \end{cases} \quad (11)$$

Hence, the total power can be equally shared among the four VSIs which lead to 25% power demand from each VSI.

## 3. The PWM modulation strategy for the quad-inverter ac drive system

In order to synthesize the reference voltage vectors  $\bar{v}^{(1)}$  and  $\bar{v}^{(2)}$ , proper multilevel PWM algorithm is required to modulate each couple of VSIs and also to satisfy the power sharing between the two windings [29–31], where techniques that suffer by zero-sequence components require compensation in the PWM strategy.



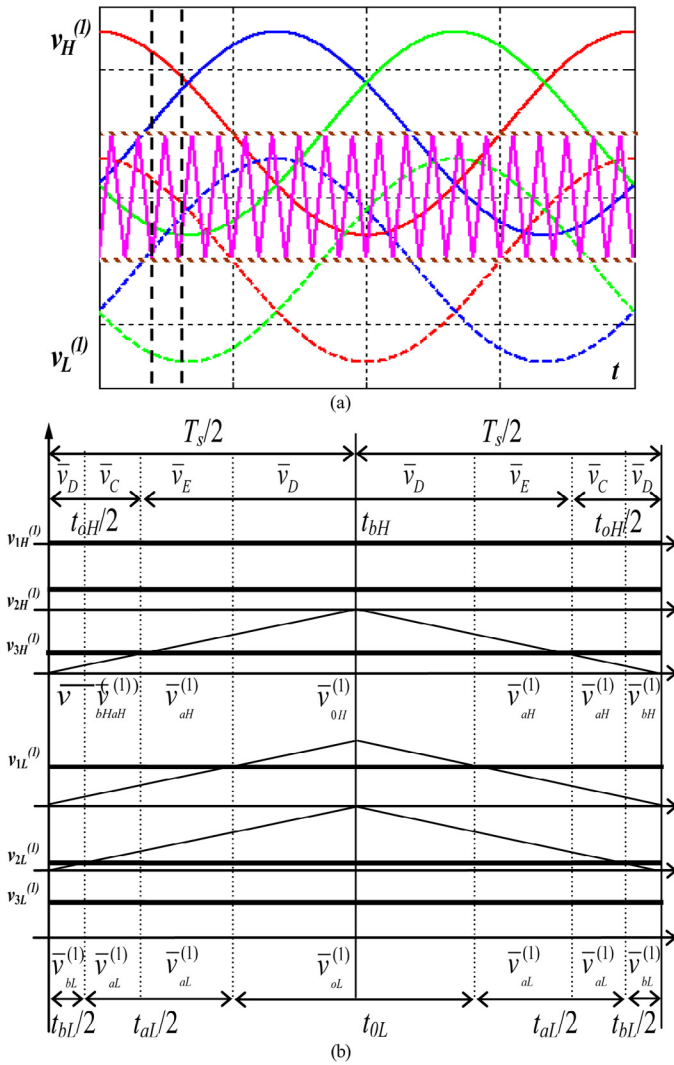
**Fig. 2.** Space vector representation for VSIs of two three-phase open windings {1} and {2}: (a) Inverter  $VSI_H^{(1)}$ , (b) Inverter  $VSI_L^{(1)}$ , (c) Power sharing between inverter  $VSI_H^{(1)}$  and  $VSI_L^{(1)}$  voltage-level generated space vectors for the three-phase open-end two windings {1} and {2} under (d) healthy state, (e) one inverter faulty state.

An approach followed in Reference 32 provides proper multilevel operation and good power sharing with two VSIs but adopted complex space vector approach. Hence multilevel operation with proper sharing can be easily generated by simplified level-shifted modulation scheme.

The voltage reference vectors  $\bar{v}^{(1)}$  and  $\bar{v}^{(2)}$  corresponds to the output voltages of two three-phase windings given by Eq. 7. By inverse three-phase space vector decomposition approach, the reference voltage space vector of the two windings is determined as [25]:

$$\begin{cases} \bar{v}^{(1)} = \bar{v}_{S1,ref} + \bar{v}_{S5,ref}^* \\ \bar{v}^{(2)} = \alpha^{-1}(\bar{v}_{S1,ref} + \bar{v}_{S5,ref}^*) \end{cases} \quad (12)$$

Eq. 4 is synthesized using independent three-phase space vectors as shown in Fig. 2(a) and (b) for inverters ( $VSI_H^{(1)}$ ,  $VSI_L^{(1)}$ ) and the same applies to inverters ( $VSI_H^{(2)}$ ,  $VSI_L^{(2)}$ ). In balanced operation, the sinusoidal voltages space vector  $\bar{v}_{S1,ref}$  determines the voltage limits, with the condition  $\bar{v}_{S3,ref} = \bar{v}_{S5,ref} = 0$  leading to the following voltage space vectors for the two sets of open-winding:

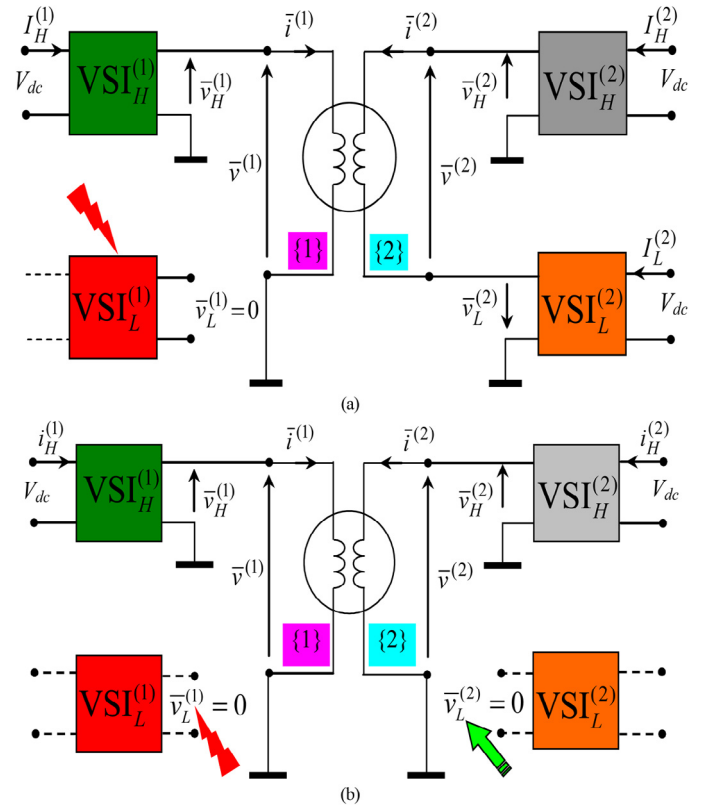


**Fig. 3.** Level-shifted multilevel modulation scheme for inverters  $VSI_H^{(1)}$  (normal line) and  $VSI_L^{(1)}$  (dotted line): (a) modulation signals for the three-phase open-winding {1}, (b) switching pattern.

$$\begin{cases} \bar{v}^{(1)} = \bar{v}_{S1,ref} \\ \bar{v}^{(2)} = \alpha^{-1} \cdot \bar{v}_{S1,ref} \end{cases} \quad (13)$$

In Fig. 2(d), regular hexagon gives voltage limitation of each VSI by the space vectors. For sinusoidal balanced voltages operation, the voltage limit is restricted to  $2/\sqrt{3} V_{dc}$ , with the outer circle radius shown in Fig. 2(d). By the symmetry of the triangles, the analysis can be limited to triangle OAB (shaded area) [32]. The sharing principle is shown in Fig. 2(c) for proper power sharing with multilevel waveforms.

Level-shifted pulse width modulation (PWM) is a well known scheme which can be used in all types of multilevel inverters. For  $l$ -levels there are  $(l-1)$  carriers shifted by  $l/(l-1)V_{dc}$ . Fig. 3(a) shows a common single carrier and this carrier is compared with each modulating signals for use in the corresponding part of the multilevel inverter. Implementation of the level-shifted PWM scheme for inverters ( $VSI_H^{(1)}$ ,  $VSI_L^{(1)}$ ) is shown in Fig. 3(a) and the corresponding switching pattern is shown in Fig. 3(b) (OCD triangle). The modulation that can be achieved using common triangular carriers with the references of each VSI is given as:



**Fig. 4.** Post-fault configuration equivalent three-phase space vectors circuit: (a) one failed inverter  $VSI_L^{(1)}$ ,  $v_L^{(1)}=0$ , and (b) minimization of power loss  $VSI_L^{(2)}$ ,  $v_L^{(2)}=0$ .

$$\begin{cases} \bar{v}_H^{(1)} = m^{(1)}V_{dc} \cos(\theta - \pi) - V_{dc}/2 \Rightarrow \{1\}; \\ \bar{v}_L^{(1)} = m^{(1)}V_{dc} \cos\theta - V_{dc}/2 \\ \bar{v}_H^{(2)} = m^{(2)}V_{dc} \cos(\theta - 5\pi/6) - V_{dc}/2 \Rightarrow \{2\} \\ \bar{v}_L^{(2)} = m^{(2)}V_{dc} \cos(\theta + \pi/6) - V_{dc}/2 \end{cases} \quad (14)$$

#### 4. Proposed post-fault tolerant strategy predictions

In a multiple ac drive connected system, if fault occurs in one VSI, the concerned faulty unit will be completely isolated from the source as well as from the load by the protective circuits, i.e. bypass switches/circuit breakers for continuous propagation of the system. In this post-fault investigation, if one  $VSI_L^{(1)}$  predicted faultiness, the ac drive continues to operate but the degrees of freedom reduce from three degrees to two degrees and is represented in space vector equivalent circuit given by Fig. 4(a). Now, the open-end windings configuration collapses to three-phase star connected windings, where  $VSI_H^{(1)}$  alone provides the power in windings {1}. But in windings {2}, where  $VSI_H^{(2)}$  and  $VSI_L^{(2)}$  provided the power, the two degrees of freedom are now represented by  $k_v^{(2)}$  sharing voltage between  $VSI_H^{(2)}$  and  $VSI_L^{(2)}$ , and  $k_i$  sharing current between two three-phase windings {1} and {2}. Hence, according to Eq. 10 the post-fault propagation is predicted as:

$$\begin{cases} \bar{v}_L^{(1)} = 0 \\ \bar{v}_H^{(1)} = \bar{v}^{(1)} \end{cases} \Leftrightarrow k_v^{(1)} = 1. \quad (15)$$

By Eq. 9, Eq. 11 and Eq. 15, VSIs individual power can be written as:

$$\begin{cases} P_L^{(1)} = 0 \\ P_H^{(1)} \cong k_i P \end{cases} \begin{cases} P_L^{(2)} \cong (1-k_i)(1-k_v^{(2)})P \\ P_H^{(2)} \cong (1-k_i)k_v^{(2)}P \end{cases} \quad (16)$$

Consequence of this fault will reduce the maximum output voltage by half for the three-phase windings {1} from  $2/\sqrt{3}V_{dc}$  to  $1/\sqrt{3}V_{dc}$ , as clearly shown in Fig. 2(e). Overall, there is a 50% decrement in maximum power of the ac drive system. In this circumstance, a different control strategy can be adopted in this post-fault operation with available three healthy VSIs ( $VSI_H^{(1)}$ ,  $VSI_H^{(2)}$ , and  $VSI_L^{(2)}$ ). Two relevant investigations are developed: the first one concerns power loss minimization and the second one concerns balanced power sharing among the three healthy VSIs ( $VSI_H^{(1)}$ ,  $VSI_H^{(2)}$ , and  $VSI_L^{(2)}$ ). For investigation purposes Eq. 15 will be formulated in numerical simulations/experimental test to represent this post-fault condition without using any protective circuitries.

#### 4.1. Minimization of power losses

The first post-fault condition is adopted for the balanced sharing of currents between the two windings {1} and {2}, which is ensured by simply applying  $k_i = 1/2$ . Voltage sharing coefficient  $k_v^{(2)}$  synthesizes voltage reference  $v^{(2)}$  between inverters  $VSI_H^{(2)}$  and  $VSI_L^{(2)}$ . Subsequently, the usage of inverters ( $VSI_H^{(2)}$ ,  $VSI_L^{(2)}$ ) is not optimal from the point of inverter losses. The desired output voltage can be synthesized with just one inverter ( $VSI_H^{(2)}$  or  $VSI_L^{(2)}$ ), therefore inverter  $VSI_H^{(1)}$  can propagate with just  $VSI_H^{(2)}$  and set  $VSI_L^{(2)}$  to zero voltage output or vice versa, maintaining exactly the same characteristics. Hence, the open-end windings configuration collapses to star connected in both windings {1} and {2}, represented by the space vector equivalent circuit by Fig. 4(b). By Eq. 10 and Eq. 11, prediction for the post-fault condition by Eq. 12 can be further written as:

$$\begin{cases} \bar{v}_L^{(2)} = 0 \\ \bar{v}_H^{(2)} = \bar{v}^{(2)} \end{cases} \Leftrightarrow k_v^{(2)} = 1, \quad (17)$$

$$\begin{cases} P_L^{(1)} = 0 \\ P_H^{(1)} = \frac{1}{2}P \end{cases} \begin{cases} P_L^{(2)} = 0 \\ P_H^{(2)} = \frac{1}{2}P \end{cases} \Leftrightarrow k_i = \frac{1}{2}. \quad (18)$$

For investigation purposes Eq. 17 will be formulated in numerical simulations/experimental test to represent this first post-fault condition without using any protective circuitries.

#### 4.2. Balanced power sharing among the healthy VSIs

The second the post-fault operating condition is adopted for sharing equally the total power among the three healthy inverters,  $VSI_H^{(1)}$ ,  $VSI_H^{(2)}$ , and  $VSI_L^{(2)}$ . To realize this post-fault condition, unbalanced power sharing has to be created between the two windings {1} and {2}; hence 1/3 of the total power must be supplied by each inverter. Through Eq. 9 to Eq. 11, Eq. 15 to Eq. 16, the post-fault condition can be predicted as:

$$\begin{cases} \bar{v}_L^{(2)} = \frac{1}{2}\bar{v}^{(2)} \\ \bar{v}_H^{(2)} = \frac{1}{2}\bar{v}^{(2)} \end{cases} \Leftrightarrow k_v^{(2)} = \frac{1}{2}, \quad (19)$$

$$\begin{cases} P_L^{(1)} = 0 \\ P_H^{(1)} = \frac{1}{3}P \end{cases} \begin{cases} P_L^{(2)} = \frac{1}{3}P \\ P_H^{(2)} = \frac{1}{3}P \end{cases} \Leftrightarrow k_i = \frac{1}{3}. \quad (20)$$

**Table 1**

Simulation parameters of dual three-phase asymmetrical induction motor.

$P_{rated}$	=8 kW	$R_s$	=0.51 $\Omega$
$I_{s,rated}$	=16 A <sub>rms</sub>	$R_r$	=0.42 $\Omega$
$V_{s,rated}$	=125 V <sub>rms</sub>	$L_{s1}$	=58.2 mH
$\omega_{s,rated}$	= $2\pi 50$ rad/s	$L_{r1}$	=58.2 mH
$P$	=2 (pairs)	$M_1$	=56 mH

For investigation purposes Eq. 19 will be formulated in numerical simulations/experimental test to represent this second post-fault condition without using any protective circuitries.

## 5. Numerical simulation and experimental implementation results

Table 1 gives the main numerical simulation parameters of ac motor drive system. Complete six-phase (quad) asymmetrical open-end windings motor is numerically developed in PLECS/Matlab simulation software. Table 2 gives the main hardware prototype parameters of quad-inverter system. For simplicity in implementation with experimental task, tests are carried out by two DSP TMS320F2812 processor, each one controlling two three-phase inverter ( $VSI_H^{(1)}$  and  $VSI_L^{(1)}$ ,  $VSI_H^{(2)}$  and  $VSI_L^{(2)}$ ) with two three-phase open-end impedance (R-L) load.

Fig. 5(a) provides the overall view of laboratory setup of prototype hardware modules and Fig. 5(b) shows the detailed view of control units and the whole six-phase (quad) inverter prototype hardware system. DSP-1 performs all calculations as master control unit and modulates inverters ( $VSI_H^{(1)}$  and  $VSI_L^{(1)}$ ). DSP-2 receives the modulating signals from the DSP-1 acts as slave control unit and modulates inverters ( $VSI_H^{(2)}$  and  $VSI_L^{(2)}$ ). Communication channel was framed between two DSPs by data cables through multi-channel buffered serial port (McBSP) and properly synchronized for transmitting/receiving data between DSPs [33,34].

#### 5.1. Investigation for performance in healthy condition

In this verification test, the system is analysed in healthy state for the whole time interval [0–90 ms]. Keeping all the sharing coefficients to 1/2 as depicted in Fig. 6(a) and (b), it is ensured that the total power is equally shared among the four VSIs with balanced operation. To be noted, with the frequency set to 50 Hz, modulation indexes of  $VSI_H^{(1)}$ ,  $VSI_L^{(1)}$ ,  $VSI_H^{(2)}$ ,  $VSI_L^{(2)}$  are  $m_H^{(1)} = m_L^{(1)} = m_H^{(2)} = m_L^{(2)} = 0.9$ , i.e.  $m^{(1)} = m^{(2)} = 0.9$ .

Fig. 6(c) and (d) illustrates the simulation and experimental results of the first-phase voltages with fundamental component and phase output currents  $v_1^{(1)}$  (windings {1} purple trace) and  $v_1^{(2)}$  (windings {2} turquoise trace). As predicted, multilevel waveforms with 9-levels appeared, since the modulation index is greater than 0.5 (Fig. 2(d)) and phase shift of  $30^\circ$  is observed.

Six-phase phase currents  $i_{123}^{(1)}$  (windings {1} purple traces) and  $i_{123}^{(2)}$  (windings {2} turquoise traces) are shown in Fig. 6(c) (simulation) and Fig. 6(d) (experimental). Currents are showing sinusoidal

**Table 2**

Hardware parameters of quad-inverter system and six-phase open-winding loads.

MOSFETs (six in parallel per switch)	Vishay Siliconix SUM85N15-19
MOSFET ratings	$V_{DSS} = 150$ V; $R_{DS} = 19$ m $\Omega$ @ $V_{GS} = 10$ V; $I_D = 85$ A
Carrier frequency	=2 kHz (Hardware)
DC-bus capacitance (4 banks)	=12 mF
DC-bus voltage (4 in all)	=52 V
Load impedance (open ends, 6 in all)	=6 $\Omega$
Load power factor (angle)	=0.67 (48 $^\circ$ )
Load rated current	=10 A

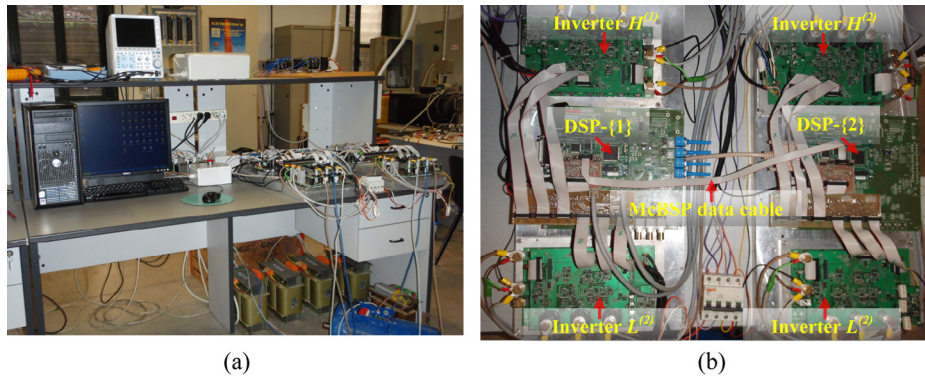


Fig. 5. Six-phase (quad) multiphase-multilevel drives system experimental setup: (a) working area in Lab and (b) overall view of two dsp TMS320F2812 controlled complete ac drive system.

behavior and the same amplitude with correct 30° phase angle displacements, hence proving the effectiveness of the modulation strategy in healthy condition with balanced operating conditions by numerical simulation test and confirming experimental result. But slightly six-phase currents unbalanced in amplitude could be observed with experimental results, due to imperfectly balanced impedances among six-phase.

5.2. Investigation for performance in post-fault conditions with one failed inverter

Following two investigation tests shown in Figs. 7 and 8, post-fault conditions were performed with healthy state [0–30 ms] and faulty condition (red shock arrow) on inverter  $VSI_L^{(1)}$  by setting Eq. 15 ( $k_v^{(1)} = 1$ ). At time instant  $t = 30$  ms the fault on inverter  $VSI_L^{(1)}$  occurs and no further actions are taken ( $t = 30$ –60 ms). Further, the two proposed post-fault (redundancy) conditions (green straight arrow) is adopted at time instant  $t = 60$  ms with respect to the strategies

provided in sub-section 4.1 and sub-section 4.2. To be noted, the frequency set to 25 Hz, modulation indexes of  $VSI_H^{(1)}$ ,  $VSI_L^{(1)}$ ,  $VSI_H^{(2)}$ ,  $VSI_L^{(2)}$  are  $m_H^{(1)} = m_L^{(1)} = m_H^{(2)} = m_L^{(2)} = 0.32$  i.e.  $m^{(1)} = m^{(2)} = 0.32$ .

5.2.1. Balanced power sharing between the two open-end windings

First post-fault condition was conducted to prove the effectiveness of control strategy proposed in sub-section 4.1. Fig. 7(a) and (b) shows the numerical simulation and experimental waveforms variation of voltage and current sharing coefficients when the fault occurs ( $t = 30$  ms,  $k_v^{(1)}$  turns to 1) and post-fault strategy (redundancy) is applied ( $t = 60$  ms,  $k_v^{(2)}$  turns to 1) according to Eq. 17 and Eq. 18. The current sharing coefficient is set at  $k_i = 1/2$  and remains unchanged.

Fig. 7(c) and (d) shows the numerical simulation and experimental waveforms of artificial line-to-neutral voltages with fundamental component of the first-phase of  $VSI_H^{(1)}$ ,  $VSI_L^{(1)}$  (green, red traces) and  $VSI_H^{(2)}$ ,  $VSI_L^{(2)}$  (gray, orange traces) respectively. When the  $VSI_L^{(1)}$  fault occurs on it ( $k_v^{(1)} = 1$  at  $t = 30$  ms), the output voltage

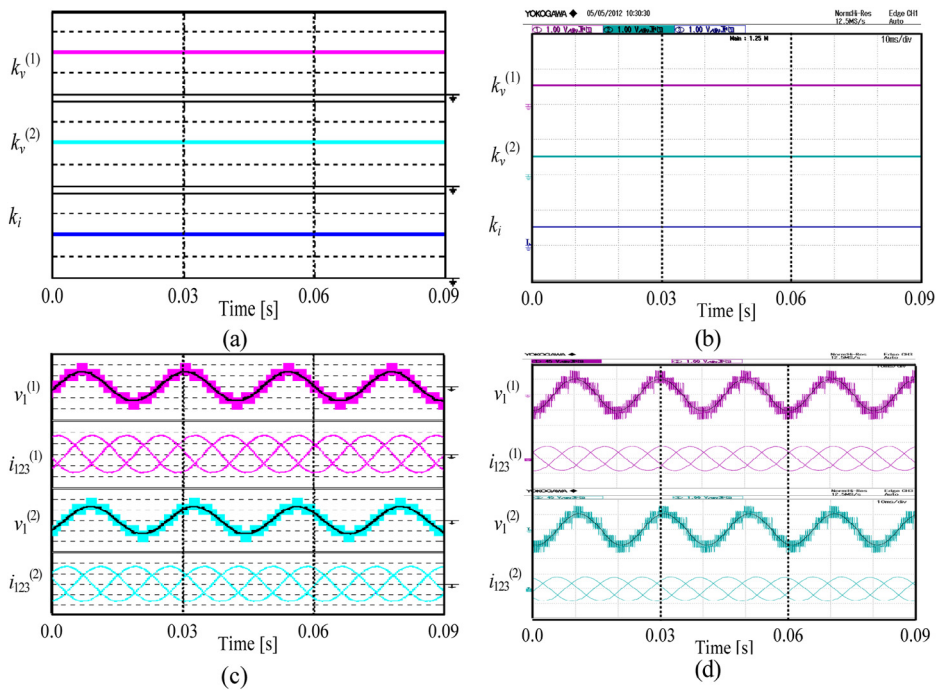
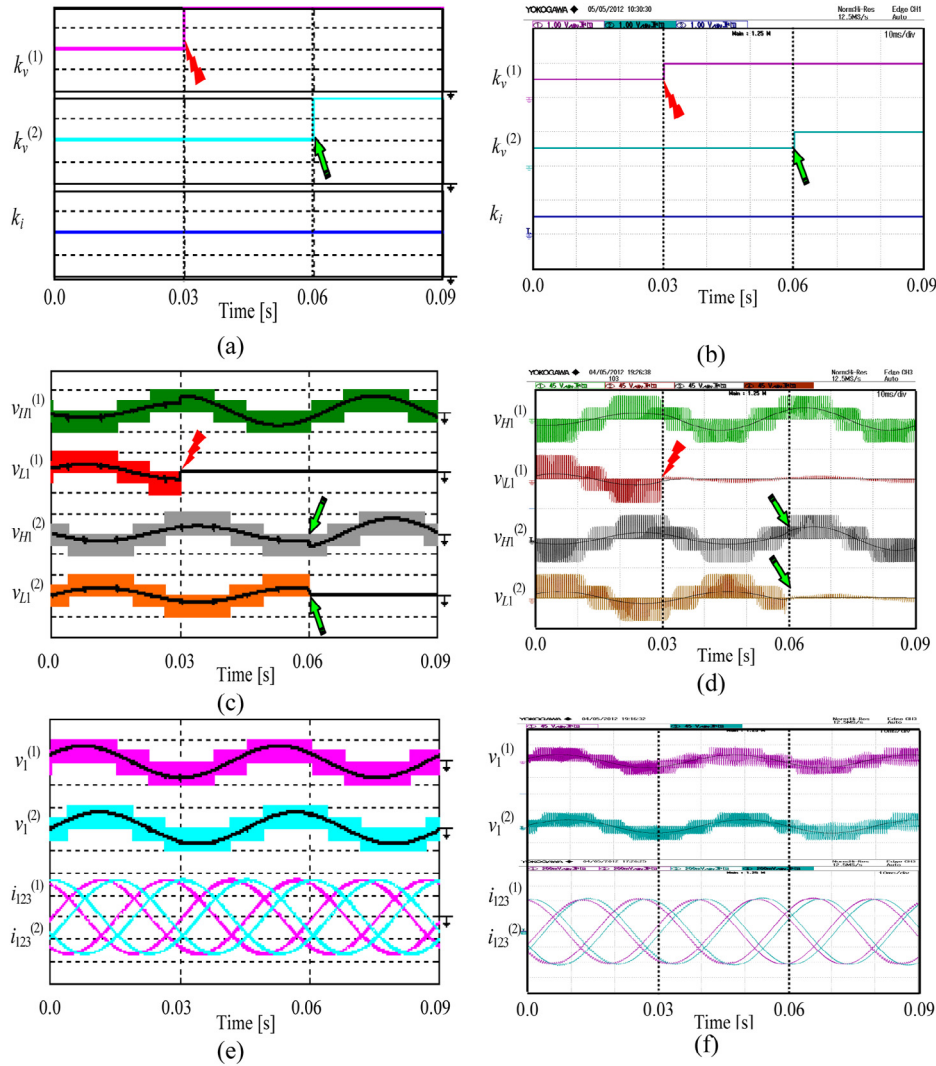


Fig. 6. (a) Simulated and (b) hardware generated waveforms (Healthy condition) of the proposed three degrees of freedom, voltage (turquoise, cyan traces) [0.25 units/div], current sharing coefficients (blue trace) [1 units/div]. First-phase output voltages with time scaled average components and three-phase currents of open-end two windings {1} ( $i_{123}^{(1)}$  – purple traces), {2} ( $i_{123}^{(2)}$  – turquoise traces), (c) simulated [100 V/div, 10 A/div], (d) hardware [45 V/div, 10 A/div] generated waveforms.



**Fig. 7.** (a) Simulated and (b) hardware generated waveforms (**Post-fault condition-1**) of the proposed three degrees of freedom, voltage (turquoise, cyan traces) [0.25 units/div], current sharing coefficients (blue trace) [1 units/div]. Artificial first-phase output voltages along with time scaled average components of VSIs, open-winding {1} ( $V_{SI_H}^{(1)}$  – green,  $V_{SI_L}^{(1)}$  – red traces) and {2} ( $V_{SI_H}^{(2)}$  – gray,  $V_{SI_L}^{(2)}$  – yellow), (c) simulated [100 V/div], (d) hardware [45 V/div] generated waveforms. First-phase output voltages with time scaled average components and three-phase currents of open-end two windings {1} ( $i_{123}^{(1)}$  – purple traces), {2} ( $i_{123}^{(2)}$  – turquoise traces), (e) simulated [100 V/div, 10 A/div], (f) hardware [45 V/div, 2 A/div] generated waveforms.

$v_{L1}^{(1)}$  goes to zero, whereas for the voltage on the other side of three-phase windings {1} provided by the inverter  $V_{SI_H}^{(1)}$ , its output voltage  $v_{H1}^{(1)}$  doubles its value for balancing windings voltage. It is observed during this condition voltages  $v_{H2}^{(2)}$  and  $v_{L2}^{(2)}$  on windings {2} are unaffected. During faulty instant modulation indexes of  $V_{SI_H}^{(1)}$ ,  $V_{SI_L}^{(1)}$ ,  $V_{SI_H}^{(2)}$ ,  $V_{SI_L}^{(2)}$  are  $m_H^{(1)} = 0.64$ ,  $m_L^{(1)} = 0$ ,  $m_H^{(2)} = m_L^{(2)} = 0.32$ , i.e.  $m^{(1)} = m^{(2)} = 0.32$ . Next, the first post-fault control (redundancy) strategy is applied, the  $V_{SI_L}^{(2)}$  turned-off ( $k_v^{(2)} = 1$  at  $t = 60$  ms), the output voltage  $v_{L2}^{(2)}$  goes to zero, whereas for the voltage on the other side of three-phase windings {2} provided by the  $V_{SI_H}^{(2)}$ , its output voltage  $v_{H2}^{(2)}$  doubles its value for the balancing windings voltage. Now, the remaining active  $V_{SI_H}^{(1)}$  and  $V_{SI_H}^{(2)}$  provide the voltages  $v_{H1}^{(1)}$  and  $v_{H2}^{(2)}$  with same amplitudes and the proper  $30^\circ$  phase angle shift is observed. During this post-fault strategy modulation indexes of  $V_{SI_H}^{(1)}$ ,  $V_{SI_L}^{(1)}$ ,  $V_{SI_H}^{(2)}$ ,  $V_{SI_L}^{(2)}$  are  $m_H^{(1)} = 0.64$ ,  $m_L^{(1)} = 0$ ,  $m_H^{(2)} = 0.64$ ,  $m_L^{(2)} = 0$ , i.e.  $m^{(1)} = m^{(2)} = 0.32$ .

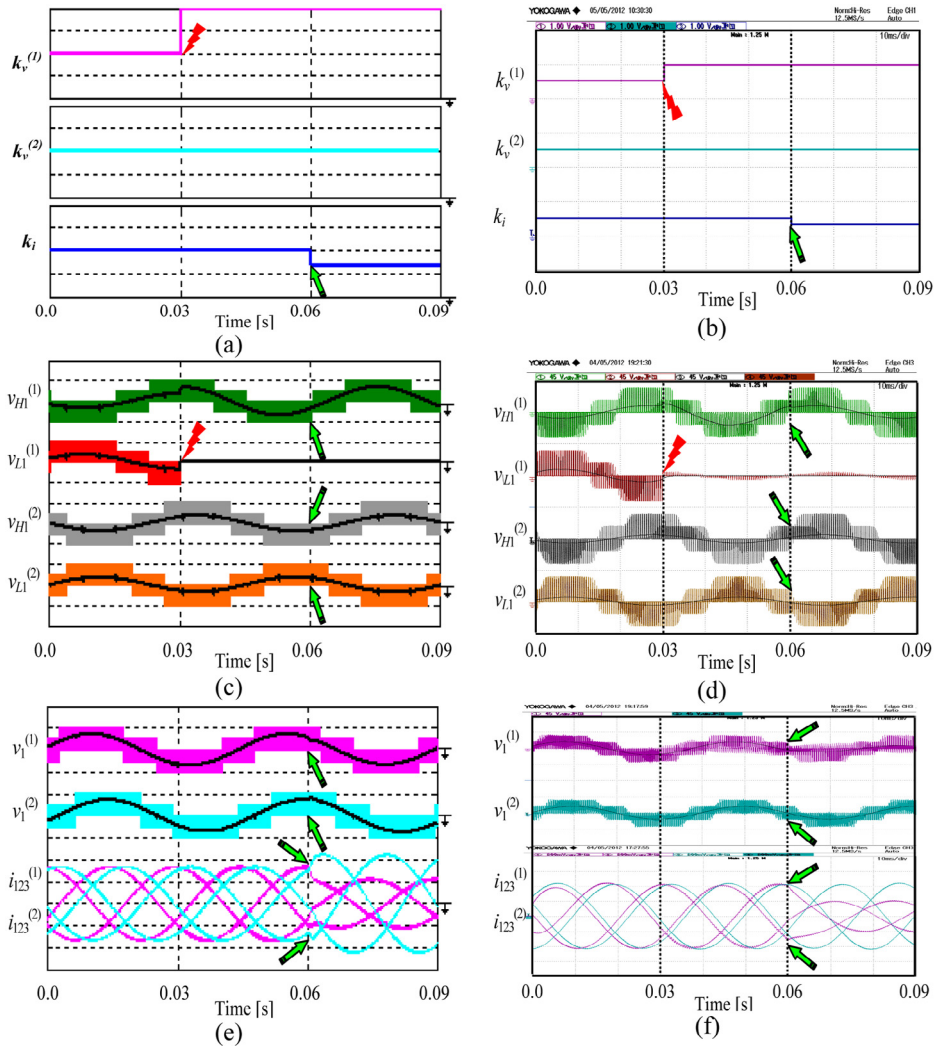
Fig. 7(e) and (f) illustrates the numerical simulation and experimental results of the first-phase voltages with fundamental component and phase output currents,  $v_1^{(1)}$  (purple trace) and  $v_1^{(2)}$  (turquoise trace). As predicted, multilevel waveforms reduced from

9-levels to 5-levels appeared, since the modulation index lesser than 0.5 (Fig. 2(e)) and phase shift of  $30^\circ$  is observed.

Six-phase phase currents  $i_{123}^{(1)}$  (windings {1} purple traces) and  $i_{123}^{(2)}$  (windings {2} turquoise traces) are shown in Fig. 7(e) (simulation) and Fig. 7(f) (experimental). It is expected that practically both voltages and currents are unaffected by the fault and transients by the power sharing. It is verified from both simulation and experimental results that the total power is equally shared between inverters  $V_{SI_H}^{(1)}$  and  $V_{SI_H}^{(2)}$  in this first post-fault control strategy according to Eq. 18.

#### 5.2.2. Balanced power sharing among the three healthy VSIs

Second post-fault condition was conducted to prove the effectiveness of the proposed control strategy in sub-section 4.2. Fig. 8(a) and (b) shows the numerical simulation and experimental waveforms variation of voltage and current sharing coefficients when the fault occurs ( $t = 30$  ms,  $k_v^{(1)}$  turns to 1) and post-fault strategy (redundancy) is applied ( $t = 60$  ms,  $k_i$  turns to  $1/3$ ) according to Eq. 19 and Eq. 20. The current sharing coefficient set at  $k_v^{(2)} = 1/2$  and remains unchanged.



**Fig. 8.** (a) Simulated and (b) hardware generated waveforms (**Post-fault condition-II**) of the proposed three degrees of freedom, voltage (turquoise, cyan traces) [0.25 units/div], current sharing coefficients (blue trace) [1 units/div]. Artificial first-phase output voltages along with time scaled average components of VSIs, open-winding {1} ( $V_{SIH}^{(1)}$  – green,  $V_{SIL}^{(1)}$  – red traces) and {2} ( $V_{SIH}^{(2)}$  – gray,  $V_{SIL}^{(2)}$  – yellow), (c) simulated [100 V/div], (d) hardware [45 V/div] generated waveforms. First-phase output voltages with time scaled average components and three-phase currents of open-end two windings {1} ( $i_{123}^{(1)}$  – purple traces), {2} ( $i_{123}^{(2)}$  – turquoise traces), (e) simulated [100 V/div, 10 A/div], (f) hardware [45 V/div, 2 A/div] generated waveforms.

Fig. 8(c) and (d) shows the numerical simulation and experimental waveforms of artificial line-to-neutral voltages with fundamental component of the first-phase of  $V_{SIH}^{(1)}$ ,  $V_{SIL}^{(1)}$  (green, red traces) and  $V_{SIH}^{(2)}$ ,  $V_{SIL}^{(2)}$  (gray, orange traces) respectively. When the  $V_{SIL}^{(1)}$  fault occurs on it ( $k_v^{(1)} = 1$  at  $t = 30$  ms), the output voltage  $v_{L1}^{(1)}$  goes to zero, whereas for the voltage on the other side of three-phase windings {1} provided by the inverter  $V_{SIH}^{(1)}$ , its output voltage  $v_{H1}^{(1)}$  doubles its value for balancing windings voltage. It is observed during this condition that voltages  $v_{H2}^{(2)}$  and  $v_{L2}^{(2)}$  on windings {2} are unaffected. During faulty instant modulation indexes of  $V_{SIH}^{(1)}$ ,  $V_{SIL}^{(1)}$ ,  $V_{SIH}^{(2)}$ ,  $V_{SIL}^{(2)}$  are  $m_H^{(1)} = 0.64$ ,  $m_L^{(1)} = 0$ ,  $m_H^{(2)} = m_L^{(2)} = 0.32$ , i.e.  $m^{(1)} = m^{(2)} = 0.32$ . Next, the second post-fault control (redundancy) strategy is applied ( $k_i = 1/3$  at  $t = 60$  ms), active  $V_{SIH}^{(1)}$ ,  $V_{SIH}^{(2)}$ ,  $V_{SIL}^{(2)}$  provide the voltages with same amplitudes and the proper  $30^\circ$  phase angle shift is observed. During this second post-fault condition modulation indexes  $V_{SIH}^{(1)}$ ,  $V_{SIL}^{(1)}$ ,  $V_{SIH}^{(2)}$ ,  $V_{SIL}^{(2)}$  are  $m_H^{(1)} = m_L^{(1)} = m_H^{(2)} = 0.32$ ,  $m_L^{(2)} = 0$ , i.e.  $m^{(1)} = 0.16$ ,  $m^{(2)} = 0.32$ . It is verified from both simulation and experimental results that the  $V_{SIH}^{(1)}$ ,  $V_{SIH}^{(2)}$ ,  $V_{SIH}^{(1)}$  provides the same power (voltages) observed from their individual fundamental components of artificial

line-to-neutral voltages in this second post-fault control strategy according to Eq. 20.

Fig. 8(e) and (f) illustrates the numerical simulation and experimental results of the first-phase voltages with fundamental component and phase output currents,  $v_1^{(1)}$  (purple trace) and  $v_1^{(2)}$  (turquoise trace). As predicted, multilevel waveforms reduced from 9-levels to 5-levels appeared, since the modulation index lesser than 0.5 (Fig. 2(e)) and phase shift of  $30^\circ$  is observed.

Six-phase phase currents  $i_{123}^{(1)}$  (windings {1} purple traces) and  $i_{123}^{(2)}$  (windings {2} turquoise traces) are shown in Fig. 8(e) (simulation) and Fig. 8(f) (experimental). The change of current sharing coefficient at  $t = 60$  ms leads to increased currents in windings {2} and decreased currents in windings {1}, according to Eq. 9. It is expected that practically both voltages and currents are unaffected by the fault and transients by the power sharing.

## 6. Conclusion

This manuscript exploited the original developments of post-fault original control strategies for ac drive system based on four



three-phase VSI with simplified level-shifted PWM technique. The whole six-phase (quad) inverter ac drive configuration along with control strategies are numerically implemented with PLECS/Matlab simulation software. Experimental tasks are carried with two DSP TMS320F2812 processors, controlling four VSIs with six-phase open-winding impedances (R-L) as loads. In normal operation, it is confirmed that output voltage generated by the ac drive system will be multilevel stepped waveforms which are equivalent to a 3-level VSI. The total power is shared with three degrees of freedom among the four VSIs by currents and voltages to quadruple the power capabilities. Further, it is verified that in the proposed post-fault conditions (one failed inverter), the total power is reduced to half and one degree of freedom is lost. Other two degrees of freedom are effectively utilized to equally share the total power between the two three-phase open-end winding (motor/R-L impedance) loads or among the three healthy VSIs. Finally, both the obtained simulation and experimental results show close agreement with the developed theoretical predictions.

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