A Wide Input-Voltage Range Quasi-Z Source Boost DC-DC Converter with High Voltage-Gain for Fuel Cell Vehicles

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***Abstract*—A quasi-Z-source Boost DC-DC converter which uses a switched-capacitor is proposed for fuel cell vehicles. The topology can obtain a high voltage gain with a wide input-voltage range, and requires only a low voltage stress across each of the components. The performance of the proposed converter is compared with other converters which use Z-source networks. A scaled-down 400V/400W prototype is developed to validate the proposed technology. The respective variation in the output voltage is avoided when the wide variation in the input voltage happens, due to the PI controller in the voltage loop, and a maximum efficiency of 95.13% is measured.**

***Index Terms*—Boost DC-DC converter, Quasi-Z source, switched-capacitor, voltage PI controller, voltage stress, wide range of voltage-gain.**

I. INTRODUCTION

There is an urgent need to develop clean energy technologies for improving the environment and addressing the challenges to energy usage due to the increasing penetration and renewables and the need to reduce fossil fuel consumption. This is becoming increasingly problematic as the number of automobiles continues to increase worldwide, which also contributes to rising air pollution. Recently, the development of vehicles powered by clean energies has been increasing and their numbers are growing as a percentage of total transportation. Fuel cell vehicles are an important contributor to these clean energy vehicles and have been applied widely in practice as they have high density current output, clean electricity generation, and high efficiency operating characteristics [1], [2]. However, unlike batteries that have a fairly constant output voltage, the fuel cell output voltage drops quickly with an increase of output current [3]-[6]. Therefore, it has to be interfaced to the high voltage DC link bus of the inverter through a step-up DC-DC converter with a wide range of voltage-gain [2].

The isolated step-up DC-DC converter can achieve a high voltage-gain easily. However, the energy of the transformer leakage inductance may produce high voltage stress, increase the switching losses and cause serious electromagnetic interference (EMI) [7]. Therefore, a non-isolated step-up DC-DC converter is often more desirable to reduce the cost, reduce the volume of the converter and improve the conversion efficiency. The commonest non-isolated step-up DC-DC converters is the conventional Boost DC-DC converter. The structure of the converter is simple: only one power switch. The theoretical duty cycle of the power switch can be adjusted from 0 to 1, so the voltage gain can be infinite [8], [9]. However, due to the presence of parasitic elements in the circuit, the voltage gain is limited [10], [11]. In addition, the voltage stress of the power switch is as large as the output voltage, and this demands a high-voltage-rated power switch when the output voltage is high.

In view of the problems described, many solutions have been presented to this challenge. A hybrid Boost three-level DC-DC converter with a high voltage-gain was proposed as a power interface between the low voltage photovoltaic (PV) arrays and the high voltage DC bus for the PV generation system, to reduce the voltage stress and match the voltage levels [12]. Although the desirable voltage stress and the voltage-gain are obtained, the non-common grounds appear between the input and output sides, which may limit its applications. A DC-DC converter with a high voltage-gain and reduced switch stress was proposed for fuel system in [13]. But, a complex three-winding coupled inductor is needed, and the switch surge voltage may be caused due to the leakage inductor. Based on diode-capacitor voltage multipliers, a DC-DC converter can obtain a high voltage-gain and reduced voltage stress [14]. However, a decrease in the output voltage will be caused due to the presence of the internal voltage drop, when the number of the multipliers increases. In another way, Z source and quasi-Z source networks have been employed with the Boost DC-DC converters [15]-[18], and the voltage-gain of these converters can be increased up to $1/(1-2d)$, where d is the duty cycle of the power switch. However, a limitation in the voltage-gain of these converters with Z source and quasi-Z source networks has been found in high voltage-gain applications. In order to improve the voltage-gain of the Boost DC-DC converters with the Z source network further, a hybridization of the Z source converter has been proposed in [19] and [20]. Alternatively, a combination of a quasi-Z source network and a switched-inductor has been proposed in [21], as well as a combination of the quasi-Z source network and a coupled-inductor in [22]. However, they still have drawbacks, such as circuit complexity, increased volume, higher cost, and reduced efficiency. The switched-capacitor

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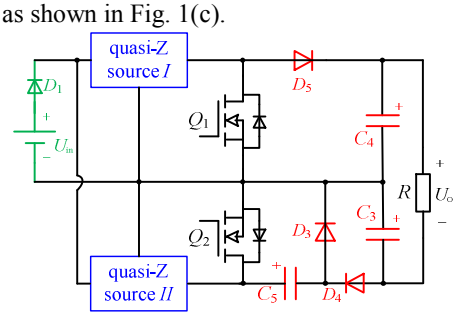
circuit was studied in [23] and [24], and it can achieve flexible voltage regulation by combination with other DC-DC converters [25]-[28]. A Z source DC-DC converter with a cascaded switched-capacitor has been presented in [29], which can improve the voltage-gain of the Z source Boost DC-DC converter by using the voltage multiplier function of the switched-capacitor. However, compared with the quasi-Z source network, this converter may induce additional maintenance safety issues for fuel cell vehicles, due to the penalty of the discontinuous input current and non-common grounds between the input voltage source side and the load side.

In this paper, a quasi-Z source Boost DC-DC converter with a switched-capacitor is proposed for improving the voltage-gain and reducing the voltage stress across the components. This paper is organized as follows: In *Section II*, the configuration and operating principles of the proposed converter are analyzed in detail. The parameter design and dynamic modeling are presented in *Section III*. In *Section IV*, the detailed application of the proposed converter for fuel cell vehicles is addressed. In *Section V*, experimental results are presented to validate the features of the proposed converter.

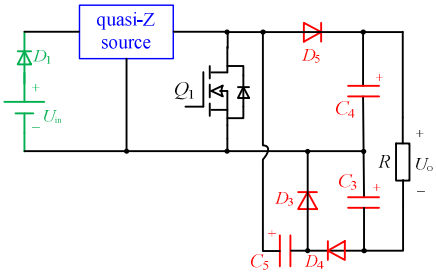
II. OPERATING PRINCIPLES OF THE PROPOSED CONVERTER

A. Configuration of the proposed converter

In order to improve the voltage-gain and reduce the voltage stress across the power semiconductors for the step-up DC-DC converter, two quasi-Z source converters are combined with the structure of input-parallel and output-series, as shown in Fig. 1(a). However, this combined topology really requires one more quasi-Z source network and one more active power switch. Therefore, the deduced and simplified topology can be obtained as shown in Fig. 1(b), in which the combined topology can share the common quasi-Z source network and the active power switch Q_1. In addition, the voltage difference across the grounds between the input and output sides in Fig. 1(b), is nearly the constant voltage across capacitor C_3. So it is better to deduce this topology to be an absolute common ground one. With the equivalent combination of the switched-capacitor networks, a proposed quasi-Z source step-up DC-DC converter with a high voltage-gain, a low voltage stress, and a common ground, is obtained as shown in Fig. 1(c).



(a)



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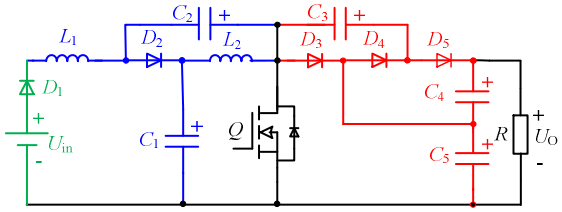


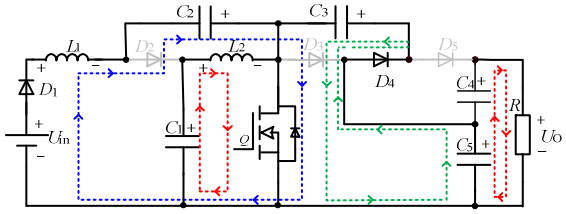
(c)

Fig. 1 Configuration of the proposed converter. (a) Combined interleaved topology with input-parallel and output-series. (b) Deduced and simplified topology. (c) Proposed converter.

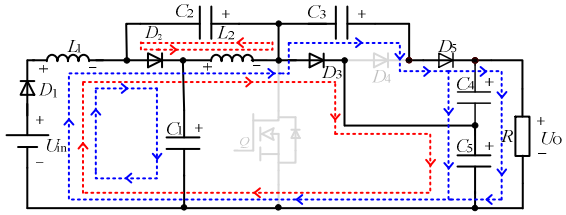
The input voltage source of the converter is comprised of the fuel cell voltage source U_{in} and the reversed blocking diode D_1. The quasi-Z source network is comprised of "L_1-D_2-L_2-C_1-C_2". And the switched-capacitor network is comprised of C_3-D_4, C_4-D_5 and C_5-D_3.

B. Analysis of operating states

According to the switching states of the power switch Q, there are two states for the proposed converter: S=1 and S=0 (Assuming that T is the switching period, d is the duty cycle of the power switch Q, and $d \times T$ is the interval of S=1). Fig. 2 shows the current flow of the proposed converter in the two switching states. Fig. 3 shows the key operating waveforms of the proposed converter over a switching period.



(a)



(b)

Fig. 2 Two operating states of the proposed converter. (a) S=1. (b) S=0.

1) ***S*=1**: The equivalent circuit of the proposed converter in the switching state S=1 is shown in Fig. 2(a). According to the key operating waveforms of the proposed converter shown in Fig. 3, Q is turned on, while diodes D_2, D_3, and D_5 are turned off. The input voltage source U_{in} and the capacitor C_2 transfer energy to the inductor L_1 through the diode D_1 and the power switch Q. C_1 transfers the energy to L_2 through Q. Capacitor C_5

transfers energy to C_3 through D_4 and Q, meanwhile C_5 and C_4 in series provide the energy for the load.

2) ***S*=0**: The equivalent circuit of the proposed converter in the switching state S=0 is shown in Fig. 2(b). According to the key operating waveforms of the proposed converter shown in Fig. 3, Q is turned off, while D_2, D_3, and D_5 are turned on. U_{in} and L_1 transfer energy to C_1 through D_1 and D_2. L_2 transfers energy to C_2 through D_2. U_{in}, L_1, and L_2 transfer energy to C_5 through D_1, D_2 and D_3. At the same time, U_{in}, L_1, L_2 and C_3 in series transfer energy to C_4 and C_5 in series and the load, through D_1, D_2 and D_5.

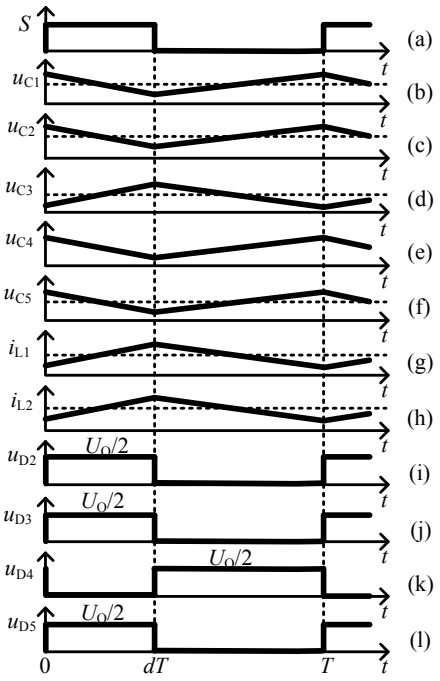


Fig. 3 Key waveforms of the proposed converter.

C. Voltage-gain

It is assumed the forward voltage drops and the on-state resistance of all power semiconductors and the parasitic parameters are ignored, and the capacitance of capacitors and the inductance of inductors in the topology are large enough. The capacitor voltages across C_1, C_2, C_3, C_4 and C_5 are U_{C1}, U_{C2}, U_{C3}, U_{C4} and U_{C5} respectively, the inductor voltages across L_1 and L_2 are U_{L1on} and U_{L2on} when the power switch Q is turned on, and the inductor voltages across L_1 and L_2 are U_{L1off} and U_{L2off} when Q is turned off.

By applying Kirchhoff's Voltage Laws (KVL) to Fig. 2(a) and (b), the following equations can be derived for S=1 and S=0, respectively.

S=1:

$$\begin{cases} U_{L1on} = U_{in} + U_{C2} \\ U_{L2on} = U_{C1} \\ U_{C3} = U_{C5} \\ U_O = U_{C4} + U_{C5} \end{cases} \tag{1}$$

S=0:

$$\begin{cases} U_{L1off} = U_{in} - U_{C1} \\ U_{L1off} = U_{in} - U_O + U_{C2} + U_{C3} \\ U_{L2off} = -U_{C2} \\ U_{C3} = U_{C4} \end{cases} \tag{2}$$

By applying the voltage-second balance principle to the inductors L_1 and L_2 in the continuous current mode, (3) can be obtained as:

$$\begin{cases} U_{L1on} \times dT + U_{L1off} \times (1-d)T = 0 \\ U_{L2on} \times dT + U_{L2off} \times (1-d)T = 0 \end{cases} \tag{3}$$

From (1)-(3), (4) can be obtained as:

$$\begin{cases} U_{C1} = \dfrac{1-d}{1-2d} U_{in} \\ U_{C2} = \dfrac{d}{1-2d} U_{in} \\ U_{C3} = U_{C4} = U_{C5} = U_O/2 \\ U_O = \dfrac{2}{1-2d} U_{in} \end{cases} \tag{4}$$

Thus, the voltage-gain M of the proposed converter can be expressed as (5)

$$M = \frac{2}{1-2d} \tag{5}$$

where $0<d<0.5$.

D. Analysis of voltage stress

1) Voltage stress across capacitors

The capacitor voltages can be expressed as (6) in terms of (4)

$$\begin{cases} U_{C1} = \dfrac{1-d}{2} U_O \\ U_{C2} = \dfrac{d}{2} U_O \\ U_{C3} = U_{C4} = U_{C5} = U_O/2 \end{cases} \tag{6}$$

In terms of (6), the sum of the voltage stresses across C_1 and C_2 is $U_O/2$, and the voltage stresses across C_3-C_5 are all $U_O/2$.

2) Voltage stress across power semiconductors

According to Fig. 2(a), when Q is turned on, D_2, D_3 and D_5 are turned off. The reverse voltage across D_2 is equal to the sum of the voltages across C_1 and C_2, which is $U_O/2$. The reverse voltage across D_3 is equal to the voltage across C_5, which is also $U_O/2$. The reverse voltage across D_5 is equal to the voltage across C_4, namely $U_O/2$. As seen in Fig. 2(b), when the power switch Q is turned off, D_4 is turned off. The voltage across Q is equal to the voltage across C_5, which is $U_O/2$. The reverse voltage across D_4 is equal to the voltage across C_3, which is $U_O/2$ too. In addition, (7) can be written as

$$U_{C5} = U_{C1} + U_{C2} \tag{7}$$

By means of (7), the capacitor voltage U_{C5} across C_5 directly depends on the sum of U_{C1} and U_{C2}, which is clamped at $U_O/2$, as well as the capacitor voltages across C_3 and C_4. So the voltages across the output capacitors C_4 and C_5 have the characteristic of self-balance.

From the analysis above, the voltage stress across all power semiconductors (except D_1, which is still turned on) in the proposed topology are half the output voltage. This feature is beneficial to reduce the conduction losses by selecting low rated-voltage power semiconductors, which have lower on-state resistance or lower forward voltage drops.

E. Analysis of current stress

The output load current is I_o, the average inductor currents of the inductors L_1 and L_2 are I_{L1} and I_{L2}, respectively. The average currents through capacitors C_1, C_2, C_3, C_4 and C_5 are I_{C1on}, I_{C2on}, I_{C3on}, I_{C4on} and I_{C5on}, when the power switch Q is turned on, and I_{C1off}, I_{C2off}, I_{C3off}, I_{C4off} and I_{C5off}, respectively, when Q is turned off. Then (8) and (9) can be obtained as:

S=1:

$$\begin{cases} I_{C1on} = -I_{L2} \\ I_{C2on} = -I_{L1} \\ I_{C4on} = -I_o \\ I_{C5on} = -(-I_{C4on} + I_{C3on}) \end{cases} \tag{8}$$

S=0:

$$\begin{cases} I_{C1off} = I_{C2off} + I_{L1} - I_{L2} \\ I_{C3off} = -I_{C4off} - I_{out} \\ I_{C5off} = I_{L1} - I_{out} - I_{C1off} \end{cases} \tag{9}$$

By applying the ampere-second balance principle to capacitors C_1, C_2, C_3, C_4 and C_5 in the continuous current mode, (10) can be obtained as

$$\begin{cases} I_{C1on} \times dT + I_{C1off} \times (1-d)T = 0 \\ I_{C2on} \times dT + I_{C2off} \times (1-d)T = 0 \\ I_{C3on} \times dT + I_{C3off} \times (1-d)T = 0 \\ I_{C4on} \times dT + I_{C4off} \times (1-d)T = 0 \\ I_{C5on} \times d\,\mathrm{T} + I_{C5off} \times (1-d)\,\mathrm{T} = 0 \end{cases} \tag{10}$$

Assuming that the input power is equal to the output power, i.e. $U_{in} \times I_{in} = U_O \times I_o$. By means of (5), the relationship between the output load current I_o and the average input current I_{in} can be written as

$$I_{in} = \frac{2}{1-2d} I_o \tag{11}$$

In terms of (8)-(11), the average inductor currents and the average capacitor currents can be derived as (12) to (17)

$$I_{L1} = I_{L2} = I_{in} = \frac{2}{1-2d} I_o \tag{12}$$

$$\begin{cases} I_{C1on} = -\dfrac{2I_o}{1-2d} \\ I_{C1off} = \dfrac{2dI_o}{(1-2d)(1-d)} \end{cases} \tag{13}$$

$$\begin{cases} I_{C2on} = -\dfrac{2I_o}{1-2d} \\ I_{C2off} = \dfrac{2dI_o}{(1-2d)(1-d)} \end{cases} \tag{14}$$

$$\begin{cases} I_{C3on} = \dfrac{1}{d} I_o \\ I_{C3off} = \dfrac{-1}{1-d} I_o \end{cases} \tag{15}$$

$$\begin{cases} I_{C4on} = -I_o \\ I_{C4off} = \dfrac{d}{1-d} I_o \end{cases} \tag{16}$$

$$\begin{cases} I_{C5on} = -\dfrac{d+1}{d} I_o \\ I_{C5off} = \dfrac{1+d}{1-d} I_o \end{cases} \tag{17}$$

According to Fig. 2(a), the currents flow through D_4 and Q, when Q is turned on. Then the current stress I_Q of the power switch Q and the current stress I_{D4} of the diode D_4 can be described by means of (12), (15) and (17) as follows:

$$I_Q = I_{L1} + I_{L2} + I_{C3on} = \frac{1+2d}{d(1-2d)} I_o \tag{18}$$

$$I_{D4} = -I_{C5on} = \frac{d+1}{d} I_o \tag{19}$$

Similarly, the currents flow through D_2, D_3 and D_5 when the power switch Q is turned off, according to Fig. 2(b). Then the current stress of diode D_2 can be obtained in terms of (12) and (14) as:

$$I_{D2} = I_{C2off} + I_{L1} = \frac{2}{(1-2d)(1-d)} I_o \tag{20}$$

The current stress of diode D_3 can be written according to (12), (14) and (15) as

$$I_{D3} = I_{L2} - I_{C2off} - (-I_{C3off}) = \frac{1}{1-d} I_o \tag{21}$$

The current stress of diode D_5 can be derived by means of (15) as

$$I_{D5} = -I_{C3off} = \frac{1}{1-d} I_o \tag{22}$$

F. Comparisons with other high voltage-gain converters

The proposed topology is compared with the other high voltage-gain Boost DC-DC converters, as shown in TABLE I, and the comparisons of voltage gain versus duty cycle are shown in Fig. 4.

Compared with the conventional quasi-Z source Boost DC-DC converter, in one hand the voltage-gain of the proposed converter is twice higher than the conventional one, in the other hand, the voltage stress across the power switch is half the output voltage, rather than the full output voltage U_O. So voltage multipliers were applied to the Boost DC-DC converter [7] to reduce the voltage stress of the semiconductors as $U_O/2$. However, if the wider voltage-gain range (including M=10~20) is required, the converter in [7] may suffer from extreme duty cycles (i.e. over d=0.8~0.9), while the proposed converter can operate well with the duty cycles close to 0.5 (i.e. around d=0.4~0.45). As to the converter with a Z-source and cascaded switch-capacitors in [29], its voltage-gain is improved much

higher than those of the converter in [7] and the conventional quasi-Z source Boost DC-DC converter. Furthermore, this converter has a wider voltage-gain range, especially in a lower duty cycle range. But, compared with the proposed one, its disadvantages still include the larger number of inductors, the higher voltage stress across semiconductors, and non-common grounds between the input and output sides. In fact, the number of inductors can be decreased by dual coupled inductors used for the converter in [30], where the turns ratio of the coupled inductors is N=19/18. However, its voltage-gain depends on the turns ratio N. Even worse, the potential difference between the input and output sides is appeared as the PWM voltage, due to the non-common grounds. While the interleaved step-up DC-DC converter with the diode-capacitor multiplier [31] can obtain a common ground, and its voltage-gain is the same with that of the converter in [30]. In addition, the ripple of its input current can be reduced more when the duty cycles of the two power switches are around 0.5, due to the interleaved structure with one more power switch. However, regarding to the voltage-gain range, the proposed converter is wider than this one in the lower duty cycle range (i.e. d=0~1/3), as the curves of voltage gain versus duty cycle shown in Fig. 4. Moreover, in the higher duty cycle range, the voltage-gain of the converter in [31] is lower than that of the proposed one. Especially, the ripple reduction of the input current will be affected both in the lower and higher duty cycle ranges, which are not close to 0.5. A three-level Boost DC-DC converter with a quasi-Z source for fuel cell vehicles was proposed in [32]. Its duty cycles for the two power switches can be in the range of 0.5~0.75, which is close to 0.5. And the voltage stress is half of the output voltage due to the three-level converter structure. However, its essential voltage-gain is still the same to that of the quasi-Z source converter, which is lower than that of the proposed one.

With the comparisons above, it is seen that the proposed converter has the integrated advantages such as the high voltage-gain without extreme duty cycles, the low voltage stress across semiconductors, and the common ground between the input and output sides.

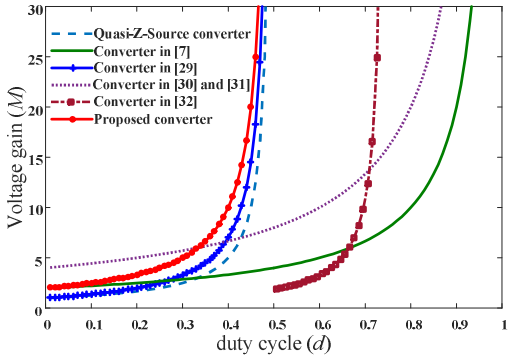


Fig. 4 Comparisons of voltage gain versus duty cycle for high voltage-gain Boost DC-DC converters.

TABLE I Comparisons among the proposed and other high voltage-gain converters.

Converters	Voltage-gain	Amount of inductors	Amount of capacitors	Amount of diodes	Amount of power switches	The maximum voltage stress across diodes	The maximum voltage stress across power switches	Common ground
Quasi-Z-Source converter	1/(1-2d)	2	3	2	1	U_O	U_O	*Yes*
Converter in [7]	2/(1-d)	2	3	3	1	U_O/2	U_O/2	*Yes*
Converter in [29]	(1+d)/(1-2d)	3	5	3	1	U_O/(1+d)	U_O/(1+d)	*No*
Converter in [30], N=19/18	2(N+1)/(1-d)	2	4	4	2	NU_O/(N+1)	U_O/(2N+2)	*No*
Converter in [31]	4/(1-d)	2	4	4	2	U_O/2	U_O/4	*Yes*
Converter in [32]	2/(3-4d)	2	4	3	2	U_O/2	U_O/2	*Yes*
Proposed converter	2/(1-2d)	2	5	4	1	U_O/2	U_O/2	*Yes*

III. COMPONENT PARAMETERS DESIGN AND DYNAMIC MODELING

A. Design of the inductors

Assuming that the maximum required current ripple of the inductors is ΔI_L, the two inductors of the proposed converter can be designed as follows. Because the currents flowing through the inductors L_1 and L_2 are the same, only the parameter design of inductor L_2 is given. The inductance can be calculated when L_2 is in the charging state as (23)

$$L_2 = u_L \frac{\mathrm{d}t}{\mathrm{d}i_{L2}} \tag{23}$$

Where $\mathrm{d}i_{L2} = \Delta I_L$, $\mathrm{d}t = d \times T = d/f$ (where f is the switching frequency), and $u_L = U_{C1}$. The inductances of L_1 and L_2 can be derived from (4) and (23) as

$$L_1 = L_2 = \frac{d(1-d)U_{in}}{(1-2d)\Delta I_L f} \tag{24}$$

B. Design of the capacitors

It is assumed that the maximum required voltage ripple of the capacitor is Δu_C, the capacitances of the five capacitors in the proposed converter can be calculated with (25) when the capacitors are in the charging or discharging states.

$$C = i_C \frac{\mathrm{d}t}{\mathrm{d}u_C} \tag{25}$$

where $\mathrm{d}t=d\times T=d/f$, i_C is the corresponding current flowing through the capacitor, C is the capacitance, and $\mathrm{d}u_C = \Delta u_C$. The capacitances of the five capacitors can be calculated from (4), and (15)-(17) as follows:

$$\begin{cases} C_1 = \dfrac{2dI_O}{(1-2d)\Delta U_{C1} f} \\ C_2 = \dfrac{2d^2 I_O}{(1-2d)\Delta U_{C2} f} \\ C_3 = \dfrac{2I_O}{\Delta U_{C3} f} \\ C_4 = \dfrac{4dI_O}{(1-2d)^2 \Delta U_{C4} f} \\ C_5 = \dfrac{(1+d)I_O}{\Delta U_{C5} f} \end{cases} \tag{26}$$

C. Dynamic modeling

It is assumed that the power semiconductors, the inductors, and the capacitors are all in the ideal conditions. Then, the average model and small-signal model can be obtained by using the state-space averaging method. According to Fig. 2(a), C_3 and C_5 are connected in parallel when Q turns on. It means the voltages across C_3 and C_5 should be equal. So, there is an invalid state variable. By considering the equivalent series resistance (e.g. r_1=0.1Ω) in the corresponding loop circuit, the coupling between C_3 and C_5 can be removed to avoid the invalid state variable. Similarly, according to Fig. 2(b), the coupling among C_1, C_2, C_3, C_4 and C_5 can also be removed to avoid the invalid state variables, by considering the equivalent series resistance (e.g. r=0.1Ω) in the corresponding loop circuit.

When the proposed converter operates in the duty cycle range of 0<d<0.5, the power semiconductor Q has two effective switching states: S=[0, 1]. $u_{in}(t)$, $u_o(t)$ and $d(t)$ are the input variable, the output variable and the control variable, respectively. $i_{L1}(t)$, $i_{L2}(t)$, $u_{C1}(t)$, $u_{C2}(t)$, $u_{C3}(t)$, $u_{C4}(t)$, and $u_{C5}(t)$ are all the state variables. When S=1, the operating time is $d(t)\times T$. So, the state space average model can be obtained as (27), where R is the load resistance. When S=0, the operating time is $[1\text{-}d(t)]\times T$. Then the state space average model can be written as (28). Combining (27) with (28), the average model of the converter can be obtained as (29).

The state variables, the input variable, the output variable and the control variables can be described by the small-signal disturbance variables as (30), where I_{L1}, I_{L2}, U_{C1}, U_{C2}, U_{C3}, U_{C4}, U_{C5}, U_{in}, U_O and D are the steady state components, $\hat{i}_{L1}(t)$, $\hat{i}_{L2}(t)$, $\hat{u}_{C1}(t)$, $\hat{u}_{C2}(t)$, $\hat{u}_{C3}(t)$, $\hat{u}_{C4}(t)$, $\hat{u}_{C5}(t)$, $\hat{u}_{in}(t)$, $\hat{u}_o(t)$ and $\hat{d}(t)$ are the corresponding small-signal disturbance variables. As a result, the small-signal model of the converter can be written as (31).

$$\begin{cases} \begin{bmatrix} \frac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C3}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C4}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C5}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_3 r_1} & 0 & \frac{1}{C_3 r_1} \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_4 R} & -\frac{1}{C_4 R} \\ 0 & 0 & 0 & 0 & \frac{1}{C_5 r_1} & -\frac{1}{C_5 R} & -\frac{R+r_1}{C_5 R r_1} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{in}(t) \\ u_o(t) = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1] [i_{L1}(t) \quad i_{L2}(t) \quad u_{C1}(t) \quad u_{C2}(t) \quad u_{C3}(t) \quad u_{C4}(t) \quad u_{C5}(t)]^T \end{cases} \tag{27}$$

$$\begin{cases} \begin{bmatrix} \frac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C3}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C4}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C5}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_2} & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & -\frac{r+r_1}{C_1 r r_1} & -\frac{r+r_1}{C_1 r r_1} & -\frac{1}{C_1 r} & \frac{1}{C_1 r} & \frac{r+r_1}{C_1 r r_1} \\ 0 & \frac{1}{C_2} & -\frac{r+r_1}{C_2 r r_1} & -\frac{r+r_1}{C_2 r r_1} & -\frac{1}{C_2 r} & \frac{1}{C_2 r} & \frac{r+r_1}{C_2 r r_1} \\ 0 & 0 & -\frac{1}{C_3 r} & -\frac{1}{C_3 r} & -\frac{1}{C_3 r} & \frac{1}{C_3 r} & \frac{1}{C_3 r} \\ 0 & 0 & \frac{1}{C_4 r} & \frac{1}{C_4 r} & \frac{1}{C_4 r} & -\frac{R+r}{C_4 R r} & -\frac{R+r}{C_4 R r} \\ 0 & 0 & \frac{r+r_1}{C_5 r r_1} & \frac{r+r_1}{C_5 r r_1} & \frac{1}{C_5 r} & -\frac{R+r}{C_5 R r} & -\frac{R r_1 + r r_1 + R r}{C_5 R r r_1} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{in}(t) \\ u_o(t) = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1] [i_{L1}(t) \quad i_{L2}(t) \quad u_{C1}(t) \quad u_{C2}(t) \quad u_{C3}(t) \quad u_{C4}(t) \quad u_{C5}(t)]^T \end{cases} \tag{28}$$

$$\begin{cases} \begin{bmatrix} \frac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C3}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C4}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}u_{C5}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{d(t)-1}{L_1} & \frac{d(t)}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{d(t)}{L_2} & \frac{d(t)-1}{L_2} & 0 & 0 & 0 \\ \frac{1-d(t)}{C_1} & -\frac{d(t)}{C_1} & \frac{(r+r_1)[d(t)-1]}{C_1 r r_1} & \frac{(r+r_1)[d(t)-1]}{C_1 r r_1} & \frac{d(t)-1}{C_1 r} & \frac{1-d(t)}{C_1 r} & \frac{(r+r_1)[1-d(t)]}{C_1 r r_1} \\ -\frac{d(t)}{C_2} & \frac{1-d(t)}{C_2} & \frac{(r+r_1)[d(t)-1]}{C_2 r r_1} & \frac{(r+r_1)[d(t)-1]}{C_2 r r_1} & \frac{d(t)-1}{C_2 r} & \frac{1-d(t)}{C_2 r} & \frac{(r+r_1)[1-d(t)]}{C_2 r r_1} \\ 0 & 0 & \frac{d(t)-1}{C_3 r} & \frac{d(t)-1}{C_3 r} & \frac{d(t)(r_1-r)-r_1}{C_3 r r_1} & \frac{1-d(t)}{C_3 r} & \frac{d(t)(r-r_1)+r_1}{C_3 r r_1} \\ 0 & 0 & \frac{1-d(t)}{C_4 r} & \frac{1-d(t)}{C_4 r} & \frac{1-d(t)}{C_4 r} & \frac{d(t)R-R-r}{C_4 R r} & \frac{d(t)R-R-r}{C_4 R r} \\ 0 & 0 & \frac{(r+r_1)[1-d(t)]}{C_5 r r_1} & \frac{(r+r_1)[1-d(t)]}{C_5 r r_1} & \frac{d(t)(r-r_1)+r_1}{C_5 r r_1} & \frac{d(t)R-R-r}{C_5 R r} & \frac{d(t)R r_1 - R r_1 - r r_1 - R r}{C_5 R r r_1} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{C4}(t) \\ u_{C5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{in}(t) \\ u_o(t) = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1] [i_{L1}(t) \quad i_{L2}(t) \quad u_{C1}(t) \quad u_{C2}(t) \quad u_{C3}(t) \quad u_{C4}(t) \quad u_{C5}(t)]^T \end{cases} \tag{29}$$

$$\begin{cases} i_{L1}(t) = I_{L1} + \hat{i}_{L1}(t) \\ i_{L2}(t) = I_{L2} + \hat{i}_{L2}(t) \\ u_{C1}(t) = U_{C1} + \hat{u}_{C1}(t) \\ u_{C2}(t) = U_{C2} + \hat{u}_{C2}(t) \\ u_{C3}(t) = U_{C3} + \hat{u}_{C3}(t) \\ u_{C4}(t) = U_{C4} + \hat{u}_{C4}(t) \\ u_{C5}(t) = U_{C5} + \hat{u}_{C5}(t) \\ u_{in}(t) = U_{in} + \hat{u}_{in}(t) \\ u_o(t) = U_O + \hat{u}_o(t) \\ d(t) = D + \hat{d}(t) \end{cases} \tag{30}$$

According to (31) and the experimental parameters in TABLE II, when the input voltage is U_{in}=40V, the control-to-output transfer function can be achieved from the time domain to the complex frequency as (32).

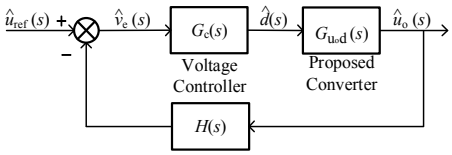


Fig. 5 Voltage loop control scheme of the proposed converter.

Based on (32), the voltage loop control scheme for the proposed converter can be obtained as shown in Fig. 5. $G_{u_o d}(s)$ is the transfer function of the converter, $G_c(s)$ is the voltage controller (i.e. a PI controller) transfer function as shown in (33), and $H(s)$ is the feedback transfer function. Therefore, the voltage controller can be designed for the proposed converter to achieve the static and dynamic performances.

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{u}_{C1}(t)}{dt} \\ \frac{d\hat{u}_{C2}(t)}{dt} \\ \frac{d\hat{u}_{C3}(t)}{dt} \\ \frac{d\hat{u}_{C4}(t)}{dt} \\ \frac{d\hat{u}_{C5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{D-1}{L_1} & \frac{D}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{D}{L_2} & \frac{D-1}{L_2} & 0 & 0 & 0 \\ \frac{1-D}{C_1} & -\frac{D}{C_1} & \frac{(r+r_l)(D-1)}{C_1 r r_l} & \frac{(r+r_l)(D-1)}{C_1 r r_l} & \frac{D-1}{C_1 r} & \frac{1-D}{C_1 r} & \frac{(r+r_l)(1-D)}{C_1 r r_l} \\ -\frac{D}{C_2} & \frac{1-D}{C_2} & \frac{(r+r_l)(D-1)}{C_2 r r_l} & \frac{(r+r_l)(D-1)}{C_2 r r_l} & \frac{D-1}{C_2 r} & \frac{1-D}{C_2 r} & \frac{(r+r_l)(1-D)}{C_2 r r_l} \\ 0 & 0 & \frac{D-1}{C_3 r} & \frac{D-1}{C_3 r} & \frac{Dr_l-Dr-r_l}{C_3 r r_l} & \frac{1-D}{C_3 r} & \frac{Dr-Dr_l+r_l}{C_3 r r_l} \\ 0 & 0 & \frac{1-D}{C_4 r} & \frac{1-D}{C_4 r} & \frac{1-D}{C_4 r} & \frac{DR-R-r}{C_4 R r} & \frac{DR-R-r}{C_4 R r} \\ 0 & 0 & \frac{(r+r_l)(1-D)}{C_5 r r_l} & \frac{(r+r_l)(1-D)}{C_5 r r_l} & \frac{Dr+r_l-Dr_l}{C_5 r r_l} & \frac{DR-R-r}{C_5 R r} & \frac{DRr_l-Rr_l-rr_l-Rr}{C_5 R r r_l} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{u}_{C1}(t) \\ \hat{u}_{C2}(t) \\ \hat{u}_{C3}(t) \\ \hat{u}_{C4}(t) \\ \hat{u}_{C5}(t) \end{bmatrix} \tag{31}$$

$$+ \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{u}_{in}(t) + \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{1}{L_2} & 0 & 0 & 0 \\ -\frac{1}{C_1} & -\frac{1}{C_1} & \frac{r+r_l}{C_1 r r_l} & \frac{r+r_l}{C_1 r r_l} & \frac{1}{C_1 r} & -\frac{1}{C_1 r} & -\frac{r+r_l}{C_1 r r_l} \\ -\frac{1}{C_2} & -\frac{1}{C_2} & \frac{r+r_l}{C_2 r r_l} & \frac{r+r_l}{C_2 r r_l} & \frac{1}{C_2 r} & -\frac{1}{C_2 r} & -\frac{r+r_l}{C_2 r r_l} \\ 0 & 0 & \frac{1}{C_3 r} & \frac{1}{C_3 r} & \frac{r_l-r}{C_3 r r_l} & -\frac{1}{C_3 r} & \frac{r-r_l}{C_3 r r_l} \\ 0 & 0 & -\frac{1}{C_4 r} & -\frac{1}{C_4 r} & -\frac{1}{C_4 r} & \frac{R}{C_4 R r} & \frac{R}{C_4 R r} \\ 0 & 0 & -\frac{r+r_l}{C_5 r r_l} & -\frac{r+r_l}{C_5 r r_l} & \frac{r-r_l}{C_5 r r_l} & \frac{R}{C_5 R r} & \frac{Rr_l}{C_5 R r r_l} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ U_{C1} \\ U_{C2} \\ U_{C3} \\ U_{C4} \\ U_{C5} \end{bmatrix} \hat{d}(t)$$

$$\hat{u}_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) & \hat{i}_{L2}(t) & \hat{u}_{C1}(t) & \hat{u}_{C2}(t) & \hat{u}_{C3}(t) & \hat{u}_{C4}(t) & \hat{u}_{C5}(t) \end{bmatrix}^T$$

$$G_{u_o d}(s) = \left. \frac{\hat{u}_o(s)}{\hat{d}(s)} \right|_{\hat{u}_{in}(s)=0} = \tag{32}$$

$$\frac{3.1\times10^{-18}s^6 + 2.4\times10^{-13}s^5 + 3.2\times10^{-9}s^4 + 1.2\times10^{-5}s^3 + 1.7\times10^{-2}s^2 + 51s + 2700}{1.02\times10^{-24}s^7 + 1.02\times10^{-19}s^6 + 1.6\times10^{-15}s^5 + 6.8\times10^{-12}s^4 + 7.9\times10^{-9}s^3 + 3.1\times10^{-5}s^2 + 6.8\times10^{-4}s + 1}$$

$$G_c(s) = K_p + K_i \frac{1}{s} \tag{33}$$

where K_p=0.0001, and K_i=0.0005, which are used in the experiments.

IV. Application of the Proposed Converter for Fuel Cell Vehicles

A. Characteristics of fuel cell

For fuel cell vehicles, the proton exchange membrane fuel cell (PEMFC) can be used to comprise a fuel cell source for vehicles with the parallel and series connections, and the fuels consist of a supply of hydrogen (H_2) and oxygen (O_2). The basic structure of the PEMFC is shown in Fig. 6 [33]. When a fuel cell operates, H_2 is oxidized at the anode, described as follows:

$$H_2 \rightarrow 2H^+ + 2e^- \tag{34}$$

where "H^+" is the hydrogen ion, and "e^-" is the electric charge. In addition, O_2 is consumed by H^+, generating the water as follows:

$$O_2 + 4H^+ + 4e^- \rightarrow 2H_2O \tag{35}$$

where "H_2O" is the produced water. Therefore, the electric charge "e^-" that flows through the anode and the cathode if there is a load, is generated with the clean water [34].

As to a fuel cell, its simplified circuit can be described as shown in Fig. 7 [34]. Where E_o is the open-circuit voltage of the fuel cell, the paralleled C_a and R_a are the anode reaction capacitor and the resistor, respectively. Similarly, the paralleled C_c and R_c are the cathode reaction capacitor and the resistor, respectively. In addition, R_m is the equivalent series resistor for the membrane of the PEMFC. Finally, U and I are the output voltage and current of the fuel cell. Therefore, the output voltage U can be expressed as (36)

$$U = E_o - I \times (R_a + R_m + R_c) \tag{36}$$

where the total resistance of R_a, R_c, and R_m varies with the inside changing temperature and pressure of the PEMFC.

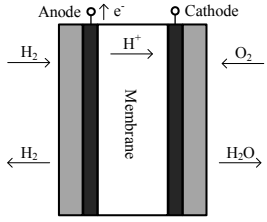


Fig. 6 Basic structure of PEMFC.

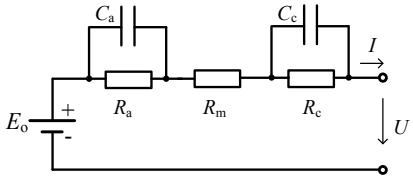


Fig. 7 Simplified circuit for PEMFC.

Therefore, the general output characteristic curve of the voltage-current (V-A) for the PEMFC can be described as shown in Fig. 8, in terms of (36) and the inside temperature and pressure. It can be seen that the output voltage U of the fuel cell decreases rapidly with the increase of the output current I, especially in the smaller output current stage. However, this characteristic is not beneficial for fuel cell vehicles, unless the wide output voltage range of the fuel cell source can be converted well by a wide input-voltage range Boost DC-DC converter, obtaining the rather constant DC bus voltage for fuel cell vehicles.

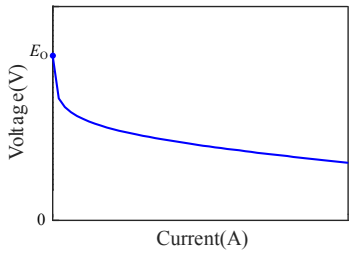


Fig. 8 General output characteristic curve of voltage-current (V-A) for PEMFC.

B. Application of the proposed converter for fuel cell vehicles

Based on the characteristics of the fuel cell described previously, the energy sources of fuel cell vehicles can be comprised of a fuel cell source and super capacitor or battery

stacks, and the powertrain of fuel cell vehicles with the proposed converter is shown in Fig. 9. In order to decouple the power controls of the hybrid energy sources, DC-DC converters are required for the power interfaces of fuel cell vehicles, as well as the common DC bus, with which the hybrid energy sources can be connected in parallel to provide the proper required powers for the motor, respectively. As a result, the fuel cell source of the vehicle only needs to provide the average power for the motor without a quick response. The super capacitor or battery packs can output the required high frequency power for the motor, or absorb the controllable regenerative power from the motor. In addition, the terminal voltage of the fuel cell source varies widely when its output current is within a wide range according to the motor load, and a wide voltage-gain range of a power converter is also required for the fuel cell source.

As shown in Fig. 9, the proposed DC-DC converter with a high voltage-gain is interfaced between the low voltage fuel cell source and the high voltage DC bus. The fuel cell source provides the average power P_{FC} for the DC bus by the proposed converter, boosting the low voltage of fuel cell source to the high DC bus voltage. When the fuel cell vehicle is accelerating, the super capacitor stacks supply the instantaneous power required from the DC bus by the bidirectional DC-DC converter (BDC), due to the slow dynamic response characteristics of the fuel cell source (i.e. the fuel cell output current I_{FC}). Then, I_{FC} increases slowly and the output voltage U_{FC} of the fuel cell source decreases in a wide variation. During this process, the proposed converter steps up the variable fuel cell voltage to the constant high DC bus voltage. When the fuel cell vehicle decelerates or brakes, the regenerative energy is absorbed completely by the super capacitor stacks, and the fuel cell source decreases its output power, i.e. reducing I_{FC}. At the same time, the proposed converter drops its voltage-gain to remain the constant DC bus voltage, according to the increasing U_{FC}. When the fuel cell vehicle runs smoothly, the fuel cell source provides the stable energy for the inverter by the proposed converter with the corresponding voltage-gain, and charges the super capacitor stacks if it is needed.

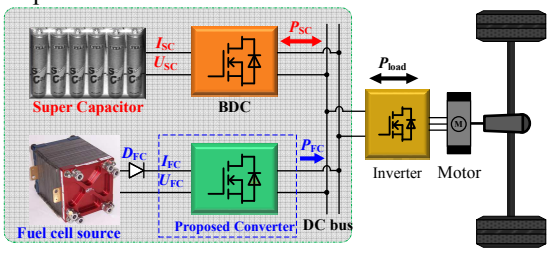


Fig. 9 Powertrain of fuel cell vehicles with proposed converter.

V. EXPERIMENTAL RESULTS AND ANALYSIS

A scaled-down 400W experimental prototype was developed to validate the correctness of the theoretical analysis and the effectiveness of the proposed converter, as shown in Fig. 10. An adjustable DC voltage source with the range of U_{in}=0~200V is used as the input voltage source, and the converter output voltage loop is controlled by a DSP TMS32028335. The power switch MOSFET (IXTK102N30P) and Schottky Barrier Diodes (DSEC60-03A) are selected. In addition, the switching frequency is f_s=20kHz, the initial values of the quasi-Z source network inductors are L_1=323μH and L_2=318μH respectively, the load resistor is R_L=400Ω, and the reference output voltage is 400V. The main experimental parameters of the proposed converter are shown in TABLE II.

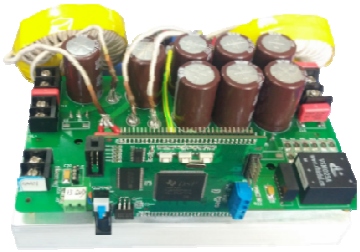


Fig. 10 Experimental prototype.

TABLE II Main experimental parameters of proposed converter.

Parameters	Values(units)
Input DC voltage U_{in}	40~150V
Output DC voltage U_O	400V
Inductor L_1	323μH
Inductor L_2	318μH
Capacitor C_1	520μF
Capacitor C_2	780μF
Capacitors C_3, C_4, and C_5	520μF
Rated power P_n	400W
Load resistor R_L	400Ω
Switching frequency f_s	20kHz
MOSFET Q	IXTK102N30P
Diodes D_1-D_5	DSEC60-03A

The voltage waveforms of the power switch Q, capacitors C_1-C_5 and diodes D_2-D_5, and the current waveforms of the inductors, are shown in Fig. 11-Fig. 13, when the output voltage is 400V.

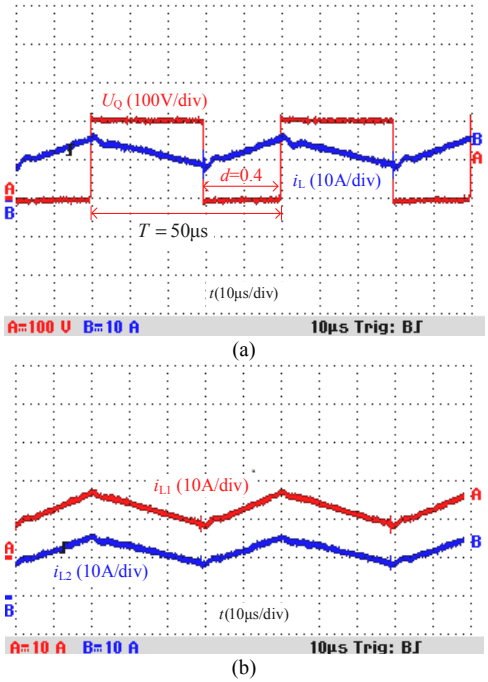
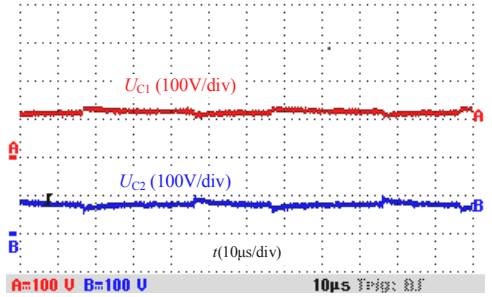


Fig. 11 Voltage stress across power switch Q and inductor currents. (a) Voltage stress across power switch Q and inductor L_1 current. (b) Inductors L_1 and L_2 currents.

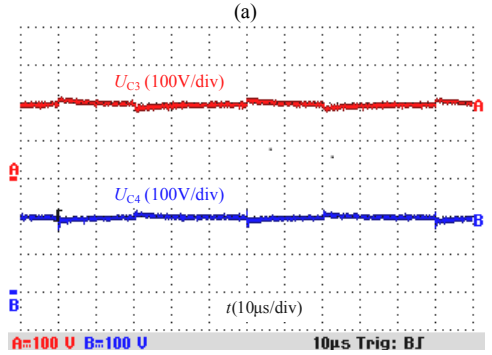
Fig. 11 shows the voltage stress across the power switch Q and the waveforms of the inductor currents i_{L1}, and i_{L2}. From Fig.

11, it can be seen that the switching frequency of the power switch Q is 20kHz, and its duty cycle is 0.4. When Q is turned on, the inductors L_1 and L_2 are charged at the same time, so the currents i_{L1} and i_{L2} increase linearly. When the power switch Q is turned off, the inductors L_1 and L_2 are discharged at the same time, so the currents i_{L1} and i_{L2} decrease linearly. The voltage stress across the power switch is 200V, i.e. half of the output voltage.

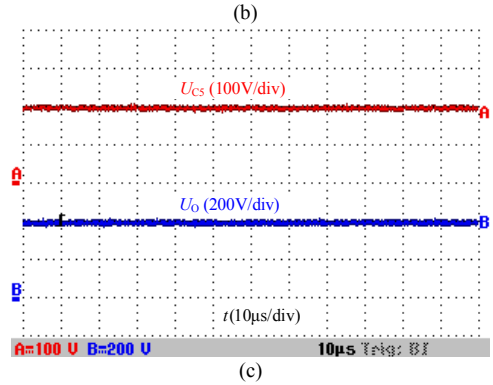
Fig. 12 shows the voltage waveforms of all capacitors in the proposed converter. It is easy to see that the voltage across capacitor C_1 is approximately 122V and the voltage across capacitor C_2 is approximately 82V as shown in Fig. 12(a), which are basically consistent with the theoretical calculated capacitor voltages U_{C1}=120V, and U_{C2}=80V. The capacitor voltage stresses in the quasi-Z source are reduced by a half compared with those in the quasi-Z source Boost DC-DC converter when they have the same voltage-gain. From Fig. 12(b) and (c), the capacitor voltages U_{C3}, U_{C4}, and U_{C5} are approximately half the output voltage U_O=400V, i.e. 200V.



(a)



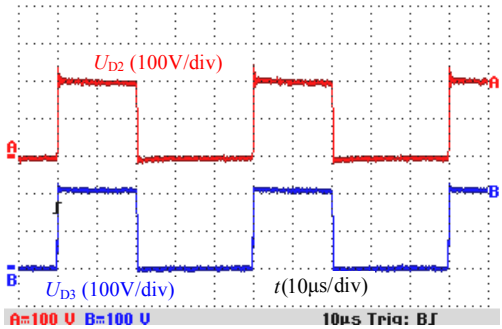
(b)



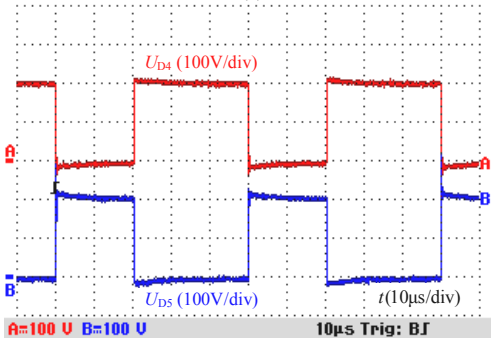
(c)

Fig. 12 Capacitor voltage stresses. (a) Voltage stress across C_1 and C_2. (b) Voltage stress across C_3 and C_4. (c) Voltage stress across C_5 and U_O.

The experimental waveforms for the diode voltage stresses are shown in Fig. 13. The reverse voltages across diodes D_2, D_3, and D_5 are basically equal to half of the output voltage when D_2, D_3, and D_5 are turned off, and D_4 is turned on at the same time. In addition, the reverse voltage across D_4 is also equal to half of the output voltage when D_4 is turned off. The voltage stress across all the diodes are in agreement with the theoretical value U_O/2=200V.



(a)



(b)

Fig. 13 Diode voltage stresses. (a) Voltage stresses across D_2 and D_3. (b) Voltage stresses across D_4 and D_5.

In order to validate the feasibility of the proposed converter for fuel cell vehicles, the experimental operation of the fast input voltage variation like a fuel cell source is implemented, and the experimental results are shown in Fig. 14. The input voltage U_{in} is changed gradually in the wide range of 120V to 40V over several seconds (i.e. the input voltage changing rate is around 8V per second, as the fast input voltage variation is from 120V to 40V over 10 seconds, rather than a step change). Then the input current i_{L1} increases gradually, which is in accordance with the characteristics of the output current of the fuel cell source. Therefore, the PI controller of the voltage loop makes the duty cycle for the active power switch increase with a better dynamic response, according to the input voltage changing rate 8V/s. It is seen that the output voltage nearly stays around the reference voltage 400V as shown in Fig. 14(a), due to the adjustment of the voltage loop PI controller. In Fig. 14(b), the input current i_{L1} increases gradually to match the demand power for the DC bus, due to the gradual decreasing input voltage U_{in}. Hence, the proposed converter can realize a wide step-up voltage-gain range, which changes from 3.3 to 10 during the dynamic operation with the input voltage variation.

The efficiency curves of the experimental prototype are shown in Fig. 15, when the input voltage is changed from 50 to 150V, the output reference voltage is set as 400V, and the output power is 400W and 500W, respectively. The efficiency is measured by a Power Analyzer (Yokogawa-WT3000). It is noticed that the maximum measured efficiency is 95.13% as

shown in Fig. 15, which is higher than the maximum efficiencies 89.3%, 94.37%, and 94% claimed in [29]-[31], respectively. In addition, when the output power is constant and the input voltage declines, the efficiency decreases correspondingly, due to the increasing losses caused by the increasing input current.

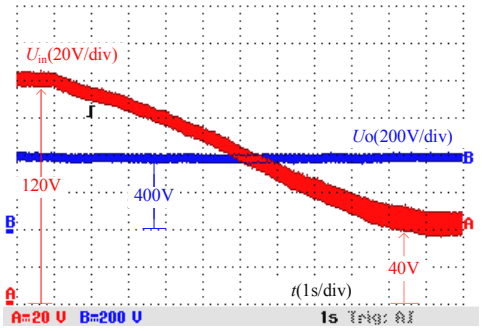


Fig. 14 Dynamic operation results with the input voltage variation. (a) Output voltage and wide range changing input voltage from 120V to 40V. (b) Input current and wide range changing input voltage from 120V to 40V.

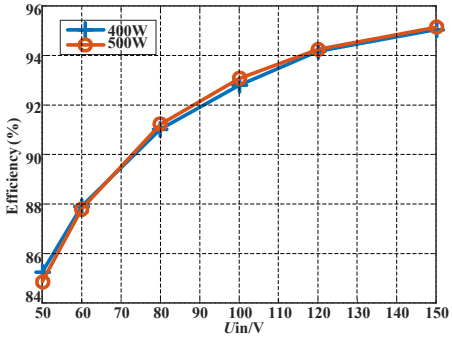


Fig. 15 Relationship between efficiency, and variable input voltages at different output powers.

The calculated loss distributions for the experiment under U_{in}=150V, U_O=400V, and P_O=400W are shown in Fig. 16. The total losses of the proposed converter are 18.6W. The turn-on and turn-off (switching) losses of the power switch Q (i.e. P_2=5.98W) account for 32.1% of the total losses. The conduction losses of all diodes D_1-D_5 (i.e. P_D=3.57W) account for 19.2% of the total losses, which is about three times of that of the power switch Q (i.e. P_Q=1.13W), due to the higher conduction loss of D_2 (which is located in the quasi-Z-source network). In addition to the conduction losses of the semiconductors, the copper losses P_{Cu} of inductors L_1 and L_2 is 3.98W, which account for 21.4% of the total losses. And the core losses P_{Fe} of inductors L_1 and L_2 account for 15.48% of the total losses, which is close to that of the copper losses. The capacitor losses P_C of C_1-C_5 are very close to the conduction loss of the power switch Q, which account for 6.8% of the total losses.

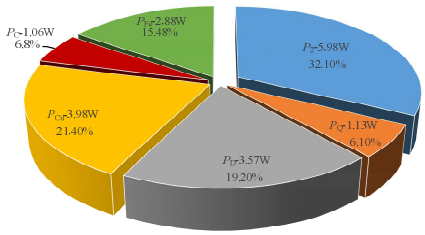


Fig. 16 Calculated loss distributions for experiment under U_{in}=150V, U_O=400V, and P_O=400W (P_2: turn-on and turn-off losses of Q; P_Q: conduction loss of Q; P_D: conduction losses of D_1-D_5; P_{Cu}: copper losses of L_1 and L_2; P_C: capacitor losses of C_1-C_5 , and P_{Fe}: core losses of L_1 and L_2).

VI. Conclusion

The topology of a quasi-Z source Boost DC-DC converter with a switched-capacitor is proposed in this paper. The proposed converter retains all the advantages of the traditional quasi-Z source topology, such as continuous input current and common ground between the input voltage source side and the load side, and it realizes a high voltage gain 2/(1-2d) with the duty cycles between 0 and 0.5 for the power switch. In addition, the maximum voltage stresses of all components in the proposed converter is half of the output voltage. Furthermore, the voltages of the output capacitors can be clamped at half the output voltage by the capacitor voltages of the quasi-Z source network. Therefore, the proposed converter is suitable for the power interface of fuel cell vehicles.

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