Single-Switch, Wide Voltage-Gain Range, Boost DC-DC Converter for Fuel Cell Vehicles

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***Abstract*—In order to match voltages between the fuel cell stacks and the DC link bus of fuel cell vehicles, a single-switch Boost DC-DC converter with diode-capacitor modules is proposed in this paper. The capacitors are charged in parallel and discharged in series. The wide voltage-gain range can be obtained by using a simple structure. In addition, the basic operating principles, the extended stages, the fault tolerant operation, and steady-state characteristics of the converter are analyzed and presented in this paper, and the small-signal model is also derived. A 400V, 1.6kW experimental prototype is developed, and the wide voltage-gain range (3.3~8) is demonstrated with a maximum efficiency at 97.25%. The experimental results validate the effectiveness and feasibility of the proposed converter and its suitability as a power interface for fuel cell vehicles.**

***Index Terms*—Boost DC-DC converter; Fault tolerant operation; Fuel cell vehicles; Low voltage stress; Single-switch; Wide voltage-gain range.**

I. INTRODUCTION

Challenges associated with CO_2 reduction and depleting fossil fuel resources [1]-[4] together with the increasing penetration of renewable resources [5]-[8] has focused research into the electrification of transport including hybrid and full electric vehicles (EVs) [9]-[12]. Fuel cell vehicles have the advantages of high energy conversion efficiency and zero emissions together with a higher range than battery vehicles [13]-[15]. However, fuel cells output a relatively low voltage and high current and they cannot be used directly for electric vehicles which require a high DC bus voltage (e.g. 400V) [16]. In order to match the low voltage of fuel cells with the high DC bus voltage required for EVs, a high voltage-gain Boost DC-DC converter is needed to act as the power interface between the fuel cell stacks and the DC bus. In addition, a battery pack can be connected to the DC bus by a bidirectional DC-DC converter, resulting in a high efficiency powertrain [17]-[18]. Moreover, the output voltage of fuel cells drops with the increasing output power [19]. Therefore, the Boost DC-DC converter for fuel vehicles needs to operate with a wide voltage-gain range.

The conventional Boost DC-DC converter has an ideal voltage-gain of $1/(1-d)$, where d is the duty cycle of the active power switch. However, the high voltage-gain is limited by the effects of parasitic resistance and extreme duty cycles, and the voltage stress seen by all the semiconductors used is as high as the output voltage [20]-[22]. Even though the three-level Boost DC-DC converter can reduce the voltage stress to half of the output voltage, the ideal voltage-gain is still $1/(1-d)$ [23]. In addition, a complicated control strategy is needed for the flying-capacitor voltage to balance the voltage stress seen by all the semiconductors [24]. The switched-inductor Boost DC-DC converter with a high voltage-gain is proposed in [25], but the voltage stress across the power switch is still equal to the output voltage. The two-stage cascaded Boost DC-DC converter also has a high voltage-gain, but its efficiency is the product of the efficiency of each stage [26]. In addition, the semiconductors of the output stage still suffer from a high voltage stress. In [27], a switched-capacitor Boost DC-DC converter is proposed with a high voltage-gain, as well as a low voltage stress. However, a diode is located between the input and output grounds in the circuit, and the corresponding potential difference between the two

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grounds pulsates at the switching frequency. This condition will limit its applications due to the additional electromagnetic interference created.

In addition to widening the voltage-gain range of the Boost DC-DC converter for fuel cell vehicles and reducing its conduction and switching losses, the dv/dt of the potential difference between the input and output grounds of the converter should be zero (i.e. a common ground) or very small. In order to improve the performance over the previously discussed approaches, a single-switch wide voltage-gain range Boost DC-DC converter is proposed in this paper. The voltage stress across all the semiconductors is half of the output voltage, the voltage-gain is 2/(1-d), which is double that of the conventional Boost DC-DC converter, and the variation of the potential difference between the input and output grounds is very small. In *Section II*, the topology of the proposed converter is introduced, and the operating principle is analyzed in *Section III*. In *Section IV*, small-signal model for the proposed converter is developed together with its steady-state analysis and the fault tolerant operation. In *Section V*, an experimental prototype is developed, and the experimental results are presented to validate the proposed converter.

II. TOPOLOGY

The development of the proposed topology is shown in Fig.1. The diode-capacitor branches with the common inductor are in Fig.1(a). D_2-C_1 and D_1-C_2 are two diode-capacitor modules; they are charged in parallel by the input voltage source U_{in} and the inductor L. In Fig.1(b), D_3-C_3 is another diode-capacitor module, and Q-C_1 is reconstructed as a switched-capacitor module from the diode-capacitor module D_2-C_1. The energy stored in C_1 can then be transferred to C_3 through the active power switch Q and the diode D_3. Therefore, the total voltage of the output capacitors C_2 and C_3 in series is double that of the conventional Boost DC-DC converter. Therefore, a single-switch wide voltage-gain Boost DC-DC converter is created as shown in Fig.1(c).

From Fig.1(c), it can be seen that the proposed topology is comprised of one inductor, one active power switch and three diode-capacitor modules with C_1=C_2=C_3.

i_L is the inductor current of L, i_Q is the current through Q, and i_{D1}, i_{D2} and i_{D3} are the currents flowing in D_1, D_2 and D_3, respectively. U_Q is the blocking voltage across Q, U_{D1}, U_{D2} and U_{D3} are the voltage stresses across D_1, D_2 and D_3, respectively. U_{C1}, U_{C2} and U_{C3} are the voltages across C_1, C_2 and C_3. U_o is the output voltage, and I_o is the load current.

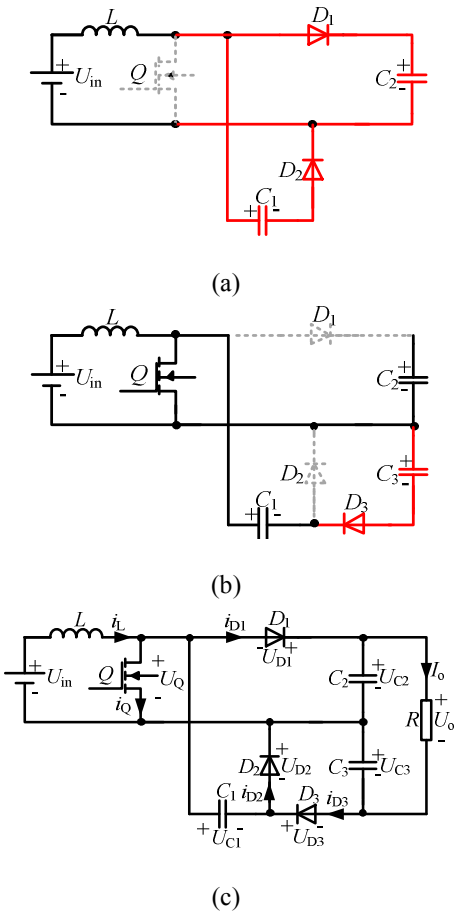


Fig.1 Development of the proposed topology. (a) Diode-capacitor branches with the common inductor. (b) Diode/switch-capacitor branches with the energy transferring. (c) Single-switch wide voltage-gain Boost DC-DC converter.

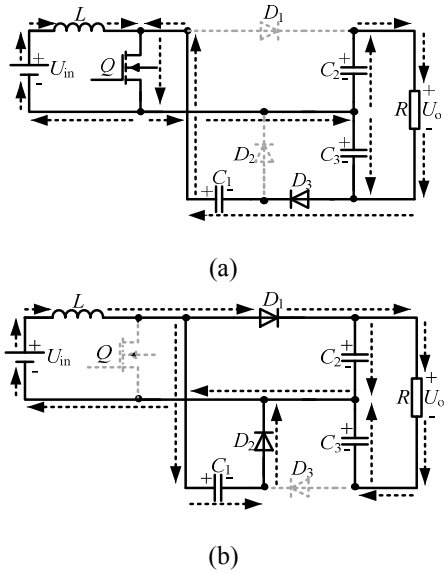
III. OPERATING PRINCIPLES FOR THE PROPOSED CIRCUIT

According to the proposed topology in Fig.1(c), the single-switch DC-DC converter only has two operating states in terms of the turn-on and turn-off states of the active power switch Q. The turn-on and turn-off states of the remaining semiconductors for the two operating states are listed in TABLE. I. The energy flow paths for the two operating states are shown in Fig.2, and the

operating waveforms of the proposed topology are shown in Fig.3.

TABLE. I Turn-on and turn-off states of the corresponding semiconductors under two operating states.

Operating state	*Q*	D_1	D_2	D_3
I	ON	OFF	OFF	ON
II	OFF	ON	ON	OFF



(a)

(b)

Fig.2 Energy flow paths for the two operating states. (a) Operating state *I*. (b) Operating state *II*.

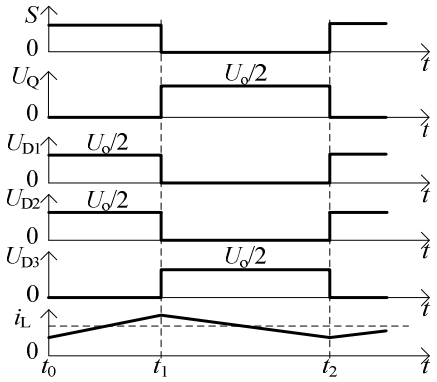


Fig.3 Operating waveforms for the proposed topology.

Operating state I (t₀-t₁): when the active power switch *Q* is turned on, the inductor *L* is charged from U_{in}, C_3 is charged by C_1 through *Q* and D_3, and the load resistor *R* is supplied by C_2 as shown in Fig.2(a). Therefore, D_1 and D_2 are turned off and see blocking voltages of U_{C2} and U_{C3}, respectively. The inductor current i_L rises linearly, and the output voltage U_o is the combined voltages of C_2 and C_3, i.e. $U_o=U_{C2}+U_{C3}$.

Operating state II (t₁-t₂): when *Q* is turned off, U_{in} and the inductor *L* in series discharge into the two diode-capacitor modules in parallel, i.e. C_1 and C_2 are charged in parallel. In addition, the load resistor *R* is supplied by U_{in}, *L*, and C_3 in series as shown in Fig.2(b). Therefore, the voltage stress across *Q* is U_{C2}, and D_3 is turned off with a blocking voltage of U_{C3}. The inductor current i_L falls linearly, and the output voltage U_o is the total voltage of U_{in}, U_L and U_{C3}, i.e. $U_o=U_{C2}+U_{C3}$.

IV. SMALL-SIGNAL MODEL, STEADY-STATE ANALYSIS AND FAULT TOLERANT OPERATION

A. Small-signal model

Assuming that $C_1=C_2=C_3=C$, and the inductance and capacitance of the inductor and capacitors are large enough. The average model and small-signal model can be obtained by using the state-space averaging method. The duty cycle of the active power switch *Q* is *d*. $u_{in}(t)$, $u_o(t)$ and $d(t)$ are the input variable, the output variable and the control variable, respectively. $i_L(t)$, $u_{C1}(t)$, $u_{C2}(t)$ and $u_{C3}(t)$ are the state variables. According to Fig.2(a), C_1 and C_3 are connected in parallel while the active power switch *Q* and diode D_3 are turned on, which means the voltages across C_1 and C_3 are equal. So, there is an invalid state variable in $u_{C1}(t)$ and $u_{C3}(t)$. Similarly, as shown in Fig.2(b), the voltages across C_1 and C_2 are equal, which means there is also an invalid state variable in $u_{C1}(t)$ and $u_{C2}(t)$. By considering the series resistance *r* of capacitor C_1, the coupling between the capacitors can be removed to avoid the invalid state variables.

When *Q* is turned on, the converter is operated in ***operating state I***, and the state space average model can be obtained as follows:

$$\begin{cases} \begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{du_{C1}(t)}{dt} \\ \frac{du_{C2}(t)}{dt} \\ \frac{du_{C3}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{Cr} & 0 & \frac{1}{Cr} \\ 0 & 0 & -\frac{1}{CR} & -\frac{1}{CR} \\ 0 & \frac{1}{Cr} & -\frac{1}{CR} & -\frac{R+r}{CRr} \end{bmatrix} \begin{bmatrix} i_L(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} u_{in}(t) \\ u_o(t) = [0 \quad 0 \quad 1 \quad 1][i_L(t) \quad u_{C1}(t) \quad u_{C2}(t) \quad u_{C3}(t)]^T \end{cases} \quad (1)$$

When Q is turned off, the converter is operated in ***operating state II***, and the state space average model can be written as:

$$\begin{cases}\begin{bmatrix}\frac{\mathrm{d}i_{\mathrm{L}}(t)}{\mathrm{d}t}\\ \frac{\mathrm{d}u_{\mathrm{C1}}(t)}{\mathrm{d}t}\\ \frac{\mathrm{d}u_{\mathrm{C2}}(t)}{\mathrm{d}t}\\ \frac{\mathrm{d}u_{\mathrm{C3}}(t)}{\mathrm{d}t}\end{bmatrix}=\begin{bmatrix}0 & 0 & -\frac{1}{L} & 0\\ 0 & -\frac{1}{Cr} & \frac{1}{Cr} & 0\\ \frac{1}{C} & \frac{1}{Cr} & -\frac{R+r}{CRr} & -\frac{1}{CR}\\ 0 & 0 & -\frac{1}{CR} & -\frac{1}{CR}\end{bmatrix}\begin{bmatrix}i_{\mathrm{L}}(t)\\ u_{\mathrm{C1}}(t)\\ u_{\mathrm{C2}}(t)\\ u_{\mathrm{C3}}(t)\end{bmatrix}+\begin{bmatrix}\frac{1}{L}\\ 0\\ 0\\ 0\end{bmatrix}u_{\mathrm{in}}(t)\\ u_{\mathrm{o}}(t)=\begin{bmatrix}0 & 0 & 1 & 1\end{bmatrix}\begin{bmatrix}i_{\mathrm{L}}(t) & u_{\mathrm{C1}}(t) & u_{\mathrm{C2}}(t) & u_{\mathrm{C3}}(t)\end{bmatrix}^{\mathrm{T}}\end{cases} \tag{2}$$

Combining (1) and (2), the average model of the converter can be obtained as:

$$\begin{cases}\begin{bmatrix}\frac{\mathrm{d}i_{\mathrm{L}}(t)}{\mathrm{d}t}\\ \frac{\mathrm{d}u_{\mathrm{C1}}(t)}{\mathrm{d}t}\\ \frac{\mathrm{d}u_{\mathrm{C2}}(t)}{\mathrm{d}t}\\ \frac{\mathrm{d}u_{\mathrm{C3}}(t)}{\mathrm{d}t}\end{bmatrix}=\begin{bmatrix}0 & 0 & -\frac{1-d(t)}{L} & 0\\ 0 & -\frac{1}{Cr} & \frac{1-d(t)}{Cr} & \frac{d(t)}{Cr}\\ \frac{1-d(t)}{C} & \frac{1-d(t)}{Cr} & -(\frac{1-d(t)}{Cr}+\frac{1}{CR}) & -\frac{1}{CR}\\ 0 & \frac{d(t)}{Cr} & -\frac{1}{CR} & -(\frac{1}{CR}+\frac{d(t)}{Cr})\end{bmatrix}\begin{bmatrix}i_{\mathrm{L}}(t)\\ u_{\mathrm{C1}}(t)\\ u_{\mathrm{C2}}(t)\\ u_{\mathrm{C3}}(t)\end{bmatrix}+\begin{bmatrix}\frac{1}{L}\\ 0\\ 0\\ 0\end{bmatrix}u_{\mathrm{in}}(t)\\ u_{\mathrm{o}}(t)=\begin{bmatrix}0 & 0 & 1 & 1\end{bmatrix}\begin{bmatrix}i_{\mathrm{L}}(t) & u_{\mathrm{C1}}(t) & u_{\mathrm{C2}}(t) & u_{\mathrm{C3}}(t)\end{bmatrix}^{\mathrm{T}}\end{cases} \tag{3}$$

The state variables, the input variable, the output variable and the control variable can be described by introducing small-signal disturbance variables as:

$$\begin{cases}i_{\mathrm{L}}(t)=I_{\mathrm{L}}+\hat{i}_{\mathrm{L}}(t)\\ u_{\mathrm{C1}}(t)=U_{\mathrm{C1}}+\hat{u}_{\mathrm{C1}}(t)\\ u_{\mathrm{C2}}(t)=U_{\mathrm{C2}}+\hat{u}_{\mathrm{C2}}(t)\\ u_{\mathrm{C3}}(t)=U_{\mathrm{C3}}+\hat{u}_{\mathrm{C3}}(t)\\ u_{\mathrm{in}}(t)=U_{\mathrm{in}}+\hat{u}_{\mathrm{in}}(t)\\ u_{\mathrm{o}}(t)=U_{\mathrm{o}}+\hat{u}_{\mathrm{o}}(t)\\ d(t)=D+\hat{d}(t)\end{cases} \tag{4}$$

where I_{L}, U_{C1}, U_{C2}, U_{C3}, U_{in}, U_{o} and D are the steady state components, $\hat{i}_{\mathrm{L}}(t)$, $\hat{u}_{\mathrm{C1}}(t)$, $\hat{u}_{\mathrm{C2}}(t)$, $\hat{u}_{\mathrm{C3}}(t)$, $\hat{u}_{\mathrm{in}}(t)$ and $\hat{d}(t)$ are the small-signal disturbance variables. Combining (3) and (4), the small-signal model of the converter can be written as

$$\begin{cases}\begin{bmatrix}\frac{\mathrm{d}\hat{i}_{\mathrm{L}}(t)}{\mathrm{d}t}\\ \frac{\mathrm{d}\hat{u}_{\mathrm{C1}}(t)}{\mathrm{d}t}\\ \frac{\mathrm{d}\hat{u}_{\mathrm{C2}}(t)}{\mathrm{d}t}\\ \frac{\mathrm{d}\hat{u}_{\mathrm{C3}}(t)}{\mathrm{d}t}\end{bmatrix}=\begin{bmatrix}0 & 0 & -\frac{1-D}{L} & 0\\ 0 & -\frac{1}{Cr} & \frac{1-D}{Cr} & \frac{D}{Cr}\\ \frac{1-D}{C} & \frac{1-D}{Cr} & -(\frac{1-D}{Cr}+\frac{1}{CR}) & -\frac{1}{CR}\\ 0 & \frac{D}{Cr} & -\frac{1}{CR} & -(\frac{1}{CR}+\frac{D}{Cr})\end{bmatrix}\begin{bmatrix}\hat{i}_{\mathrm{L}}(t)\\ \hat{u}_{\mathrm{C1}}(t)\\ \hat{u}_{\mathrm{C2}}(t)\\ \hat{u}_{\mathrm{C3}}(t)\end{bmatrix}\\ +\begin{bmatrix}\frac{1}{L}\\ 0\\ 0\\ 0\end{bmatrix}\hat{u}_{\mathrm{in}}(t)+\begin{bmatrix}0 & 0 & \frac{1}{L} & 0\\ 0 & 0 & -\frac{1}{Cr} & \frac{1}{Cr}\\ -\frac{1}{C} & -\frac{1}{Cr} & \frac{1}{Cr} & 0\\ 0 & \frac{1}{Cr} & 0 & -\frac{1}{Cr}\end{bmatrix}\begin{bmatrix}I_{\mathrm{L}}\\ U_{\mathrm{C1}}\\ U_{\mathrm{C2}}\\ U_{\mathrm{C3}}\end{bmatrix}\hat{d}(t)\\ \hat{u}_{\mathrm{o}}(t)=\begin{bmatrix}0 & 0 & 1 & 1\end{bmatrix}\begin{bmatrix}\hat{i}_{\mathrm{L}}(t) & \hat{u}_{\mathrm{C1}}(t) & \hat{u}_{\mathrm{C2}}(t) & \hat{u}_{\mathrm{C3}}(t)\end{bmatrix}^{\mathrm{T}}\end{cases} \tag{5}$$

B. Steady-state analysis

When the converter is operated in steady-state, the values of the small-signal disturbance variables are 0. Simplifying (3) and (4), I_{L}, U_{C1}, U_{C2}, U_{C3}, and U_{o} can be obtained as (6):

$$\begin{cases}I_{\mathrm{L}}=\frac{2DU_{\mathrm{o}}}{RD(1-D)+r}\\ U_{\mathrm{C1}}=\frac{U_{\mathrm{in}}[RD(1-D)+r-2Dr]}{(1-D)[RD(1-D)+r]}\\ U_{\mathrm{C2}}=\frac{1}{1-D}U_{\mathrm{in}}\\ U_{\mathrm{C3}}=\frac{U_{\mathrm{in}}[RD(D-1)+r]}{(D-1)[RD(1-D)+r]}\\ U_{\mathrm{o}}=\frac{2RDU_{\mathrm{in}}}{RD(1-D)+r}\end{cases} \tag{6}$$

Assuming that the resistance r is 0, simplifying (6), the (7) can be obtained as:

$$\begin{cases}I_{\mathrm{L}}=\frac{2}{1-D}I_{\mathrm{o}}\\ U_{\mathrm{C1}}=U_{\mathrm{C2}}=U_{\mathrm{C3}}=\frac{1}{1-D}U_{\mathrm{in}}\\ U_{\mathrm{o}}=\frac{2}{1-D}U_{\mathrm{in}}\end{cases} \tag{7}$$

According to (7) and Fig.2, the voltage stress across all the semiconductors can be described as:

$$\begin{cases}U_{\mathrm{Q}}=U_{\mathrm{D1}}=U_{\mathrm{C2}}=\frac{U_{\mathrm{o}}}{2}\\ U_{\mathrm{D2}}=U_{\mathrm{C1}}=\frac{U_{\mathrm{o}}}{2}\\ U_{\mathrm{D3}}=U_{\mathrm{C3}}=\frac{U_{\mathrm{o}}}{2}\end{cases} \tag{8}$$

Based on (7) and (8), all the capacitor voltages are half of the output voltage (these are the voltage stresses across all the semiconductors). However, the voltage-gain M of the proposed topology is double that of the conventional Boost DC-DC converter (9):

$$M=\frac{2}{1-d} \tag{9}$$

Then, the duty cycle can be calculated as

$$d=1-\frac{2}{M} \tag{10}$$

If the voltage-gain range of the proposed converter is from 3.3 to 8, the corresponding required duty cycle range is from 0.4 to 0.75, according to (10).

The current stress on all the semiconductors can be deduced from the ampere-second equations for C_1 – C_3, Fig.2, and (7) as:

$$\begin{cases} I_{\mathrm{Q}} = (\dfrac{2}{1-d} + \dfrac{1}{d}) I_{\mathrm{o}} \\ I_{\mathrm{D1}} = I_{\mathrm{D2}} = \dfrac{1}{1-d} I_{\mathrm{o}} \\ I_{\mathrm{D3}} = \dfrac{1}{d} I_{\mathrm{o}} \end{cases} \tag{11}$$

According to (7) and (11), it can be seen that the current stress I_{Q} on Q is larger than the inductor current I_{L}. However, I_{Q} moves closer to I_{L} as the voltage-gain increases. In addition, the current stress on D_1 and D_2 is half of the inductor current, and the current stress on D_3 is (1-d)/d times larger than the inductor current.

The comparisons among the three-level Boost DC-DC converter, the high voltage-gain Boost DC-DC converter in [28], the converters in [29]-[31] and the proposed Boost DC-DC converter are shown in TABLE. II. From the comparison in TABLE. II, it can be seen that the voltage-gain of the proposed converter is higher than that of the three-level Boost DC-DC converter, while the voltage stress and the number of the active power switches and inductors are lower than those of the high voltage-gain Boost DC-DC converter in [28].

According to TABLE. II, the converters in [29] and [30] also have a higher voltage-gain. But the proposed converter can achieve an additional lower voltage stress across the power semiconductors. The single switch hybrid DC-DC converter in [31] can obtain the same voltage-gain and the same voltage stress across the semiconductors, as well as a constant capacitor voltage between the input and output grounds. However, it needs one more inductor and one more capacitor, which may improve the volume, and reduce the efficiency.

TABLE. II Comparisons among the topologies.

	Three-level Boost DC-DC converter	**High voltage-gain Boost DC-DC converter of [20]**	**Converter in [29]**	**Converter in [30]**	**Converter in [31]**	**Proposed converter**
Voltage-gain	1/(1-d)	2/(1-d)	1/(1-d)^2	2(1-d)/(1-2d)	2/(1-d)	2/(1-d)
Maximum voltage stress across power switches	U_{o}/2	U_{o}/2	U_{o}	U_{o}/(2-2d)	U_{o}/2	U_{o}/2
Maximum voltage stress of diodes	U_{o}/2	U_{o}	(2-d)U_{o}	U_{o}/(2-2d)	U_{o}/2	U_{o}/2
The potential difference between the input and output side grounds	Common ground	A high frequency PWM voltage	Common ground	Common ground	A constant capacitor voltage	A constant capacitor voltage
Number of inductors/couple inductors	1	2	2	2	2	1
Number of power switches	2	2	2	1	1	1
Number of diodes	2	2	2	2	3	3

According to the previously analyzed, the proposed converter has these advantages: (a) a high voltage-gain which is double that of the conventional Boost DC-DC converter. (b) a low voltage stress across the power semiconductors which is half of the output voltage. So it is easier (and cheaper) to choose the power semiconductors for the converter, and the switching losses can also be reduced due to the lower on-state resistance. (c) a constant capacitor voltage across the input and output side grounds, which means the variation of the potential difference is very small.

However, there are still some disadvantages for the proposed converter: (a) the current stress on the power switch is high a little bit, it may cause additional power losses. (b) the input current ripple is not low enough, comparing with that of the conventional interleaved Boost converter, due to employing a single inductor and only one active power switch.

C. Stability analysis

1. Stability analysis of the proposed converter

When U_o=400V, d=0.75, L=234μH, C_1=C_2=C_3=470μF, R=100Ω, and r=30mΩ, according to (5), the input-to-output transfer function $G_{io}(s)$ and the control-to-output transfer function $G_{do}(s)$ can be obtained from the time domain to the complex frequency domain as:

$$\begin{cases} G_{io}(s)=\left.\dfrac{\hat{u}_o(s)}{\hat{u}_{in}(s)}\right|_{\hat{d}(s)=0} \\ =\dfrac{4.97\times10^{-9}s^2+6.17\times10^{-4}s+9.38}{2.19\times10^{-15}s^4+3.1\times10^{-10}s^3+6.2\times10^{-6}s^2+3.3\times10^{-4}s+1.17} \\ G_{do}(s)=\left.\dfrac{\hat{u}_o(s)}{\hat{d}(s)}\right|_{\hat{u}_{in}(s)=0} \\ =\dfrac{-1.49\times10^{-10}s^3-1.75\times10^{-5}s^2-0.16s+1875}{2.19\times10^{-15}s^4+3.1\times10^{-10}s^3+6.2\times10^{-6}s^2+3.3\times10^{-4}s+1.17} \end{cases} \quad (12)$$

The PI voltage controller is adopted in the proposed converter, and the voltage loop control scheme of the proposed converter is shown in Fig.4.

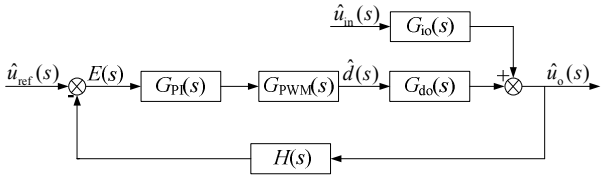


Fig.4 Voltage loop control scheme of the proposed converter.

$E(s)$ is the image function of $e(t)$ in the complex frequency domain. The transfer function $G_{PI}(s)$ of the PI voltage controller, the transfer function $G_{PWM}(s)$ of the pulse-width modulator (PWM), and the feedback transfer function $H(s)$ can be obtained as

$$\begin{cases} G_{PI}(s)=0.0001+\dfrac{0.0008}{s} \\ G_{PWM}(s)=1 \\ H(s)=1 \end{cases} \quad (13)$$

Assuming that $\hat{u}_{in}(s)$ =0, according to Fig.4, the closed-loop transfer function can be obtained by combining (12) and (13) as follows:

$$G(s)=\frac{-6.81(s+1.06\times10^5)(s+1.77\times10^4)(s-6677)(s+8)}{(s+1.18\times10^5)(s+2.4\times10^4)(s+1.1)(s^2+38.64s+2.2\times10^5)} \quad (14)$$

According to (14), all the real parts for the poles of the closed-loop transfer function are less than 0. Therefore, the closed-loop system of the proposed converter with the PI voltage controller can operate stably.

Assuming that $\hat{u}_{ref}(s)$ =0, according to Fig.4, (12) and (13), the steady-state error $e_{ss}(t)$ can be described as

$$\begin{aligned} e_{ss}(t)&=\lim_{t\to\infty}e(t)=\lim_{s\to0}sE(s) \\ &=-\lim_{s\to0}s\frac{H(s)}{1+G_{PI}(s)G_{PWM}(s)G_{do}(s)H(s)}\hat{u}_{in}(s) \\ &=-0.78\lim_{s\to0}s^2\hat{u}_{in}(s) \end{aligned} \quad (15)$$

According to (15), to make the steady-state error $e_{ss}(t)$=0, the disturbance variable of the input voltage $\hat{u}_{in}(t)$ needs to satisfy (16) as follows:

$$\lim_{s\to0}s^2\hat{u}_{in}(s)=0 \quad (16)$$

where $\hat{u}_{in}(s)$ is the image function of $\hat{u}_{in}(t)$. (16) can be simplified as (17) by applying the final-value theorem

$$\lim_{t\to\infty}\frac{d\hat{u}_{in}(t)}{dt}=0 \quad (17)$$

If the voltage variation of the input voltage $\hat{u}_{in}(t)$ satisfies (16) or (17), the closed-loop system of the proposed converter can operate stably.

2. Influences of the input inductor and output capacitors

It should be noticed that (10) is deduced under ideal conditions. The parasitic parameters and the semiconductors in the converter will generate power

losses which can reduce the voltage-gain of the converter. Therefore, in order to obtain the real voltage-gain of the proposed converter, the duty cycle d will be a bit higher than the calculated value from (10). The equivalent circuit of the proposed converter considering the equivalent series resistors of the input inductor L, the output capacitors C_2 and C_3 is shown in Fig.5, where R is the load resistor, r_L is the equivalent series resistance of L, r_{C2} and r_{C3} are the equivalent series resistances of C_2 and C_3.

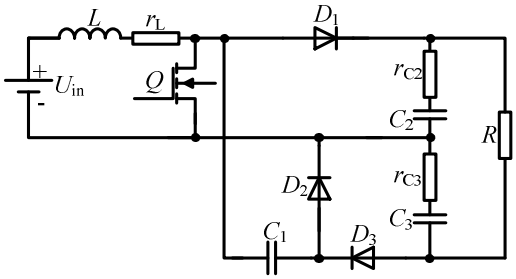


Fig.5 The equivalent circuit of the proposed converter.

According to Fig.5, the following equations can be obtained by applying the ampere-second balance principle on C_1-C_3

$$\begin{cases} d\times I_{D3}=(1-d)\times I_{D2} \\ d\times I_o=(1-d)\times(I_{D1}-I_o) \\ (1-d)\times I_o=d\times(I_{D3}-I_o) \\ I_L=I_{D1}+I_{D2} \end{cases} \tag{18}$$

where I_{D1}, I_{D2} and I_{D3} are the average currents of diodes D_1, D_2 and D_3 in the *ON* state, respectively. Simplifying (18), I_L, I_{D1}, I_{D2} and I_{D3} can be obtained as

$$\begin{cases} I_L=\dfrac{2}{1-d}I_o \\ I_{D1}=\dfrac{1}{1-d}I_o \\ I_{D2}=\dfrac{1}{1-d}I_o \\ I_{D3}=\dfrac{1}{d}I_o \end{cases} \tag{19}$$

The input power P_{in} and the power losses P_2 of C_2 and C_3 can be calculated respectively as

$$\begin{cases} P_{in}=U_{in}I_L \\ P_2=I_L{}^2r_L+[I_o{}^2+(I_{D1}-I_o)^2]r_{C2}+[I_o{}^2+(I_{D3}-I_o)^2]r_{C3} \end{cases} \tag{20}$$

Combining (19) and (20), the output voltage U_o can be obtained as:

$$\begin{aligned} U_o&=\frac{P_{in}-P_2}{I_o} \\ &=\frac{2Rd^2(1-d)^2}{A_1d^4-A_2d^3+A_3d^2-4r_{C3}d+r_{C3}}U_{in} \end{aligned} \tag{21}$$

where

$$\begin{cases} A_1=2r_{C2}+2r_{C3}+R \\ A_2=2r_{C2}+6r_{C3}+2R \\ A_3=4r_L+r_{C2}+7r_{C3}+R \end{cases} \tag{22}$$

According to (21), the real voltage-gain of the proposed converter considering the equivalent series resistors of the input inductor L, the output capacitors C_2 and C_3 can be described as:

$$M=\frac{2Rd^2(1-d)^2}{A_1d^4-A_2d^3+A_3d^2-4r_{C3}d+r_{C3}} \tag{23}$$

Therefore, when the proposed converter operates with the voltage-gain range 3.3~8, the duty cycle range will be a bit higher than 0.4~0.75.

Influences of the series resistances of the input inductor and the output capacitors on the proposed converter can be equivalent as a disturbance variable $\gamma(t)$. The value of $\gamma(t)$ is a constant one that is less than 0, and it will reduce the duty cycle of the converter. Assuming that $\gamma(t)=c$, when the disturbance of the input voltage is 0, the voltage loop control scheme of the proposed converter with the disturbance $\gamma(t)$ is shown in Fig.6, where $\gamma(s)$ is the image function of $\gamma(t)$ in the complex frequency domain.

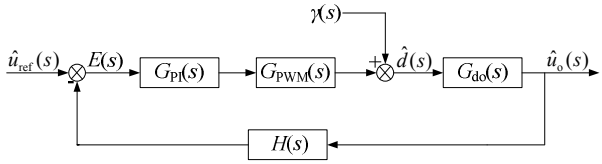


Fig.6 The voltage loop control scheme with the disturbance $\gamma(t)$.

Assuming that $\hat{u}_{ref}(s)=0$, according to Fig.6, (12), and (13), the steady-state error $e_{ss}(t)$ can be obtained as:

$$\begin{aligned} e_{ss}(t)&=\lim_{t\to\infty}e(t)=\lim_{s\to0}sE(s) \\ &=-\lim_{s\to0}s\frac{G_{do}(s)H(s)}{1+G_{PI}(s)G_{PWM}(s)G_{do}(s)H(s)}\gamma(s) \\ &=-1249.9\lim_{s\to0}s^2\gamma(s) \end{aligned} \tag{24}$$

When $\gamma(t)=c$ (i.e. $\gamma(s)=c/s$), according to (24), the steady-state error is $e_{ss}(t)=0$, which means the proposed converter can still operate stably under the influences of the input inductor and output capacitors. Due to the disturbance $\gamma(t)$, the duty cycle of the proposed converter

under the control of the closed-loop system will be higher than the calculated value by (10).

D. The DC-DC Boost converter with extended stages

The proposed converter can be extended with more stages. The topology of the extended DC-DC Boost converter is shown in Fig.7. As shown in Fig.7, the topology consists of (2*n*-1) capacitors and (2*n*-1) diodes. A high voltage-gain can be obtained by extending the number of capacitors and diodes. Fig.8 shows the on/off states of the power semiconductors in the extended DC-DC Boost converter with "*n*" stages. When the active power switch *Q* is turned on, the on/off states of the diodes are shown in Fig.8 (a). Fig.8 (b) shows the on/off states of the diodes while the active power switch *Q* is turned off.

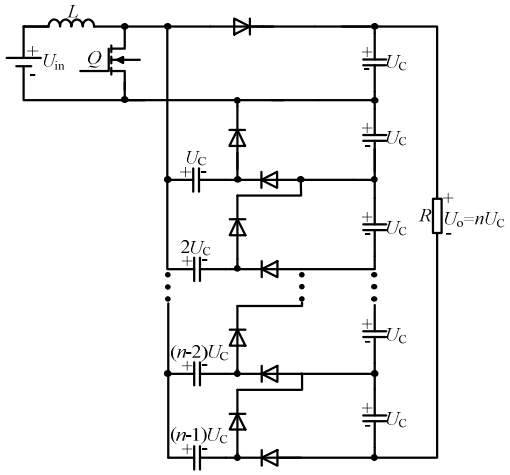


Fig.7 The topology of the DC-DC Boost converter with extended stages.

The output voltage U_o of the extended DC-DC Boost converter with "*n*" stages is:

$$U_o = nU_C = \frac{n}{1-D}U_{in} \tag{25}$$

The voltage stress across each power semiconductor is equal

$$U_Q = U_D = \frac{U_o}{n} = U_C = \frac{1}{1-D}U_{in} \tag{26}$$

where U_Q is the voltage stress across the active power switch *Q*, and U_D is the voltage stress across each diode.

E. Fault tolerant operation

In order to improve the reliability of the proposed converter, a fault tolerant operation under a power semiconductor failure is required. The fault tolerant operation scheme for the proposed converter is based on that in [32]. Then, the fault tolerant operation circuit of the proposed converter is shown in Fig.9.

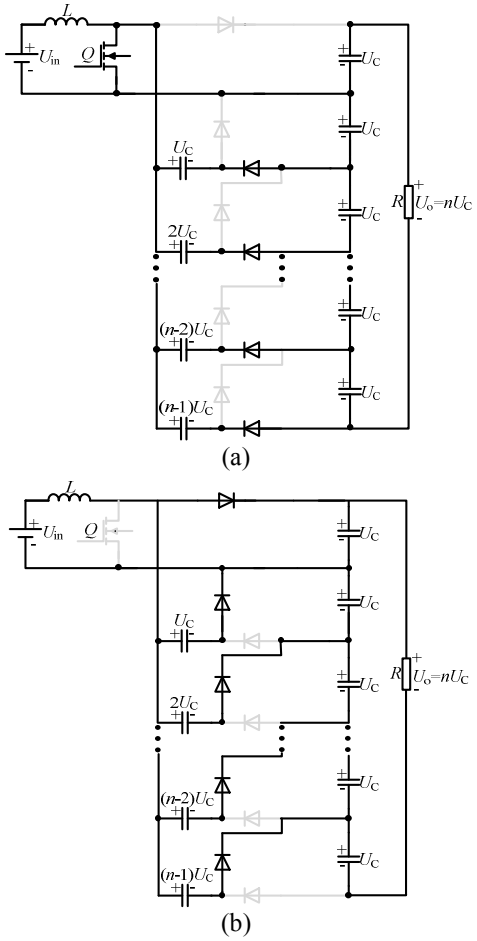


Fig.8 The on/off states of power semiconductors in the DC-DC Boost converter with extended stages. (a) *Q* is turned on. (b) *Q* is turned off.

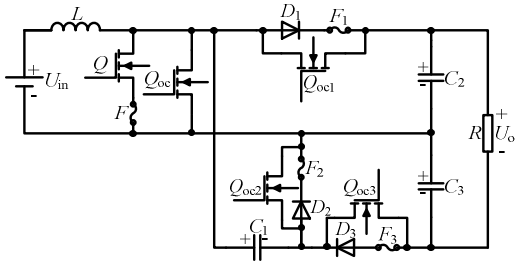


Fig.9 The fault tolerant operation circuit of the proposed converter.

In terms of Fig.1 (c) and Fig.9, the fuses *F*, F_1, F_2 and F_3 and the auxiliary power switches Q_{oc}, Q_{oc1}, Q_{oc2} and Q_{oc3} are required for the fault tolerant operation. When the converter operates in the normal state, Q_{oc}, Q_{oc1}, Q_{oc2} and Q_{oc3} are turned off. When a failure (i.e. a short circuit or an open circuit of the main power switch or the diodes) happens, the converter can still operate in the fault

tolerant condition, by employing the corresponding fuse and the auxiliary power switch.

1. Fault detection and identification

When Q operates in a normal condition, the waveform of U_Q is shown in Fig.3. The failure of Q can be detected by the signal of U_Q and the gate signal S. When S=1 and U_Q=U_o/2, it means the open-circuit fault occurs with Q. When S=0 and U_Q=0, it indicates the short-circuit fault happens with Q. Therefore, the signal "sgn_Q" can be obtained as follows:

$$\mathrm{sgn}_Q = \begin{cases} 0, & U_Q > \delta \\ 1, & U_Q < \delta \end{cases} \tag{27}$$

where δ is a small value between 0 and U_o/2.

The signal "err_Q" is defined as

$$\mathrm{err}_Q = S \oplus \mathrm{sgn}_Q \tag{28}$$

When there is no semiconductor failure, signals S and sgn_Q have the same value, and the signal err_Q is equal to 0, according to (28). When a failure happens, the value of sgn_Q is different from that of S, thus the value of err_Q is equal to 1. It should be noted that the value of err_Q will be 0 when signals S and sgn_Q have the same value again. However, the sampling period and the parasitic parameters in the converter cannot be neglected. When Q operates in a normal condition, there is a time delay between signals S and sgn_Q. During this delay, err_Q will be equal to 1 even there is no switch failure in the converter. Therefore, the strategy of the fault detection and identification for the main power switch Q can be obtained in Fig.10.

By means of Fig.10, when the converter operates in a steady state, "err_Q=0" means there is no switch failure. When the value of the signal err_Q becomes 1, the counter is activated and its output signal n_c is increased. The signal err_Q is also observed at the same time. If n_c>N (where the value of N should be predefined), the duration of "err_Q=1" is longer than the observation time NT_{sam}, where T_{sam} is the sampling period. Then it is concluded that there is a failure with Q (NT_{sam} must be longer than the time delay caused by the sampling period and the parasitic parameters). If the gate signal S is equal to 1 while n_c>N, it can be concluded that the open-circuit fault occurs with Q. Then the values of the signals for the open-circuit fault (OCF) and the short-circuit fault (SCF) become OCF=1 and SCF=0. If the gate signal S is equal to 0 while n_c>N, the short-circuit fault will be detected with Q, then the values of the signals become OCF=0 and SCF=1.

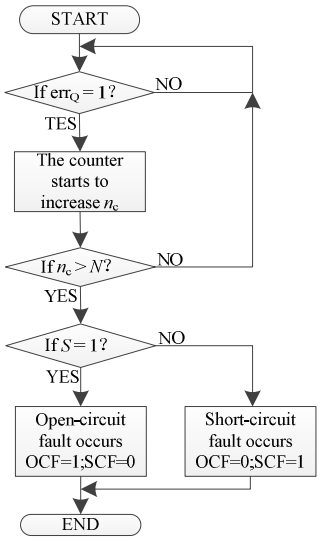


Fig.10 The strategy of fault detection and identification for the main power switch Q.

It should be noticed that only when the duration of "err_Q=1" is longer than NT_{sam}, the fault tolerant operation would work. When an open-circuit fault happens with Q, the duration of "err_Q=1" is always shorter than dT_s. When a short-circuit fault happens with Q, the duration of "err_Q=1" is always shorter than (1-d)T_s. Therefore, if the switching period T_s is close to NT_{sam}, the fault tolerant operation cannot detect the failures with Q. In order to make the fault tolerant operation work properly, T_{sam} must be much shorter than T_s.

2. Remedial actions

The control method of the power switch Q_{oc} for the fault tolerant operation is shown in Fig.11.

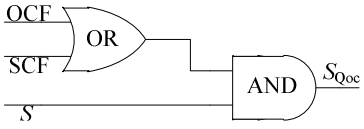


Fig.11 The control method of the power switch Q_{oc} for the fault tolerant operation.

S_{Qoc} is the gate signal of Q_{oc}. According to Fig.9 and Fig.11, when an open-circuit fault occurs with Q, the signal OCF will be set to 1. Then Q will be replaced by the power switch Q_{oc}, and the gate signal S_{Qoc} is the same as S. When a short-circuit fault is detected with Q, Q will

be isolated by the fuse F from the circuit (i.e. the branch related with Q is in the open circuit). Then, the power switch Q_{oc} will replace the power switch Q, while the signal SCF is set to 1. In addition, S_{Qoc} is also the same as S.

The fault tolerant operations of the diodes D_1, D_2 and D_3 are similar to that of the power switch Q. It should be noted that the gate signals of Q_{oc1} and Q_{oc2} need to be complementary to S, while the gate signal of Q_{oc3} should be the same as S. The fault tolerant operation method for the diodes D_2 and D_3 can also be used for the diodes in the DC-DC Boost converter with extended stages.

The proposed converter with the protection for the capacitor failures is shown in Fig.12. The additional power switch Q_C is used to protect the converter when the capacitor fails.

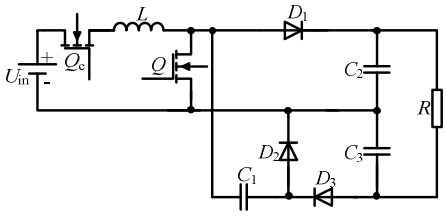


Fig.12 The proposed converter with the protection of the capacitors.

When the converter operates in a steady-state under the voltage loop control, the output voltage U_o is substantially equal to the reference voltage U_{ref}. U_o will decrease to $0.5U_{ref}$ or 0 when the capacitor failures happen, which are almost related to the short-circuit faults. Therefore, the signal "sgn_C" can be defined as follows:

$$sgn_C = \begin{cases} 0, & U_o < kU_{ref} \\ 1, & U_o > kU_{ref} \end{cases} \tag{29}$$

where k is a constant value that satisfies $0.5<k<1$. When $sgn_C=1$, U_o is equal to U_{ref}, there is no capacitor failure in the converter. When a capacitor failure occurs, "sgn_C" will be equal to 0. The signal "$m(t)$" can be obtained as follows:

$$m(t) = \begin{cases} 1, & t < t_0 \\ 0, & t > t_0 \end{cases} \tag{30}$$

where t_0 is the transient time that the converter operates from the starting to the steady-state. The gate signal of Q_C can be obtained by (29) and (30) as follows:

$$S_C = sgn_C + m(t) \tag{31}$$

where "+" represents the logical relationship "OR".

According to (31), during the transient time t_0, S_C is equal to 1, Q_C is turned on, the converter operates in a normal state. When a capacitor failure occurs, S_C is equal to 0, then Q_C will be turned off to protect the converter.

V. EXPERIMENTAL RESULTS AND ANALYSIS

A 1.6kW prototype has been developed, in which a TMS320F28335 DSP is adopted as the controller to form a voltage control loop. An IXYS-IXTK102N30P MOSFET and IXYS-DPG60C300HB Schottky diodes have been selected as the active power switches and diodes, respectively. The switching frequency is f_s=20kHz, the value of the inductor is L=234μH, and the capacitors are $C_1=C_2=C_3$=470μF. The input voltage changes continuously between U_{in}=50V~120V, and the output voltage is controlled constant at U_o=400V; the load resistor is R=100Ω. The experimental prototype is developed, as shown in Fig. 13.

The voltage stress across all the semiconductors and the inductor current for U_{in}=50V and U_o=400V are shown in Fig.14. It can be seen in Fig.14(a) that the duty cycle of the active power switch Q is about d=0.76, (as opposed to approximately d=0.9 for the three-level Boost DC-DC converter), when the voltage-gain M is 8. In addition, the blocking voltage U_Q of Q is 200V (i.e. half the output voltage). The average inductor current is 35A when the output power is 1.6kW. At the same time, the voltage stress across D_1-D_3 is 200V (again half the output voltage), as shown in Fig.14(b, c). Therefore, the single-switch Boost DC-DC converter can perform with a high voltage-gain and a low device voltage stress if a proper duty cycle is used.

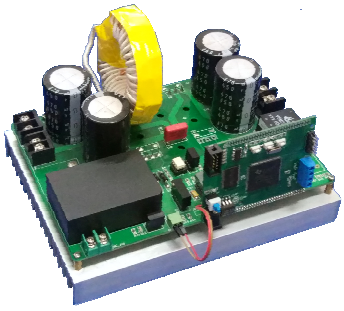
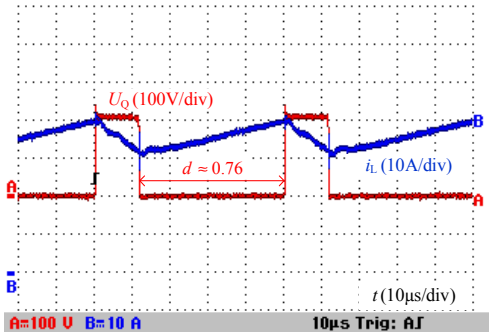
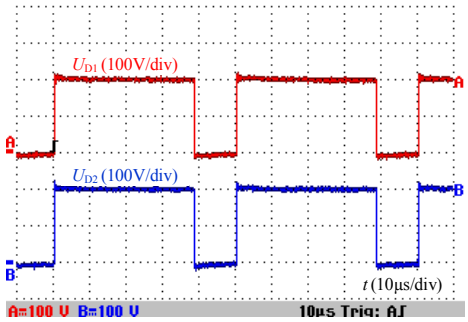


Fig. 13 The experimental prototype of the proposed converter.

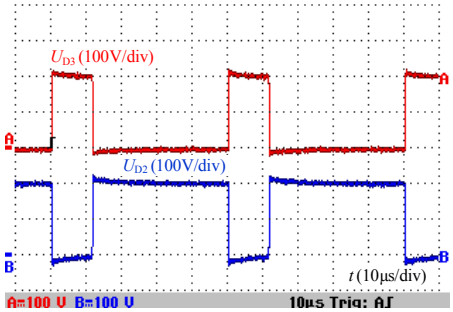
The voltages U_{C2} and U_{C3} across C_2 and C_3 (the output capacitors in series) for U_{in}=50V and U_o=400V are shown in Fig.15. Because these two capacitors are charged and discharged with the same duty cycle, U_{C2} and U_{C3} are both at constant 200V. In addition, the potential difference between the input and output grounds is the voltage across C_3, i.e. constant at 200V with a very small ripple, i.e. a very small dv/dt.



(a)



(b)



(c)

Fig.14 Voltage stress across all semiconductors and inductor current when U_{in}=50V and U_o=400V. (a) Voltage stress across Q and inductor current. (b) Voltage stresses across D_1 and D_2. (c) Voltage stresses across D_2 and D_3.

With the control of the voltage loop, the output voltage U_o can be still controlled at constant 400V, even though the input voltage U_{in} changes from 120V to 50V continuously over 16 seconds, as shown in Fig.16(a). Therefore, the proposed converter can operate well with a wide voltage-gain range, e.g. from 3.3 to 8. The inductor current i_L rises from 14A to 35A following to the falling input voltage, as shown in Fig.16(b).

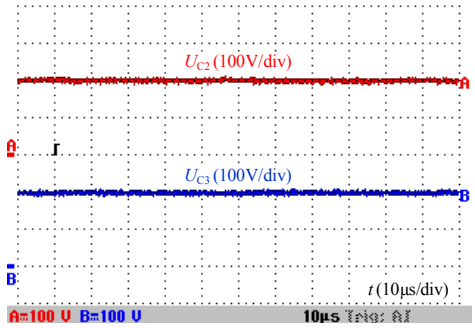
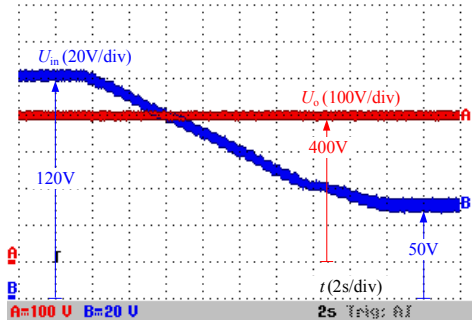
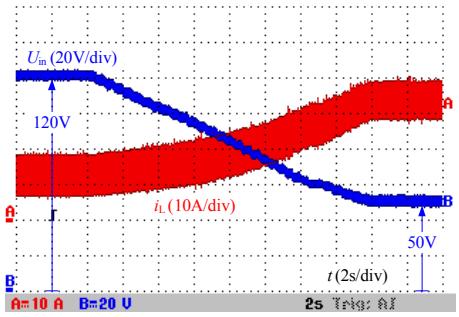


Fig.15 Voltages across C_2 and C_3 under U_{in}=50V and U_o=400V.



(a)



(b)

Fig.16 Output voltage and dynamic inductor current when U_{in} changes from 120V to 50V continuously. (a) Output voltage and input voltage. (b) Dynamic inductor current and input voltage.

In order to show the dynamic behavior of the proposed converter, an experiment with the load step change between 130Ω and 200Ω was carried out. The output voltage and the input current are shown in Fig.17. According to Fig.17, the input current increases quickly from 6.5A to 10A, and the output voltage U_o nearly keeps

at constant 400V with the control of the voltage loop. It can be seen that i_{in} changes from 6.5A to 10A over 8ms with the load step-change from 200Ω to 130Ω, and it recovers from 10A to 6.5A over 8 ms with the load step-change from 130Ω to 200Ω.

For the operation of the proposed converter with a wide input-voltage range, the conversion efficiencies related to the variable input voltages (e.g. 50V, 60V,……, 110V, 120V) and the different output powers (e.g. 800W, 1200W, 1600W) are measured using a power analyzer (YOKOGAWA/WT3000) as shown in Fig.18, when the switching frequency f_s is 20kHz. When the converter outputs 1200W, it has its maximum efficiency 97.25% while the input voltage is U_{in}=120V. And the minimum efficiency is 90.53% when the input voltage is changed to U_{in}=50V. Therefore, the efficiency falls with the increased voltage-gain, due to the increased losses caused by the increased inductor current.

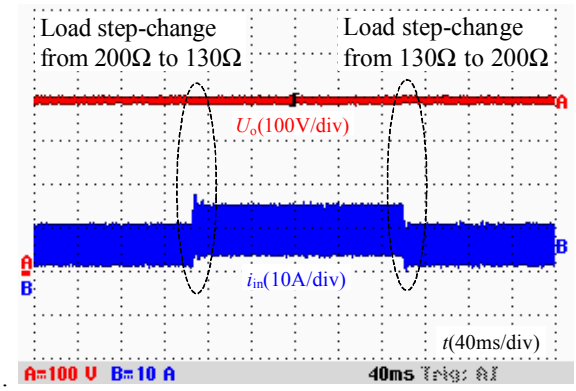


Fig.17 Output voltage and input current with load step-change between 130Ω and 200Ω.

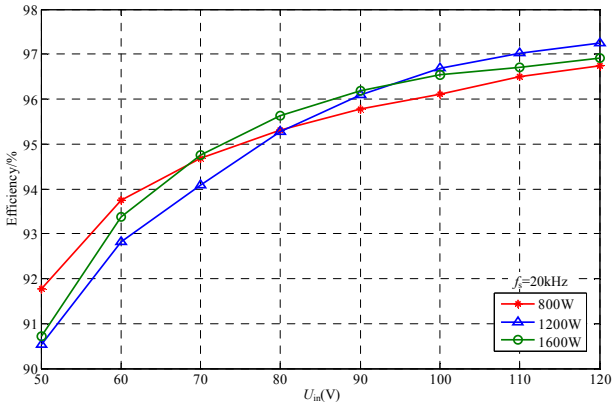


Fig.18 Relationship among efficiency, variable input voltages and different output powers when f_s=20kHz.

VI. CONCLUSION

A single-switch Boost DC-DC converter with a wide voltage-gain range is proposed in this paper. It employs one active power switch and less number of inductors and capacitors to operate over a wide voltage-gain range with the appropriate duty cycle. In addition, the voltage stress across all the semiconductors is as low as 1/*n* of the output voltage, and the potential difference between the input and the output grounds is constant. It is suitable for the power interface of fuel cell vehicles.

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