Design of Low Inductance Switching Power Cell for GaN HEMT Based Inverter

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***Abstract*—In this paper, an ultra-low inductance power cell is designed for a three-Level Active Neutral Point Clamped (3L-ANPC) based on 650 V gallium nitride (GaN) HEMT devices. The 3L-ANPC topology with GaN HEMT devices and the selected modulation scheme suitable for wide-bandgap (WBG) devices are presented. The commutation loops, which mainly contribute to voltage overshoots and increase of switching losses, are discussed. The ultra-low inductance power cell design based on a four-layer Printed Circuit Board (PCB) with the aim to maximize the switching performance of GaN HEMTs is explained. The design of gate drivers for the GaN HEMT devices is presented. Parasitic inductance and resistance of the proposed design are extracted with finite element analysis and discussed. Common-mode behaviours based on the SPICE model of the converter are analyzed. Experimental results on the designed 3L-ANPC with the output power of up to 1 kW are presented, which verifies the performance of the proposed design in terms of ultra-low inductance.**

***Index Terms*—Wide bandgap (WBG) power devices, gallium-nitride (GaN), HEMT, three-level active neutral point clamped (3L-ANPC) converter, photovoltaic (PV) systems, stray inductance.**

I. Introduction

THE 600 V normally-off gallium nitride (GaN) HEMT devices are the perfect candidate for grid-connected applications. Such GaN normally-off HEMT devices have been introduced by Panasonic at 600 V and GaN Systems at 650 V. There are several practical applications with those wide-bandgap (WBG) devices. For instance, in [1], GaN HEMT devices are implemented in a DC/DC converter for the Maximum Power Point Tracking (MPPT) control in PV applications, and the converter exhibited with a peak efficiency of 98.59% at 48 kHz switching frequency. Furthermore, the same devices have been used in other applications such as resonant LLC DC/DC converters, three-phase inverters and synchronous buck converters. Those cases have shown the high switching and conduction performance of the GaN HEMT devices in different operating conditions [2]–[5]. The potential and technology development of GaN devices in power converters is discussed in [2]. Specifically, in [3], GaN devices are adopted on a three-phase inverter with 99.3% efficiency at 900 W output power and 16 kHz switching frequency. The comparison of GaN HEMT with silicon (Si) IGBT is discussed in [4] for high speed motor drive applications. Finally, GaN HEMTs are demonstrated along with 1200 V silicon carbide (SiC) MOSFET devices in single-phase PV applications in [5], where the converter has achieved 99.2% peak efficiency at 1.4 kW output power and 16 kHz switching frequency. The presented converter proves the stable operation of WBG devices under wide load, switching frequency and ambient temperature conditions. Furthermore, normally-on GaN HEMT devices at 600 V voltage class with and without cascode structures are discussed in [6] and [7] for various topologies. More in details, performance improvement in a synchronous buck topology is presented in [6] and it is shown that smaller reverse recovery charge and output capacitance of GaN HEMT devices lead to reduction in turn-on losses and thus up to 2% efficiency improvement in comparison to Si MOSFET. The current collapse phenomena for the 600 V normally-on GaN HEMT is presented in [7]. Although the device is statically rated at 600 V, the experimental results are presented up to 50-60 V due to the increase in on-state voltage drop during dynamic testing. Nevertheless, the results presented in the referenced papers show that WBG-based power converters can achieve very high efficiency even at high switching frequencies, which is not possible with conventional Si-based power devices. Application and implementation challenges and benefits of GaN devices in high density power converters are discussed in [8] and [9]. Finally, reliability-driven assessment of GaN HEMT and Si IGBT devices in PV systems is discussed in [10].

Active Neutral Point Clamped (ANPC) inverter is a member of the half-bridge Neutral Point Clamped (NPC) inverter family and it was introduced in [11] as an alternative to the NPC inverter [12] for improving loss balancing and better utilization of semiconductor chip areas in the inverter. Replacing diodes in the NPC inverters with active switches provides additional zero states, and at the same time different modulation strategies can be applied with a flexible utilization of the redundant switching states. The topology has been discussed thoroughly

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for industrial drive applications in literature [13]–[16]. The schematic of the studied converter for a double-stage three-phase grid-connected PV system is presented in Fig. 1. As it can be observed, each leg of the 3L-ANPC inverter is formed by 6 active switches (S_1-S_{18} of three legs) in order to achieve a three-level phase output voltage with respect to the neutral point N, and the power devices (S_1-S_{18}) are rated at a half of the DC-link voltage V_{DC}. Consequently, it is possible to use GaN HEMT devices at the 600 V class for three-phase grid-connected applications, where the DC link voltage is within a range of 650-1000 V. In this configuration, a DC-DC converter between the PV strings and the 3L-ANPC inverter is adopted in order to flexibly maximize the energy production (i.e., the MPPT control) as well as to extend the operating hours of the PV systems (e.g., in the case of weak solar irradiance). The power delivered by the DC-DC converter is then fed to the 3L-ANPC inverter, while the DC-link voltage is usually maintained as constant by controlling the inverter. Normally, for the PV system, it should inject high-quality grid currents at unity power factor operation, and thus the modulation schemes applied to the 3L-ANPC inverter should be specially designed.

Different modulation strategies can be implemented for the 3L-ANPC inverter in order to achieve a balanced switching loss distribution or doubling of the effective switching frequency at the output [17]. Solutions proposed in [13]–[16] are limited to the use of Si devices and were optimized for IGBT as well as for MOSFET devices. A modulation strategy based on reverse conduction capability of SiC MOSFET devices has been introduced in [18] for a single-phase leg, as further shown in Fig. 2. It can be seen from the driving signals that there are four operating states: 1) positive voltage, 2) zero state positive current, 3) zero state negative current, and 4) negative voltage. Specifically, taking the leg-A shown in Fig. 1 as an example, the positive voltage is applied to the output of the phase leg by turning S_1 and S_3 on and the output current flows through the two devices in series. During the positive active-state, turned-on S_4 ensures an equal DC-link voltage sharing between S_5 and S_6 without conducting any current. The transition from positive active-state to zero-state is accomplished by switching S_1 off, and then simultaneously switching S_2 and S_5 on, and thus the current is divided into two parallel paths: S_2-S_3 and S_4-S_5. The same commutation scheme is used for the complementary switches during the negative active-state and the zero-state. This modulation method ensures low conduction losses at zero-states, and the outer switches (S_1 and S_6) are exposed to switching losses at unity power factor. In a Si-based converter, IGBT devices with antiparallel diodes can be employed; while in the GaN-based converter, only HEMT devices will be sufficient because of the reverse conduction capability of HEMT devices. Therefore, although the number of active devices in Si and GaN will be the same, the number of total switches will be half in GaN-based inverter due to the absence of antiparallel diodes, leading to reduced converter volume as well as heat sink size. In addition to Si IGBT devices, the Si-based super-junction MOSFET at the 600 V class can also be counted as an alternative device type due to its good on-state performance. However, the non-linear behaviour of output capacitance of the super-junction devices places large transient load on the complementary switches and extensive reverse recovery charge increases turn-on losses in hard-switching topologies [5].

Different research groups focused on the study of optimization of layouts for GaN HEMT devices, mainly focused on topologies, where half-bridge based commutation loops are used [19]–[24]. In this paper, an ultra-low stray inductance design for the 3L-ANPC inverter based on 650 V GaN HEMT devices is performed, which was initially presented in [25]. In Section II, the gate driver design for the GaN devices is presented. In Section III, the power cell commutation loop design to achieve ultra-low stray inductance is explained and the finite element based analysis results for the stray inductance and stray resistance of the design are presented. The common-mode challenges of the proposed design are discussed in Section IV. Finally, experimental results are presented in Section V.

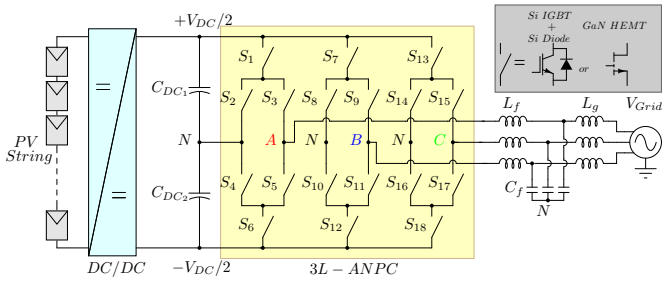


Fig. 1: Grid-connected three-phase double-stage 3L-ANPC inverter with an LCL filter in PV applications.

II. Gate Driver Design

The part number of the devices used in this paper is GS66508T, a normally-off enhancement mode 650 V, 30 A HEMT from GaN Systems. The device parameters are presented in Table I. Although the device is a normally-off e-HEMT, the gate threshold voltage (V_{th}) and input capacitance (C_{iss}) are significantly lower in comparison to Si-based MOSFET or IGBT devices. Therefore, a low inductance gate driver is required with immunity to cross-talking between commutating switches due to the high dV/dt capability of GaN HEMT devices.

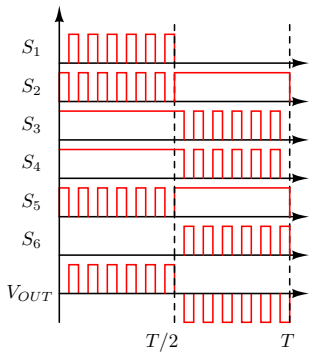


Fig. 2: Switching sequences for the leg-A of the 3L-ANPC inverter [18].

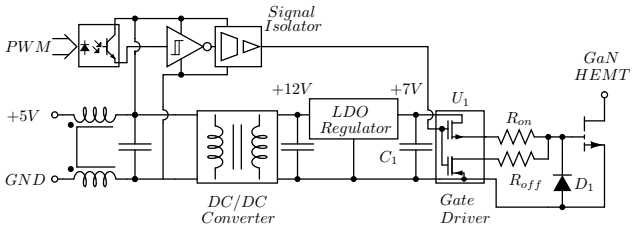


Fig. 3: Gate driver design for the GaN HEMT.

The proposed isolated gate drive design for the GaN HEMT devices is presented in Fig. 3. The pulse width modulation (PWM) signal to each switch is transferred by a fibre optic link from the control board and passed through an inverting Schmitt trigger in order to avoid any false turn-on or turn-off triggering. The signal is then fed to a digital signal isolator for transferring of the PWM signal to the isolated gate driver circuit with high common-mode dV/dt immunity and low propagation delay. In this arrangement, the Si861x series from Silicon Labs is used as the signal isolator with 50 kV/μs common-mode dV/dt immunity and 10 ns propagation delay. The device also provides 5 kV RMS (Root Mean Square) electrical isolation between input and output stages. For the power transfer to the gate driver circuit at the isolated side, a regulated DC/DC converter with 1 W, +12 V single output and 3 kV DC isolation capability is used. Ideally, the isolation capacitance should be as small as possible in order to avoid interaction between the floating gate driver circuit and the non-isolated logic stage. The selected DC/DC converter has 30 pF isolation capacitance. The +12 V output of the converter is then fed to low-drop out (LDO) regulator to provide +7 V for the supply of the non-isolated gate driver. UCC27511 from Texas Instruments is selected as the gate driver IC, which provides split outputs with 4 A and 8 A source and sink peak current capability, respectively. The separation of turn-on and turn-off paths provides optimization of turn-on and turn-off speeds independently for the GaN HEMT along with providing immunity to the Miller capacitance caused by turn-on behaviours. As the turn-off resistor R_{off} provides a low impedance path for positive dV/dt only; during negative dV/dt across the device, the Miller current will flow through the turn-on resistor R_{on}, which is generally selected larger than R_{off}, and create negative spikes across the device gate and source terminals. Depending on the resistance value of R_{on} and dV/dt, the negative spike can reach or exceed the limits of the device presented in Table I. Therefore, a clamping Schottky barrier diode D_1 (PMEG2010EPK) with 25 pF junction capacitance at 10 V reverse voltage, across gate and source of the device, as presented in Fig. 3, provides a current path for the Miller current during negative high dV/dt conditions. According to these considerations, R_{on} and R_{off} are chosen as 15 Ω and 1.5 Ω, respectively.

The PCB design for the isolated stage of the GaN HEMT gate driver is shown in Fig. 4. The design is based on a two-layer PCB with surface mount components in order to achieve low stray inductance for high speed operation. As the gate charge of the GaN HEMT is significantly lower than SiC- or Si-based devices with similar current and voltage ratings, low power surface mount packages (e.g., 0603) are used to reduce the footprint of the circuit and also to minimize the gate loop inductance.

TABLE I: GS66508T GaN HEMT Parameters.

Drain-Source Voltage (V_{DS})	650 V
Continuous Drain Current (I_{DS})	23 A @ 100 ^{o}C
Drain-Source On-State Resistance ($R_{DS_{ON}}$)	55 mΩ @ 25 ^{o}C
	129 mΩ @ 100 ^{o}C
Input Capacitance (C_{iss})	200 pF
Output Capacitance (C_{oss})	67 pF
Reverse Transfer (C_{rss})	2 pF
Gate Charge (Q_g)	6.5 nC
Min. Gate Threshold Voltage (V_{th})	1.6 V
Gate-Source Voltage (V_{GS})	-10 to +7 V
Maximum Junction Temperature (T_j)	150 ^{o}C
Reverse Recovery Charge (Q_{rr})	0 μC
Package Stray Inductance (L_σ)	0.4 nH
Device Package	GaN$_{PX}$

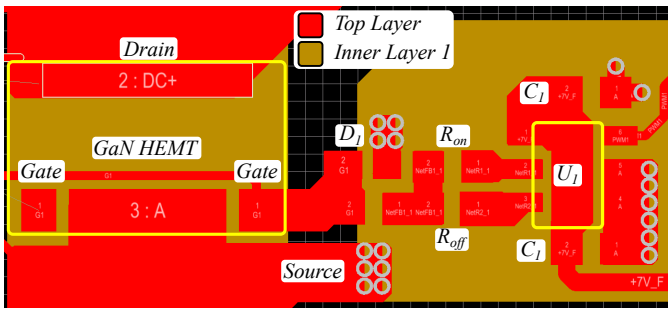


Fig. 4: PCB design for GaN HEMT gate driver.

III. Commutation Loop Design

The 3L-ANPC topology provides six different switching states (two for active-states $+V_{DC}/2$ and $-V_{DC}/2$, four for zero-states) for IGBT-based applications. The switching states and commutation schemes are discussed thoroughly for loss balancing and better utilization of Si IGBT devices. In literature, the parallel conduction of S_2, S_3, S_4 and S_5 has not been considered as a switching state due to the difficulty of the parallel conduction of these IGBT devices [11]. With respect to any selected switching strategy, S_1 or S_3 may be subject to switching losses for the positive output voltage and positive output current. In the selected switching strategy presented in Fig. 2, S_1 and S_6 switches will be subject to switching losses at positive and negative halves of the output waveform, respectively with unity power factor operation. The possible commutation loops that can be used for commutating the output current between positive state and upper and lower neutral states formed by $S_2 - S_5$ are presented in Fig. 5. The total commutation inductance formed by the commutation loop stray inductance L_σ and the DC-link capacitor self-inductance L_{DC1} has to be minimized for reducing voltage overshoots and switching losses. The self-inductance of the DC-link capacitor can be minimized by paralleling high frequency capacitors (e.g., ceramic and film) and the commutation loop inductance

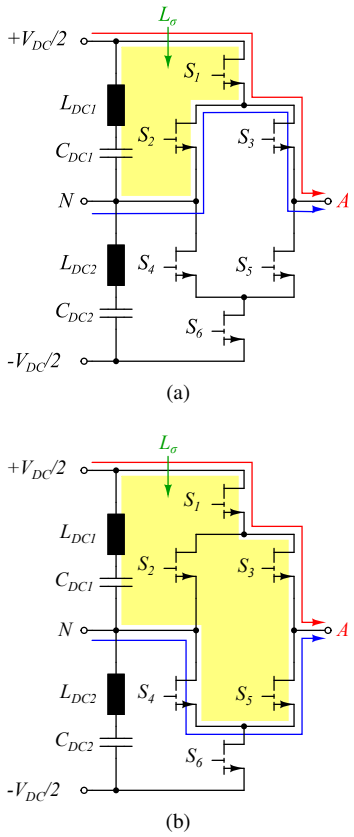


Fig. 5: Commutation loops in the 3L-ANPC from positive to neutral states: (a) positive state to upper neutral state and (b) positive state to lower neutral state.

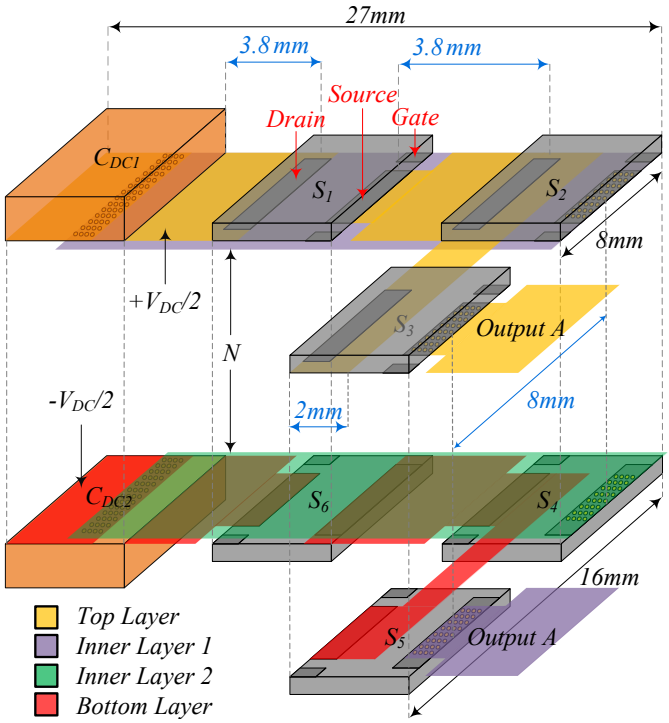


Fig. 6: Power cell design in a 4-layer PCB for ultra-low loop inductance.

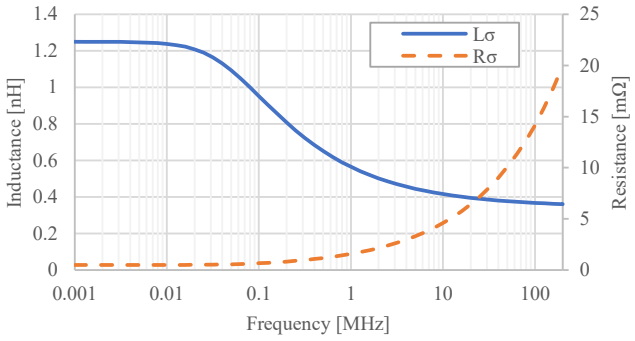
by placing conductors that carry opposing currents in adjacent layers to induce a magnetic field for self-cancellation.

The proposed low inductance commutation loop design for the 3L-ANPC inverter is presented in Fig. 6. It is worth to note that the proposed layout is realized with a low inductance surface mount package of GaN HEMT devices. The packaging technology eliminates bond wires and solder joints with extremely low stray inductance of 0.4 nH per device [26]. It is the stray inductance that is a key to achieve high switching speeds while low voltage overshoots and switching losses. In comparison to the conventional TO-220 package, the stray inductance of the GaN HEMT package has 17.5 times less stray inductance. Six GaN HEMT switches $S_1 - S_6$ are placed on a 4-layer PCB with symmetrical layout where $S_1 - S_3$ are placed on the top side and $S_4 - S_6$ are placed on the bottom side. $S_1 - S_6$, $S_2 - S_4$, $S_3 - S_5$ switch pairs are vertically aligned for providing symmetry between upper and lower sides of the 3L-ANPC phase leg. Top layer and bottom layer of the PCB are used for interconnection of DC-link capacitors, switches and connection to $+V_{DC}/2$ and $-V_{DC}/2$; while inner layers are used as return paths and connection to the neutral point.

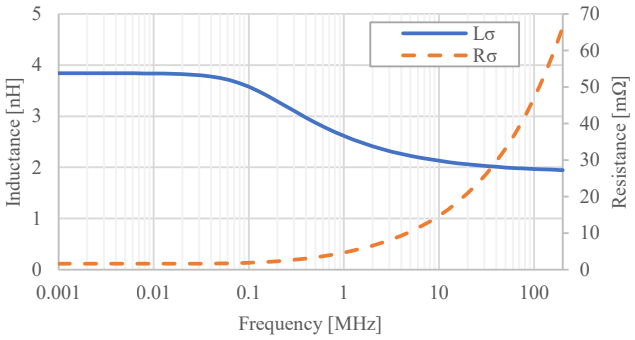
The stray inductance for each commutation loops presented in Fig. 5(a) and 5(b) can be approximately calculated using the dimensions in Fig. 6, 0.2 mm PCB material thickness between layers and the well-known equation of the loop inductance:

$$L_\sigma = \frac{\mu_r \cdot \mu_0 \cdot h \cdot l}{w} \tag{1}$$

where h is the height, l is the length and w is the width of the commutation loop, μ_r is the relative permeability of the PCB material (FR4) and μ_0 is the permeability of air. The equivalent series inductance L_{DC1-2} of 1 μF, 500 V Ceralink capacitors presented as C_{DC1} and C_{DC2} in Fig. 6 is 2.5 nH per capacitor. The self-inductance of the GaN HEMT package is 0.4 nH per device. The total commutation inductance, which includes the stray inductance, DC-link capacitor self-inductance and GaN package inductance, is calculated as 3.51 nH and 5.37 nH for commutation loops presented in Fig. 5(a) and 5(b) respectively. Therefore, the presented structure minimizes the commutation loop inductances presented in Fig. 3 and enables very high switching performance of the GaN HEMT in the 3L-ANPC topology. In addition to the above analytical estimation, the finite element analysis for the proposed layout is conducted with ANSYS Q3D software at different frequencies in order to estimate the stray inductance L_σ and stray resistance R_σ of the commutation loops excluding the stray inductance and resistance of DC link capacitors, and excluding on-state resistance of GaN HEMTs [27]. In the finite element model, GaN devices are modelled as copper planes due to the package design, which is based on planar copper interconnects between the package terminals and GaN HEMT die. The simulation results for loop 1 in Fig. 5a and loop 2 in Fig. 5b are presented in Figs. 7a and 7b respectively. It can be seen that the finite element simulation results are well aligned with the analytical estimations, verfying the approach to obtain low stray inductance design for both commutation loops. The



(a)

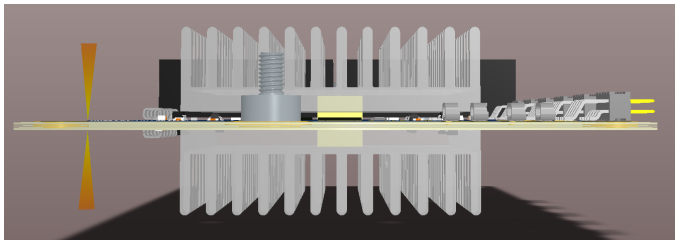


(b)

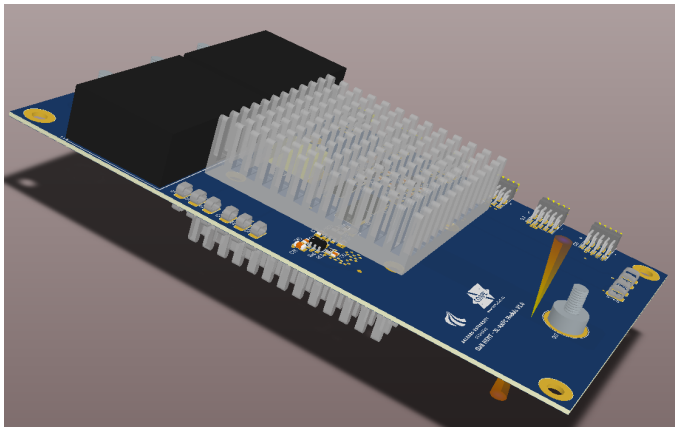
Fig. 7: Finite element analysis results for the stray inductance and resistance of the PCB layout presented in Fig. 5: (a) commutation loop in Fig. 5a and (b) commutation loop in Fig. 5b.

unbalanced stray inductance between two loops, presented in this case, can be acceptable in the view of very small values such as in this design. In other words, low stray inductance and minimum mismatch between the stray inductance values of the commutation loops are essential for better utilization of different switching states in WBG based multi level inverters.

The cooling design for the double-sided PCB layout is presented in Fig. 8. The GaN HEMT device used in this work has cooling pad on the top side of the device package, which is connected to the substrate of the GaN HEMT die. Therefore, the cooling pad has to be isolated where the common heat sink is used to cool multiple devices. The system consists of two heat sinks, which are mounted with spring loaded screws on the PCB for optimal mechanical pressure and thermal interface material between device cooling pads and heat sinks. The two heat sinks, one for top side devices S_{1-3} and one for bottom devices S_{3-6}, provide symmetrical cooling arrangement for the phase leg. The heat sinks can be connected to a larger cooling system in a vertical stacking arrangement in the case of multiphase operation, such as three-phase grid-connected systems. The thermal interface material provides electrical isolation of cooling pads with minimum thermal impedance between the junction and heat sink. Due to low profile design of the PCB, the heat sink is not obstructed by the gate driver components on the board and can be extended to improve the power dissipation for high switching frequency operations.



(a)



(b)

Fig. 8: Double-sided heat sink mounting for the proposed PCB layout: (a) side view and (b) overall view.

IV. Common-Mode Analysis

The proposed four-layer power cell design provides low inductance commutation loops by overlapping GaN devices on the top and bottom layers of the power cell PCB. Due to the overlap, top devices use top layer and inner layer 1 for gate drive circuits and bottom devices use upper layer 2 and bottom layer for gate drive circuits. The overlap of gate drive planes and tracks create a parasitic capacitance path between drain and source nodes of overlapping devices and presented as C_{S1}, C_{S2}, C_{S3} and C_{S4} in Fig. 9. The parasitic capacitances can be calculated by:

$$C_s = \frac{k \cdot \epsilon_0 \cdot A}{d} \tag{2}$$

where k is the relative permittivity of the dielectric material between each PCB layer, ϵ_0 is the permittivity of pace, A is the overlapping area of planes, and d is the thickness of FR4 between each layer. According to material properties and the calculated overlapping areas, the parasitic capacitance C_{S1}, C_{S2}, C_{S3} and C_{S4} are 57.4 pF, 43 pF, 44.7 pF and 17 pF.

Based on the gate driver design explained in Section II and by using the SPICE models of the GaN HEMT and the gate driver components (e.g., the gate driver IC and the DC/DC converter) from manufacturers, a SPICE-based model is built for common-mode analysis. The circuit presented in Fig. 9 is simulated for the positive half-cycle of the output voltage in LTSpice. This is to investigate the peak common mode current flowing through the parasitic capacitance and the logic circuit, which is independent of the switching frequency. The gate resistors are kept the same with the actual design, which

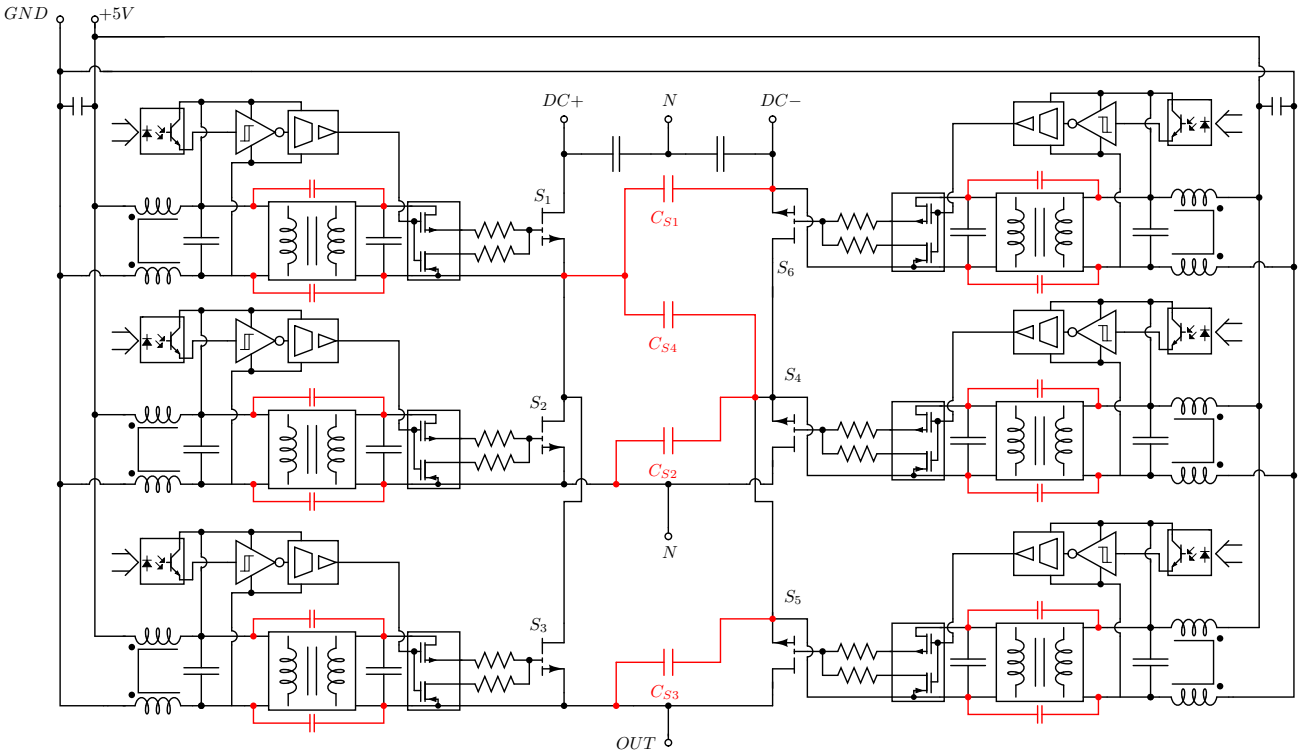


Fig. 9: Single-phase 3L-ANPC switching cell with parasitic capacitance.

are 15 Ω and 5 Ω for turn-on and turn-off, respectively. The stray capacitance of the DC/DC converters for gate drivers is chosen as 30 pF, which is specified in the manufacturer datasheet. In the simulation, the common-mode inductor at the input of each gate driver is omitted in order to evaluate the current flowing through the non-isolated side of the circuit. The common-mode currents through parasitic capacitances C_{S1}-C_{S4} with respect to a rise of the output voltage from 0 to 350 V, with a 700 V DC link voltage, are presented in Fig. 10. The results show that the parasitic capacitance causes the circulating current flow between devices with a large amplitude due to the high dV/dt. The impact of this current flowing to the non-isolated logic side due to the isolation capacitance of the DC/DC converters is presented in Fig. 11. Although the amplitude of the common-mode current at the non-isolated stage is significantly lower, it is still higher than logic current levels and can interfere with signal conditioning, causing false triggering. In order to suppress the common-mode current flowing through the non-isolated stage, common-mode chokes with a value of 470 μH are placed at the input of each gate driver. The placement of the common-mode chokes prevents the common-mode current to flow through the non-isolated side of the circuit and contains the current circulation within the power cell. In order to fully eliminate the common-mode current circulation, the additional plane can be introduced between inner layer 1 and inner layer 2 with the penalty of increasing the number of layers from 4 to 6. Another possibility is replacement of gate drive planes to avoid any overlaps between top- and bottom-side gate drive circuits for the switches. This arrangement may increase the PCB design complexity.

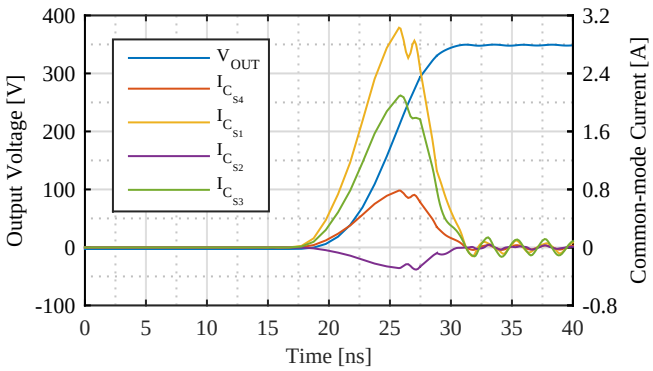


Fig. 10: Simulated common-mode currents through the parasitic capacitors with respect to the output voltage rise.

V. Experimental Results

The performance of 600 V Si IGBT devices has been well studied in literature for different applications and some of these results have been discussed in the literature. On the other hand, normally-off 650 V GaN HEMT devices with low inductance package recently emerged for power electronic applications. Therefore, a GaN HEMT based single-phase 3L-ANPC inverter demonstrator has been designed and built-up. The performance of the GaN HEMT devices is experimentally evaluated and presented in this section.

The GaN HEMT based single-phase 3L-ANPC inverter is presented in Fig. 12(a) and 12(b). The power cell is formed

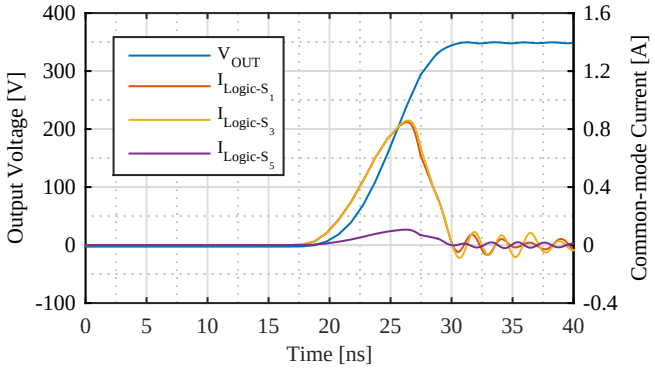
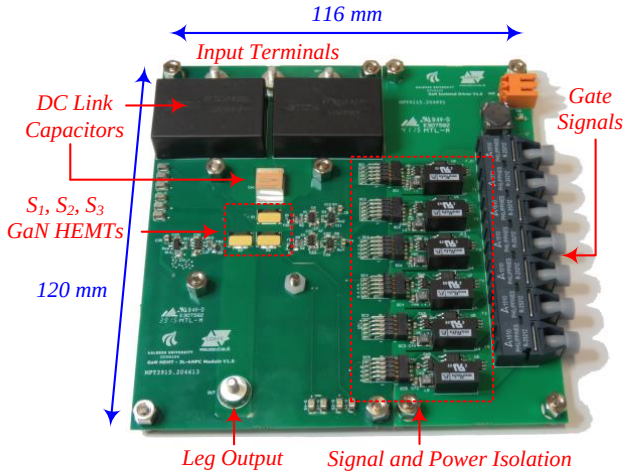
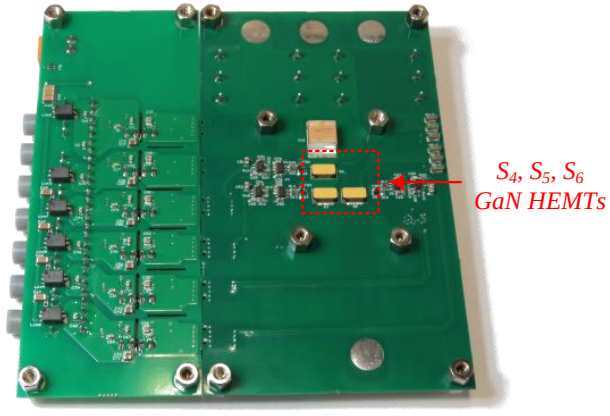


Fig. 11: Simulated common-mode currents through the non-isolated logic circuits with respect to the output voltage rise.



(a)



(b)

Fig. 12: Hardware of the GaN HEMT based single-phase 3L-ANPC power cell: (a) top view and (b) bottom view.

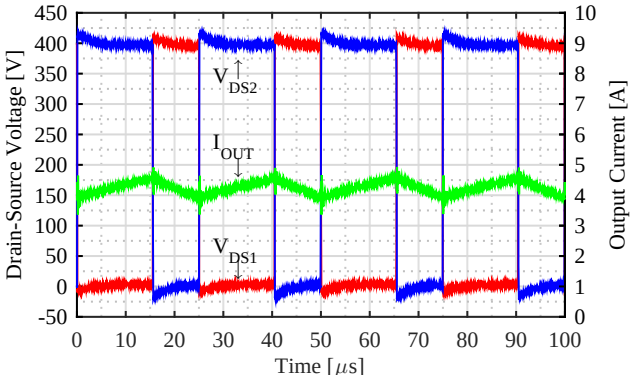


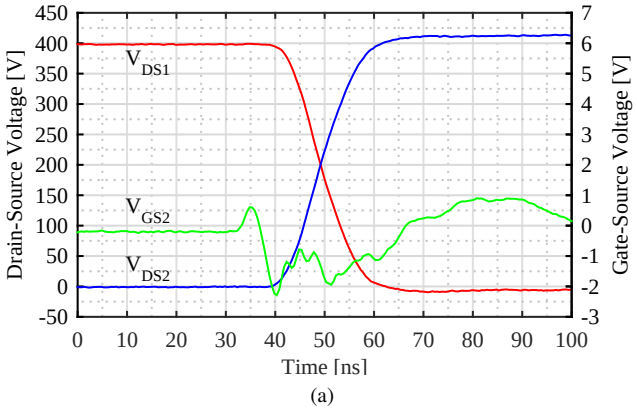
Fig. 13: Performance of the GaN HEMT in the 3L-ANPC inverter with buck configuration.

by a four-layer PCB with 140 μm copper on each layer. The power cell consists of high frequency DC link capacitors, GaN HEMT switches, gate drivers, signal and power isolation circuits for gate drivers and fibre optic receivers for gate signals. The GaN devices $S_1 - S_3$ are placed on the top side of the PCB while the GaN devices $S_4 - S_6$ are placed on the bottom side of the PCB in symmetry to $S_1 - S_3$ for minimized commutation loop at a high switching speed. The PCB is designed to have a modular system with the option to extend the demonstrator to a three-phase inverter by stacking PCBs vertically. Regarding cooling of power switches, two commercial heat sinks are used. The heat sinks are joined by 4 screws with compression springs in order to apply equal contact pressure to the devices from the top and the bottom part of the PCB. The PCB has been presented without heat sinks in order to clearly show device positions on the board.

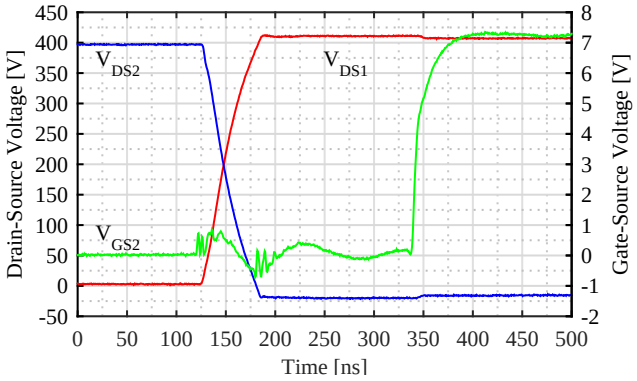
A. Switching Performance

The 3L-ANPC power cell is initially operated as a buck DC/DC converter in order to evaluate the functionality of the manufactured board and the switching performance of GaN devices and the designed power cell. For the buck configuration, upper switches $S_1 - S_3$ are used where S_3 is kept on during the switching period and complementary gate signals are applied to S_1 and S_2 with 200 ns dead-time.

Under normal operations and with a total 800 V DC link voltage, the devices in 3L-ANPC topology are subject to half of the DC link voltage. Thus, switching performance is evaluated at the 400 V blocking voltage. The switching waveforms at 40 kHz switching frequency with a 400 V DC link voltage and 1 kW output power are presented in Figs. 13 and 14. The successful operation of switches in the buck configuration is presented in Fig. 13 with device voltages and output current. In Fig. 14(a), the output current commutates from S_2 to S_1 and S_1 is subject to hard-switching. The commutation from S_1 to the reverse conduction of S_2 is presented in Fig. 14(b). Drain-source voltage waveforms V_{DS1} and V_{DS2} prove the high switching speed of GaN HEMT devices with 13.2 ns rise and fall time of V_{DS2} and V_{DS1} respectively.

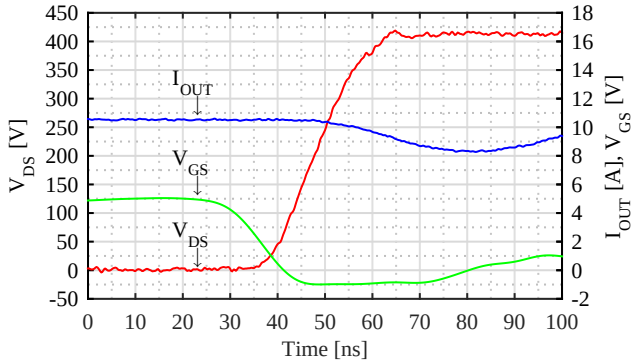


(a)

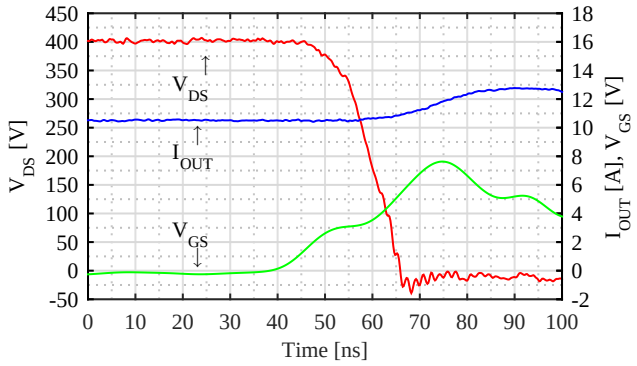


(b)

Fig. 14: Switching performance of the GaN HEMT in the 3L-ANPC inverter: (device drain-source voltage and gate-source voltage): (a) turn-on of S_1 and (b) turn-off of S_1 waveforms with the buck configuration.



(a)



(b)

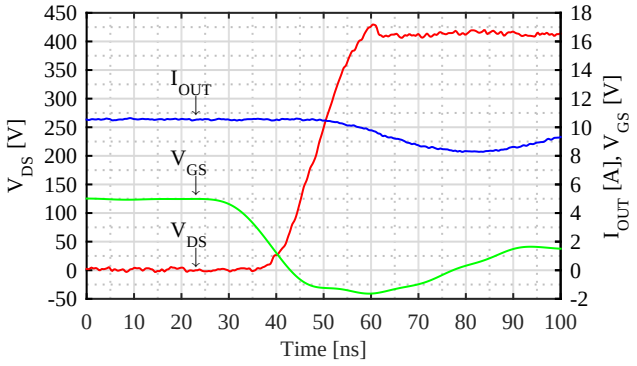
Fig. 15: Switching waveforms of S_1 in the commutation loop presented in Fig. 5a for: (a) turn-off and (b) turn-on.

In addition to the tests in the buck configuration, a double-pulse test is conducted at the 400 V blocking voltage for the commutation loops presented in Fig. 5 to evaluate the design and verify the low inductance under hard switching conditions. The switching performance of S_1 in the first commutation loop in Fig. 5a is presented in Fig. 15, where the turn-on dynamics of the commutation loop are also plotted. In this case, the commutation cell is formed by switches S_1 and S_2, and S_1 is subject to hard switching. It can be seen in Fig. 15 that at 10.5 A output current, the maximum turn-off drain-source voltage across the device is limited to 419 V. The performance of S_1 under the same operating conditions (400 V DC link voltage, 10.5 A output current, and double-pulse test) in the second commutation loop in Fig. 5a is presented in Fig. 16. In this case, the commutation cell is formed by S_1 and S_5. As the calculated stray inductance for this configuration is higher, the maximum turn-off drain-source voltage across the device is 429 V, 10 V higher than the case in Fig. 15a. Furthermore, it is observed in Fig. 15 that, the dV/dt across the device is around 25 V/ns at turn-off and 30 V/ns at turn-on and in Fig. 16, the dV/dt at turn-off and turn-on is around 31 V/ns and 50 V/ns, respectively. In addition to this, it can be seen that the turn-on performance of S_1 in the buck arrangement in Fig. 14a and the double-pulse test result in Fig. 16 are in a close agreement despite the fact that the drain-source current of S_1 is doubled in the inverter arrangement. The experimental results also validate the dV/dt of the voltage waveforms used in the LTSpice simulation for the analysis of the common-mode currents.

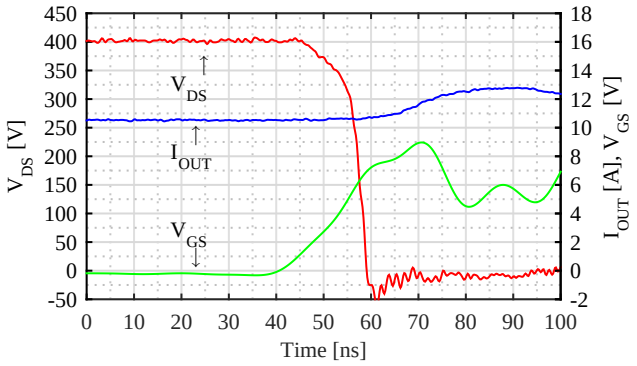
B. Inverter Performance

The single-phase 3L-ANPC inverter prototype in Fig. 12 is tested with the 700 V DC link voltage and 10 kHz switching frequency to demonstrate the performance of the GaN-based power cell without any heat sink. The inverter test setup is presented in Fig. 17. The inverter is powered by a DC power supply with DC link decoupling capacitors. An RL load configuration is used for evaluation of the performance under different load conditions. Efficiency and losses of the power cell are measured by a Yokogawa WT3000E precision power analyser with high accuracy.

The experimental output current and voltage waveforms, and power cell efficiency with experimental and simulation results, which are obtained from PLECS model, are presented in Fig. 18(a) and (b), respectively. The loss model in PLECS is based on manufacturer datasheet. The experimental results support the validity of high performance of GaN HEMT devices in simulations compared with Si IGBT devices. The efficiency comparison in Fig. 18(b) validates the high perfor-



(a)



(b)

Fig. 16: Switching waveforms of S_1 in the commutation loop presented in Fig. 5b for: (a) turn-off and (b) turn-on.

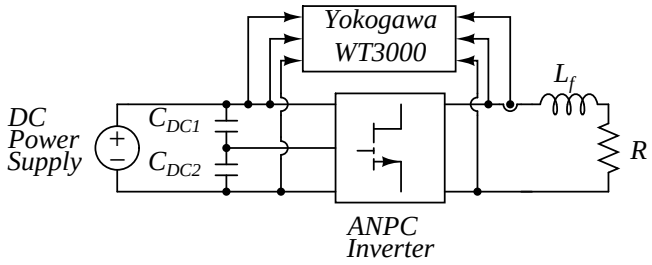
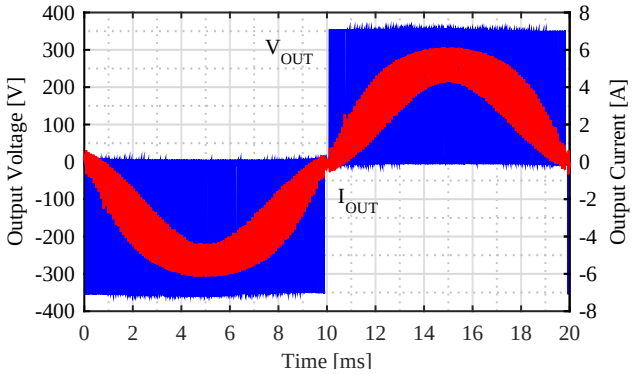


Fig. 17: Inverter test setup.

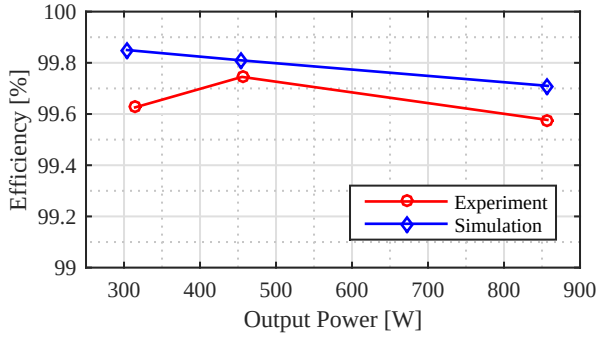
mance assumption of the GaN HEMT devices in the inverter operation mode.

VI. Conclusion

In this paper, an ultra-low inductance power cell design for the 3L-ANPC topology with low inductance surface mount package GaN HEMT devices has been presented and demonstrated with finite element analysis and experimental characterization. The finite element analysis shows that proposed layout can provide very low stray inductance for the possible commutation loops in the GaN HEMT based 3L-ANPC leg. The experimental results show that with the proposed layout, 13 ns rise time at 400 V blocking can be achieved with a 20 V voltage overshoot at 1 kW output power. The layout also comes with the challenge of the common-mode current



(a)



(b)

Fig. 18: (a) Experimental output voltage and current waveforms at 800 W output power and (b) efficiency of the 3L-ANPC power cell with experimental and simulation results.

circulation that can be eliminated by rearranging the gate drive placement carefully or by introducing shielding between the top and bottom device gate drive circuitries. The double-pulse tests for the possible commutation loops in the designed 3L-ANPC have demonstrated that the stray inductance is minimized with the proposed PCB layout. As part of the future work, the optimization of switching frequency with respect to the output filter size and converter efficiency can be carried out.

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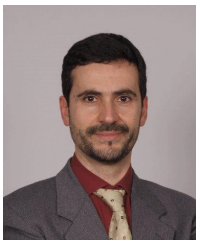

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