Comparative Stability Analysis of Droop Control Approaches in Voltage-Source-Converter-Based DC Microgrids

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***Abstract*—Droop control has been widely applied in DC microgrids (MGs) due to its inherent modularity and ease of implementation. Among the different droop control methods that can be adopted in DC MGs, two options have been considered in this paper; I-V and V-I droop. I-V droop controls the DC current depending on the DC voltage whilst V-I droop regulates the DC voltage based on the output current. The paper proposes a comparative study of V-I/I-V droop control approaches in DC MGs focusing on steady-state power sharing performance and stability. The paper presents the control scheme for current-mode (I-V droop) and voltage-mode (V-I droop) systems, derives the corresponding output impedance of the source subsystem including converters dynamics and analyzes the stability of the power system when supplying constant power loads. The paper investigates first the impact on stability of the key parameters including droop gains, local control loop dynamics and number of sources and then performs a comparison between current-mode and voltage-mode systems in terms of stability. In addition, a generalized analytical impedance model of a multi-source, multi-load power system is presented to investigate stability in a more realistic scenario. For this purpose, the paper proposes the concept of "global droop gain" as an important factor to determine the stability behaviour of a parallel sources based DC system. The theoretical analysis has been validated with experimental results from a laboratory-scale DC MG.**

***Index Terms*— Impedance, droop control, DC power system, multiple source, constant power load, stability.**

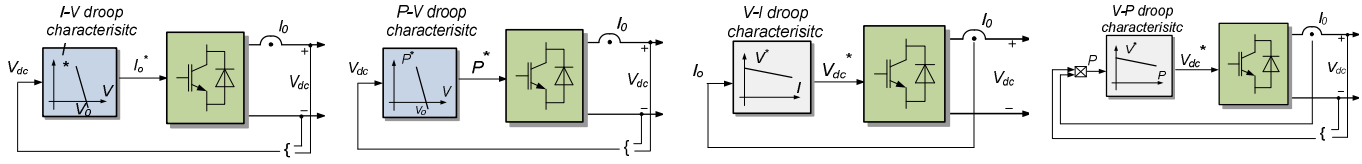
I. INTRODUCTION

In the past decade, increased awareness of limited energy resources has driven a considerable effort towards the integration of renewable distributed generators (DG) such as wind turbines, photovoltaic and energy storage devices into the AC distribution system. At the same time, DC microgrids (MGs) have been successfully used in automotive, high speed rail and aerospace applications [1], [2], due to the rapid growth of power electronics technology. The extension of DC systems to power distribution, including residential networks, has been often envisioned [3], [4]. Many renewable sources of electrical energy are inherently DC (photovoltaic, fuel-cells, energy storage) and also most the loads are DC based. A DC architecture would therefore reduce the number of power conversion stages, leading to a simpler structure with lower cost, higher efficiency and absence of reactive power compensation [5]-[9].

Typical loads in a DC MG include voltage controlled DC-DC converters and speed controlled motor drives which behave like constant power loads (CPLs) [10]. The negative incremental impedance shown by CPLs can undermine the stability of the DC MG [11]-[13], and their impact must be carefully considered during the design stage.

A DC MG architecture can also incorporate the parallel operation of multiple, dissimilar electrical energy sources. The expected benefits of using parallel energy sources include reduction of the total weight of the main generators, convenient integration of energy storage devices and improvements in power system redundancy. Existing control methods that guarantee power sharing can be divided into two categories; active load sharing and passive load sharing [15], [16]. For active load sharing schemes, three approaches are popular; master-slave (MS) control [17], [18], centralized control [19] and average current control [20]. The common drawback of these approaches is the need for a communication infrastructure linking the parallel modules. System reliability strictly depends on the reliability of the communication system. In addition, in the master-slave and centralised approaches, a failure in the master or central controller will lead to system failure. On the other hand, most of the recent research is focused on passive load sharing (decentralized control method), for example, droop control [21], [22]. In decentralized control methods, parallel modules operate independently using local measurements. Since no critical communication link is needed, system cost is reduced and reliability is improved. The basic concept of droop control is implemented by adding a "virtual resistance" into the existing local voltage controllers, enabling parallel operation. Due to its modularity and reliability, droop control has been successfully applied in DC systems [23]-[26].

Existing droop control methods for voltage source converters (VSCs)-based DC MGs implement the basic concept of droop in different ways and can be grouped in two families; current/power mode droop, including Current-Voltage (I-V) and Power-Voltage (P-V) strategies and voltage mode droop, including V-I and V-P strategies [27]. The I-V and P-V droop methods are shown in Fig. 1(a) and (b) [28]-[31]. In the implementation of these control methods, the DC voltage is measured and the injected current/power is controlled according to the droop curve. Alternatively, in the V-I and V-P methods shown in Fig. 1(c) and (d) current or power is measured and the DC voltage is regulated accordingly [32], [33].



(a) (b) (c) (d)

Fig. 1. Droop characteristic employed in VSCs. (a) I-V droop. (b) P-V droop. (c) V-I droop. (d) V-P droop.

In [35], I-V and P-V demonstrated similar performance and for this reason only I-V droop is considered in this paper as a representative of the current/power mode strategies. For current-mode droop control, the effect of the passive components (DC link capacitor, feeder impedance) and the power of CPLs on the stability margin have been investigated in [36], [37]. It is known

that the stability margin increases with an increase of DC link capacitance, decrease of feeder inductance and decrease of load power. Nevertheless, the effect of local control bandwidth and droop gains on stability has not been fully investigated.

Similarly, only V-I droop is investigated within the voltage mode methods [33], [34]. A hierarchical control scheme using V-I droop characteristics for a parallel AC-DC converter interfaced hybrid MG is presented in [33]. Within [33] the effect of the delay between secondary control (voltage restoration) and primary control (local DC voltage) on system stability is investigated. However, the effect of local control bandwidth and droop gains on stability is not fully assessed. Stability of a low voltage DC system is studied including the cable effects in [34]. In that paper the sufficient condition for stable operation is discussed but the impact of different droop methods is not considered.

In VSC-based DC MGs, systems using different droop approaches (current/power mode or voltage mode) may show different stability boundaries. However, until now there are no reports dealing with the performance comparison of the current-mode vs. voltage-mode droop-controlled systems in terms of stability. To fill this gap, this paper presents a comparison of steady state power sharing performance and stability of these two droop strategies applied to a multi-source DC MG. The main contributions of the paper can be summarized as follows:

(1) The effect of droop gain and local control bandwidth on system stability is investigated with a comparative approach. Moreover, state-space models and impedance models of both droop control strategies are presented and a stability analysis comparison is conducted. It will be shown in this paper that the current-mode droop-controlled system faces instability challenges under small droop gain whist the voltage-mode system can operate over a wider range of droop gain.

(2) Global droop gain, an important factor to facilitate the analysis of main bus V-I characteristic, is proposed in the paper and its impact on system stability is investigated in a generalized multiple source multiple load DC MG.

The paper is organized as follows. In Section II, different droop control schemes are shown and the corresponding control block diagrams are developed. Section III discusses the source impedances during single source operation for each droop control approach and compares the corresponding stability boundary in terms of droop gain and local control bandwidth. In Section IV, the impedance model of the generalized system consisting of multiple sources and loads is derived and the comparative stability analysis is conducted by means of Nyquist contours for parallel operation. Section V shows the experimental results to validate the theoretical analysis. Finally, the main conclusions are summarized in Section VI.

II. Current Mode (I-V) and Voltage Mode (V-I) Droop Control Strategies

Fig. 2 shows the equivalent circuit of a single bus DC MG with multiple sources and loads. The main DC bus is fed by two-level, three phase active rectifiers AR_1-AR_n powered by sources G_1-G_n (local generators or AC grid). C_1-C_n correspond to the local converter output capacitors (local buses) and C_b is a common capacitor bank installed on the main 270V DC bus. This architecture is based on a potential DC power system in future more electric aircraft [38] which can be considered as a

challenging case of DC MGs in islanding mode. Typical loads in the system consist of tightly controlled DC/DC converters, motor drives and resistive loads. The basic vector control scheme for the VSC is shown in Fig. 3.

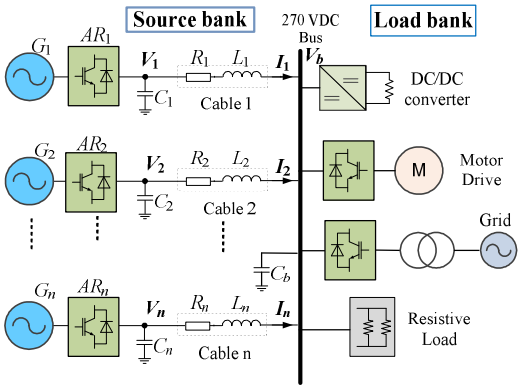


Fig. 2. Power system architecture under study.

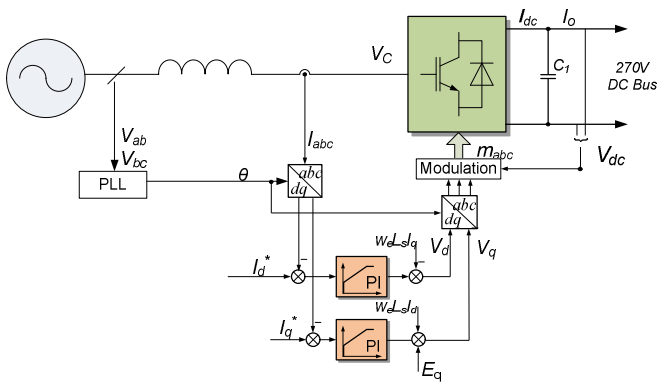


Fig. 3. Vector control strategy for the VSC.

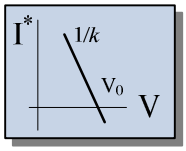
Depending on the DC control strategy, the converter can be operated either in current-mode or in voltage-mode [27]. The current-mode droop control scheme is shown in Fig. 4(b) with the current reference derived from the I-V droop characteristic in Fig. 4(a), based on the DC voltage measurement as shown below,

$$I_{dc}^{*} = \frac{V_o - V_{dc}}{k} \tag{1}$$

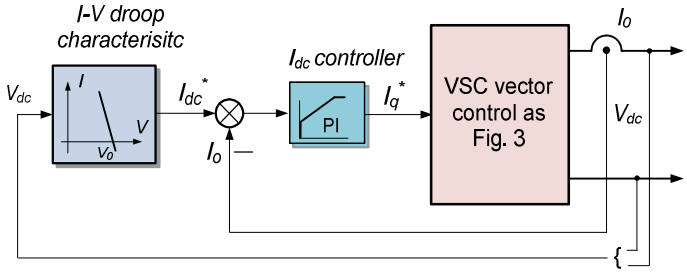
where V_o is the nominal bus voltage (270V); k is the droop gain; V_{dc} is the DC voltage measurement; I_{dc}^{*} is the generated DC current reference.

The control scheme for voltage-mode droop-controlled VSC is shown in Fig. 5(b). As expressed in (2), the DC voltage reference is generated according to the branch output DC current using the V-I droop characteristic shown in Fig. 5(a).

$$V_{dc}^{*} = V_o - kI_{dc} \tag{2}$$



(a)



(b)

Fig. 4. I-V droop and its corresponding *current-mode* control scheme. (a) I-V droop characteristic. (b) Current-mode control scheme.

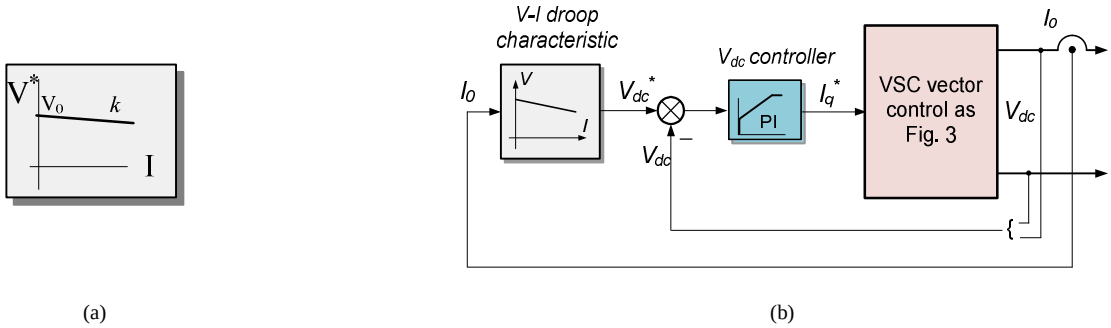


Fig. 5. V-I droop and its corresponding *voltage-mode* control scheme. (a) V-I droop characteristic. (b) Voltage-mode control scheme.

A. Power Sharing Performance

For *current-mode* systems, I_{dc}^{*} can be generated by measuring either the local output voltage V_i (local voltage feedback, LVF) or the main bus voltage V_b (global voltage feedback, GVF). The two approaches are shown in Fig. 6.

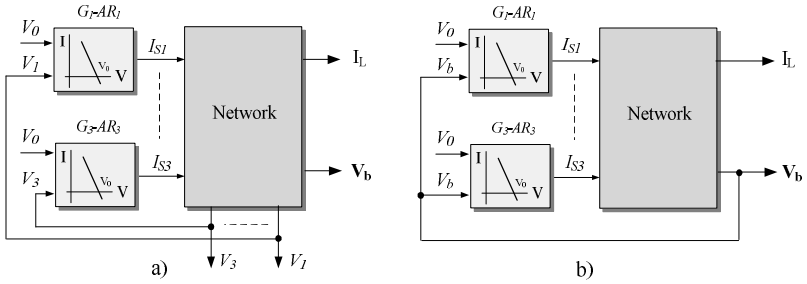


Fig. 6. Current-mode approaches. (a) LVF. (b) GVF.

Current sharing in steady-state among the parallel branches for LVF and GVF can be derived in (3) [27],

$$\begin{cases} I_1 : I_2 : \cdots : I_n = \dfrac{1}{k_1 + R_1} : \dfrac{1}{k_2 + R_2} : \cdots : \dfrac{1}{k_n + R_n} & \text{(Current mode-LVF)} \\ I_1 : I_2 : \cdots : I_n = \dfrac{1}{k_1} : \dfrac{1}{k_2} : \cdots : \dfrac{1}{k_n} & \text{(Current mode-GVF)} \end{cases} \tag{3}$$

where k_1, k_2, k_n are the droop coefficients for parallel modules and R_1, R_2, R_n are the cable resistances. Equation (3) shows how in current-mode droop with GVF the current sharing only depends on the droop gains, while in LVF the sharing is affected by cable resistances. However, GVF can only be implemented if a measurement of the common bus voltage V_b is dispatched to all the parallel modules, requiring a communication channel. The voltage-mode droop can only be implemented by measuring the local current injected by each parallel module. Current sharing in steady state can be derived as:

$$I_1 : I_2 : \cdots : I_n = \frac{1}{k_1 + R_1} : \frac{1}{k_2 + R_2} : \cdots : \frac{1}{k_n + R_n} \tag{4}$$

Equation (4) shows how the voltage-mode droop is affected by cable resistance. A comparison of the steady-state power sharing performance of the three methods is reported in Table I. The GVF approach can provide accurate current sharing among parallel

modules whilst the accuracy of the LVF approach is compromised by the cable resistance which changes with environmental conditions. The GVF approach can attenuate the effect of cable impedance and improve the power sharing accuracy compared to LVF as detailed discussed in [27], which neglects the measurement error found in practical systems.

TABLE I
PROPERTIES OF VOLTAGE MODE AND CURRENT MODE DROOP CONTROL METHODS

Droop control method	Accurate power sharing	Properties
Voltage-mode	No	Only dependent on local measurement
Current-mode (LVF)	No	Only dependent on local measurement
Current-mode (GVF)	Yes	Dependent on global voltage measurement and communication channel

B. Control Schemes and Small Signal Modelling

(1) Current-mode Droop Control Scheme

Fig. 7 shows the equivalent control block diagram for the current-mode droop control scheme. The output of the voltage droop controller is the DC current reference (i_{dc}^*) and the DC current is regulated by a PI controller G_{Idc}. Since the inner current loop is much faster than the outer loop, it can be simplified by a first-order lag G_{cc}(s).

$$G_{CC}(s)=\frac{1}{\tau s+1} \tag{5}$$

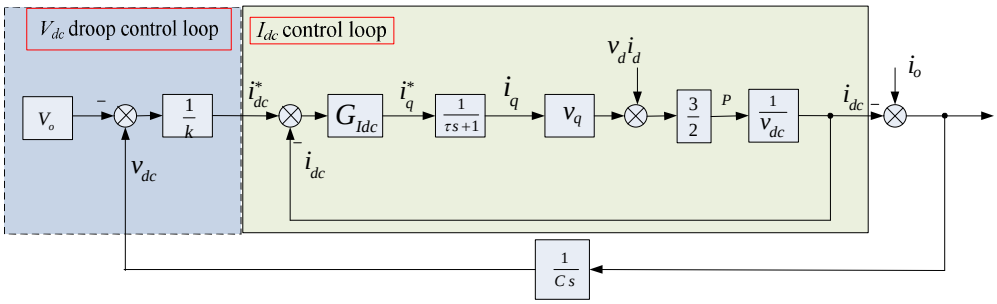


Fig. 7. Control block diagram for the current-mode droop-controlled system.

Using the amplitude invariant transformation, the active power can be expressed in the *dq* frame as:

$$P=\frac{3}{2}(v_d i_d+i_q v_q) \tag{6}$$

where v_d and v_q are the converter terminal voltages in the *dq* frame and i_d and i_q are the AC currents.

Using the classical vector control in the *dq* frame, the *d*-axis and *q*-axis stator voltages yield:

$$\begin{cases} v_d=(R_s+L_s s)i_d-\omega_e L_s i_q+e_d \\ v_q=(R_s+L_s s)i_q+\omega_e L_s i_d+e_q \end{cases} \tag{7}$$

where e_{dq} is the point of common coupling (PCC) bus voltage; R_s is the stator resistance; ω_e is the grid frequency in rad/s; L_S is the AC side inductance. In this paper, the q-axis is used to regulate the active power. Thus, e_d is controlled to be zero and e_q is the magnitude of the phase voltage vector.

According to (7), the linearized q-axis voltage, v_q, can be expressed as:

$$\triangle v_q = (R_s + L_s s)\triangle i_q + \omega_e L_s \triangle i_d \tag{8}$$

Assuming the reactive power component equals zero (i_d = 0), equation (6) can be linearized about an operating point (indicated with the subscript "o"):

$$\triangle P = \frac{3}{2}(\triangle v_q i_{qo} + \triangle i_q v_{qo}) \tag{9}$$

By substituting equation (8) into (9), the active power perturbation can be written as:

$$\triangle P = \frac{3}{2}[((R_s + L_s s)i_{qo} + v_{qo})\triangle i_q + \omega_e L_s i_{qo} \triangle i_d] \approx \frac{3}{2}(L_s i_{qo} s + R_s i_{qo} + v_{qo})\triangle i_q \tag{10}$$

Fig. 8 shows the linearized control block diagram for the current-mode droop-controlled system. The control-to-output (Δi_{dc} to Δi_q^*) G_{P_C} can be expressed as:

$$G_{P\_C} = \frac{\triangle i_{dc}}{\triangle i_q^*} = \frac{1.5(i_{qo} L_s s + R_s i_{qo} + v_{qo})}{V_{dco}(\tau s + 1)} \tag{11}$$

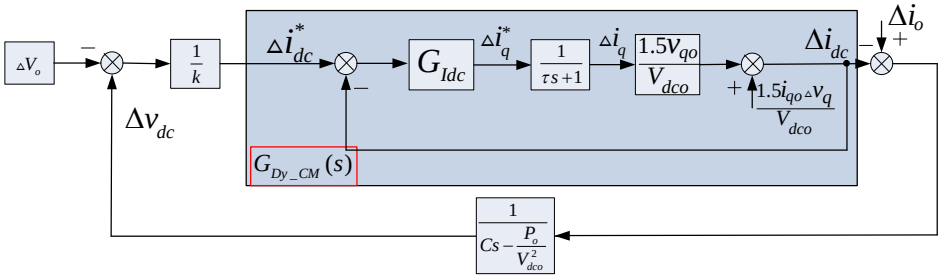


Fig. 8. Linearized control block diagram of the current-mode droop-controlled system.

The I_{dc} control dynamics can be mathematically expressed as in (12),

$$G_{Dy\_CM} = \frac{\triangle i_{dc}(s)}{\triangle i_{dc}^*(s)} = \frac{(k_{pdc} s + k_{idc})(L_s i_{qo} s + R_s i_{qo} + v_{qo})}{\frac{2}{3} v_{dco} s(\tau s + 1) + (k_{pdc} s + k_{idc})(L_s i_{qo} s + R_s i_{qo} + v_{qo})} \tag{12}$$

where k_{pdc} and k_{idc} are the PI control parameters for the I_{dc} controller G_{Idc}(s).

Due to the term ($L_s i_{qo}$s+$R_s i_{qo}$+v_{qo}) in the control-to-output transfer function (i_{qo} is negative and v_{qo} is positive at the operating point), a positive right half plane (RHP) zero exists in the I_{dc} control loop (G_{Dy_CM}) which can be expressed as:

$$z = -\frac{v_{qo} + R_s i_{qo}}{L_s i_{qo}} \tag{13}$$

This RHP zero will pose some challenges to system stability, as will be discussed in Section III.

Considering the DC bus voltage dynamics, the relationship between DC current and voltage perturbation can be written as:

$$C\frac{d\triangle v_{dc}}{dt}=\triangle i_o-\triangle i_{dc}=\triangle i_o-(\frac{\triangle P}{v_{dco}}-\frac{P_o}{v_{dco}^2}\triangle v_{dc})=-\frac{1}{v_{dco}}\triangle P+\frac{P_o}{v_{dco}^2}\triangle v_{dc}+\triangle i_o \tag{14}$$

In the Laplace domain, (14) can be rewritten as:

$$\triangle v_{dc}=\frac{1}{(Cs-\frac{P_o}{v_{dco}^2})}\triangle i_o-\frac{1}{(Cs-\frac{P_o}{v_{dco}^2})}\triangle i_{dc} \tag{15}$$

The overall closed loop transfer function of the V_{dc} droop control yields (16):

$$\frac{\triangle v_{dc}}{\triangle v_o}=\frac{G_{Dy\_CM}}{G_{Dy\_CM}+k(Cs-\frac{P_o}{V_{dco}^2})} \tag{16}$$

Substituting (12) into (16), the closed loop transfer function of V_{dc} loop for the current-mode droop-controlled system is expressed as follows:

$$\frac{\triangle v_{dc}}{\triangle v_o}=\frac{(k_{pIdc}s+k_{iIdc})(L_s i_{qo}s+R_s i_{qo}+v_{qo})}{(k_{pdc}s+k_{idc})(L_s i_{qo}s+R_s i_{qo}+v_{qo})+k(Cs+\frac{P_o}{V_{dco}^2})\frac{2}{3}V_{dco}(s(\tau s+1)+(k_{pIdc}s+k_{iIdc})(L_s i_{qo}s+R_s i_{qo}+v_{qo}))} \tag{17}$$

It can be inferred from (17) that the droop gain will not only affect the steady-state voltage deviation but also influence the voltage loop bandwidth.

(2) Voltage-mode Droop Control Scheme

Fig. 9 shows the control block diagram for the voltage-mode droop-controlled system. Linearizing the system around the equilibrium point, as shown in Fig. 10, the control-to-output (Δv_{dc} to Δi_q^*) transfer function G_{p_V}(s) yields:

$$G_{P\_V}(s)=\frac{\triangle v_{dc}}{\triangle i_q^*}=\frac{1.5(i_{qo}L_s s+R_s i_{qo}+v_{qo})}{V_{dco}(\tau s+1)(Cs-\frac{P_o}{V_{dco}^2})} \tag{18}$$

It can be observed that a faster bandwidth within the V_{dc} control will challenge stability due to the RHP zero in (18). In comparison with the current-mode droop control diagram, a small droop gain *k* applied to the voltage-mode droop does not impose limitations to stability, as *k* appears as a feedforward term in the block diagram.

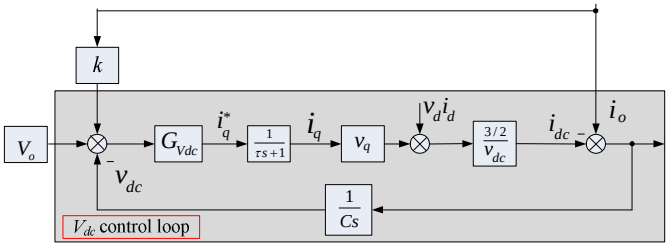


Fig. 9. Control block diagram for the voltage-mode droop-controlled system.

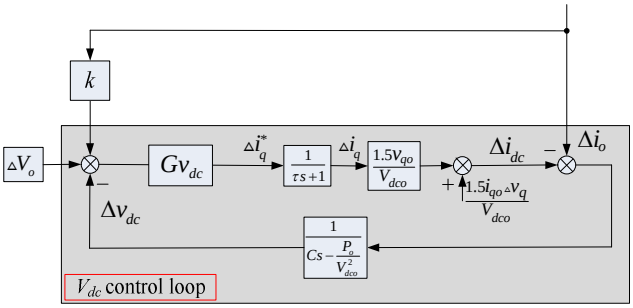


Fig. 10. Linearized control block diagram for the voltage-mode system.

Hence, the voltage control dynamics can be expressed as:

$$G_{Dy\_VM}=\frac{\Delta v_{dc}}{\Delta v_o}=\frac{G_{Vdc}G_{P\_V}}{1+G_{Vdc}G_{P\_V}}=\frac{1.5(i_{qo}L_s s+R_s i_{qo}+v_{qo})(k_{pVdc}s+k_{iVdc})}{s(\tau s+1)(V_{dco}Cs-\frac{P_o}{V_{dco}})+1.5(i_{qo}L_s s+R_s i_{qo}+v_{qo})(k_{pVdc}s+k_{iVdc})} \tag{19}$$

where k_{pVdc} and k_{iVdc} are the proportional gain and integral gain of the V_{dc} controller G_{Vdc}, respectively. If the load disturbance is neglected, it is inferred that the voltage dynamics are mainly determined by the controller bandwidth rather than the droop gain.

III. Stability Analysis of Single Source Operation

Before considering the parallel configuration, the impedance and stability properties of the two droop techniques will be investigated within a single source scenario. The system can be represented in a cascaded way: source converter subsystem and load converter subsystem. Assuming that the source converter and load converter are individually stable, when the output impedance of the source converter Z_S is less than the input impedance of the load converter Z_L over the entire frequency range, the stability of the cascaded system can be guaranteed based on the Middlebrook's criterion [39]. However, it has been shown that the previously proposed understanding of the minor loop gain (impedance ratio Z_S/Z_L) is sometimes incorrect [40], [41]. If the source converter is controlled as a voltage source, the impedance ratio should be Z_S/Z_L but if the source converter is controlled as a current source, the impedance ratio should be Z_L/Z_S. In general, the impedance on the numerator has to be the internal impedance of the subsystem containing the voltage source or sink, and the impedance on the denominator has to be the internal impedance of the subsystem containing the current source or sink [42], [43]. In addition, the voltage-source or current-source should also be an independent source and should not be related to other variables (controlled source). For the current-mode droop-controlled system as shown in Fig. 4, the DC current reference is still dependent on the voltage and the control target is to regulate the DC terminal voltage in proportion to the load (see Fig. 7). Hence, the minor loop gain for the current-mode approach should still be Z_S/Z_L when using the impedance-based approach [44], [45].

A. Impedance Analysis

The equivalent circuits for the current-mode and voltage-mode droop-controlled systems, including the droop equations and the local control dynamics, are shown in Fig. 11 and Fig. 12 respectively. The parasitic capacitance of the cable is much smaller than bus capacitor (C_b) and local capacitor (C_i), and it can be included in the converter DC side capacitances. Thus, the cabling is represented by series *R-L* branches (R_1, L_1). As discussed in [46] and [47], a linearized CPL can be approximately expressed by a negative impedance ($-R_{CPL}$) in parallel with a current source (I_{CPL}).

$$Z_L = -R_{CPL} = -\frac{V_b^2}{P_{CPL}}, \quad I_{CPL} = 2\frac{P_{CPL}}{V_b} \tag{20}$$

where P_{CPL} is the absorbing power of the CPL and Z_L is the input impedance of the CPL.

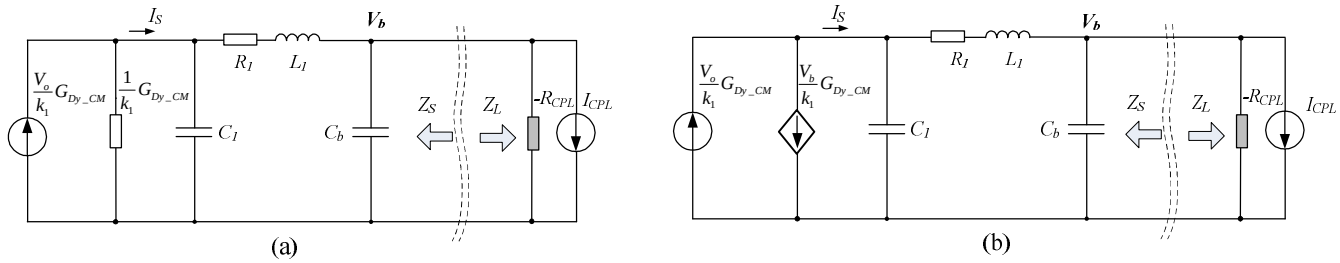


Fig. 11. Equivalent impedance circuit for the current-mode droop approaches. (a) LVF. (b) GVF.

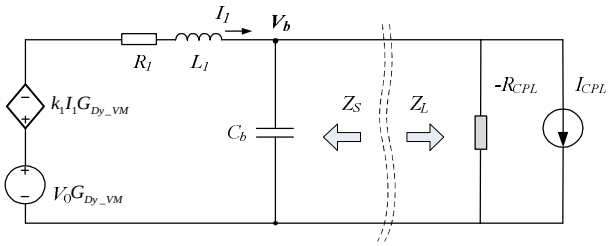


Fig. 12. Equivalent impedance circuit for the voltage-mode droop approach.

According to the equivalent linearized circuits shown in Fig. 11 and 12, the source impedances for different droop approaches can be derived as:

$$\begin{cases} Z_{s\_LVF}(s) = \dfrac{k_1(L_1C_1s^2 + R_1C_1s + 1) + G_{Dy\_CM}(L_1s + R_1)}{k_1s(L_1C_1C_bs^2 + R_1C_1C_bs + C_1 + C_b) + G_{Dy\_CM}(L_1C_bs^2 + R_1C_bs + 1)} \\ Z_{s\_GVF}(s) = \dfrac{k_1(L_1C_1s^2 + R_1C_1s + 1)}{k_1s(L_1C_1C_bs^2 + R_1C_1C_bs + C_1 + C_b) + G_{Dy\_CM}} \\ Z_{s\_VM}(s) = \dfrac{(L_1s + R_1) + k_1G_{Dy\_VM}}{(L_1C_bs^2 + R_1C_bs + 1) + C_bk_1sG_{Dy\_VM}} \end{cases} \tag{21}$$

G_{Dy_CM} and G_{Dy_VM} are the DC current and DC voltage control dynamics for the current-mode (see (12)) and voltage-mode (see (19)), droop-controlled systems respectively.

Using the parameter values listed in Table II, the Bode diagrams of the LVF and GVF source impedances, as shown in Fig. 13, indicate that the stability characteristics for LVF and GVF are quite similar. In comparison to the GVF approach, LVF is not

an accurate solution for power sharing performance. However, its control scheme can be implemented using only local measurements. For the GVF approach, the main bus voltage needs to be measured, i.e. an extra voltage sensor and additional communication links between the common bus and the individual parallel modules would be required within a large DC MG. This would compromise the modular, decentralized feature of droop control. Hence, the LVF method is selected as a representative of the current-mode droop control approach within this paper. A comparative stability analysis using the current-mode and voltage-mode approach will be presented in the following subsection.

TABLE II
SYSTEM PARAMETERS

Category	Parameter	Symbol	Value
Cable	Cable resistance	R_i	3 mΩ
	Cable inductance	L_i	5 μH
Droop characteristic	Nominal voltage	V_o	270 V
	Droop gain	k_1	1
Capacitor	Local capacitance	C_1	1.2 mF
	Bus capacitance	C_b	0.8 mF

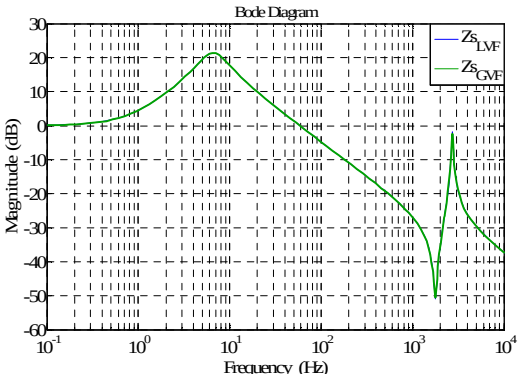


Fig. 13. Source impedance for the current-mode droop control under LVF and GVF approach adopting the same control parameters.

B. Effect of Local Control Bandwidth

In the current-mode droop-controlled system there are three control loops, i.e. voltage droop control, I_{dc} control loop and inner current loop. If the second loop, the I_{dc} control loop, is simplified to be a first-order system with bandwidth ω_{Idc}, the voltage loop can be rewritten as:

$$\frac{\triangle v_{dc}}{\triangle v_o} = \frac{\omega_{Idc}}{k_1 C_1 V_{dco}(s^2 + (\omega_{Idc} - \frac{P_o}{C_1 V_{dco}^2})s + \frac{\omega_{Idc}}{C_1}(\frac{1}{k_1 V_{dco}} - \frac{P_o}{V_{dco}^2}))} \tag{22}$$

It can be inferred from (22) that decreasing the droop gain, k_1, increases the voltage-loop bandwidth for the *current-mode* droop-controlled system. Using the Routh-Herwitz stability criterion, in order to ensure stability the simplified DC current loop bandwidth ω_{Idc} should satisfy:

$$\omega_{Idc} > \frac{P_o}{C_1 V_{dco}^2} \tag{23}$$

Fig. 14 shows the source impedance of the current-mode system with different I_{dc} control bandwidth. A tightly regulated 3 kW buck converter can be utilized as an example of a CPL **Error! Reference source not found.**, the input impedance of the buck converter (load impedance Z_L) is also shown to see the interaction between the source and load subsystem. Slow I_{dc} control dynamics (5 Hz bandwidth) will challenge the stability since the magnitude of source impedance hits the load impedance at

around 3 Hz while the phase discrepancy between source and load impedance exceeds 180°. Increasing the I_{dc} control bandwidth can attenuate the peak magnitude of the source impedance and consequently enlarge the stability margin. However, it should be noted that the RHP zero shown in (12) could impose severe stability limitations, including high gain instability and restricted closed-loop bandwidth [51]. It can be seen that the RHP zero migrates closer to the origin and results in strict limitations on the feasible bandwidth of the DC current loop. According to [51], the feasible bandwidth should be limited to approximately:

$$\omega_{Idc} < \frac{z}{2} = \frac{-(v_{qo} + R_s i_{qo})}{2L_s i_{qo}} \tag{24}$$

Normally, the DC current loop bandwidth cannot exceed the upper limit due to the cascaded control structure.

The voltage-mode droop-controlled system consists of two loops: the V_{dc} control loop and the inner current loop, as shown in Fig. 9. Droop control is implemented as a feedforward link. It can be seen in Fig. 15 that with a 5 Hz V_{dc} control bandwidth the source impedance magnitude hits the load impedance and the phase discrepancy is larger than 180º, indicating that the system is unstable. With a higher control bandwidth (10 Hz or 20 Hz), the magnitude of the source impedance is always lower than the load impedance. Therefore, it shows that the system stability is guaranteed when the V_{dc} control bandwidth is increased to 10 Hz or 20 Hz. Alternatively, as can be seen from (18), the RHP zero in the plant implies that the stability margin will reduce with increased gain in the V_{dc} controller.

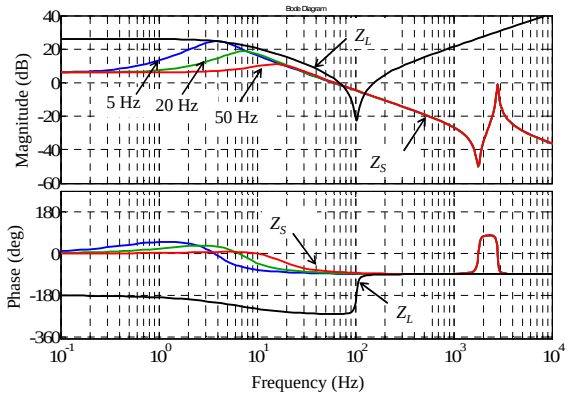


Fig. 14. Bode diagram for the current-mode droop-controlled system with different I_{dc} control bandwidth.

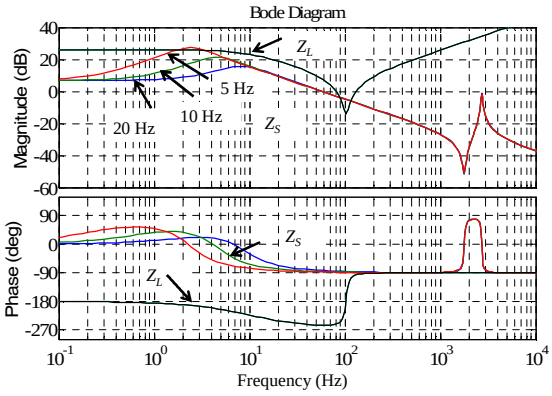


Fig. 15. Bode diagram for the voltage-mode droop-controlled system with different V_{dc} control bandwidth.

C. *Effect of Droop Coefficient*

(1) Equilibrium point-Upper limit

It is known that a larger droop coefficient will cause more voltage deviation [52] and therefore the system needs to be designed carefully in order to ensure the equilibrium point is achievable according to the load power. As shown in Fig. 16, the V-I characteristic can be expressed as:

$$V_b = V_o - (k_i + R_i) I_o \tag{25}$$

For the load side, a CPL creates a hyperbolic line which can be expressed as:

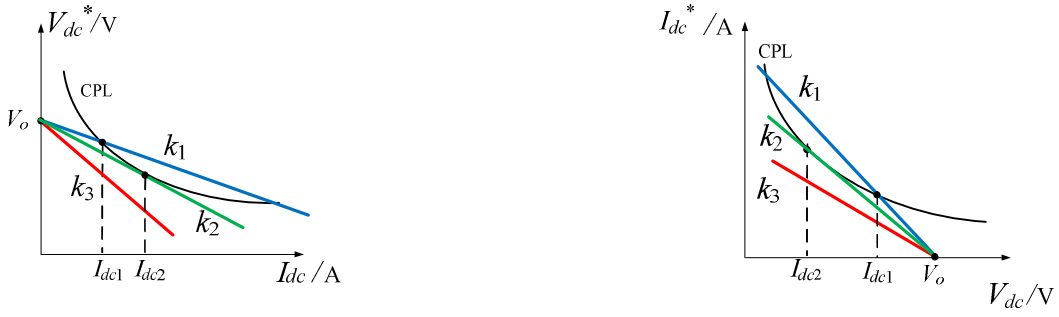
$$P_{CPL} = V_b I_o \tag{26}$$

where P_{CPL} is the power of the CPL and I_o is the load current. The cascaded system can operate normally only if the two curves have an intersection point (equilibrium point). The stable equilibrium point can be derived as follows:

$$V_b = \frac{1}{2}(V_o + \sqrt{V_o^2 - 4(k_i + R_i)P_{CPL}}), \quad I_o = \frac{1}{2k_i}(V_o - \sqrt{V_o^2 - 4(k_i + R_i)P_{CPL}}) \tag{27}$$

Fig. 16(a) shows that a larger droop constant will cause bigger bus voltage deviation and can even result in there being no intersection point between the source curve and CPL curve (for example the k_3 curve). As a consequence, no steady-state solution can be found, leading to instability. Using (27), the maximum droop gain can be derived as:

$$k_i < \frac{V_o^2}{4P_{CPL}} - R_i \tag{28}$$



(a) (b)

Fig. 16. Interaction between the droop-controlled source system and CPL. (a) *Voltage-mode*. (b) *Current-mode*.

(2) Source and Load impedance interaction-Upper limit

The droop coefficient will also influence the source and load impedance and consequently affect the system stability. For the current-mode droop approach, the Bode diagram of the impact of droop coefficient variation on the source/load impedance is shown in Fig. 17. With an increase in the droop coefficient, it can be seen that the source impedance magnitude increases (especially at low frequencies). The DC bus voltage will reduce and as a result, the magnitude of the load impedance will decrease according to (20) (see Fig. 17(b)). Overall, the system stability margin shrinks with increased droop gain.

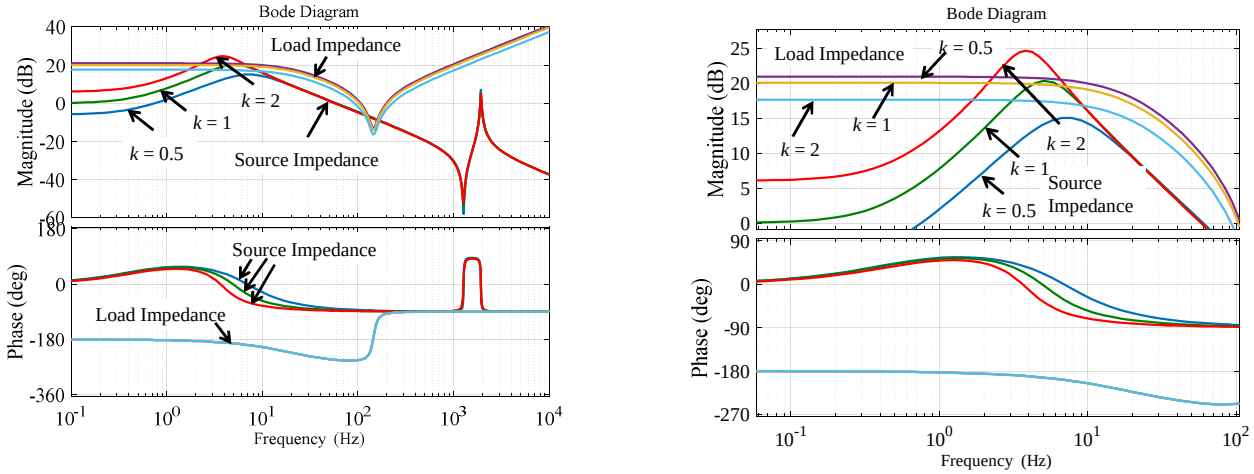


Fig. 17. Bode diagram of source/load impedances with different values of droop gain using the current-mode droop control approach (6kW CPL). (a) Overview. (b) Zoomed part of the load impedances.

The Bode plot of the source and load impedance in the voltage-mode droop-controlled system is shown in Fig. 18. Similarly to the current-mode droop-controlled system, the source impedance magnitude in the low frequency range also increases with an increase in the droop gain whilst the load impedance magnitude decreases. Therefore, the stability of the voltage-mode droop-controlled system is also degraded with an increased value of the droop coefficient. However it is worth noting that in contrast with the current-mode approach, the frequency peak within the voltage-mode approach is quite similar under different droop gains and the peak can be attenuated by increasing the voltage loop bandwidth (see Fig. 15).

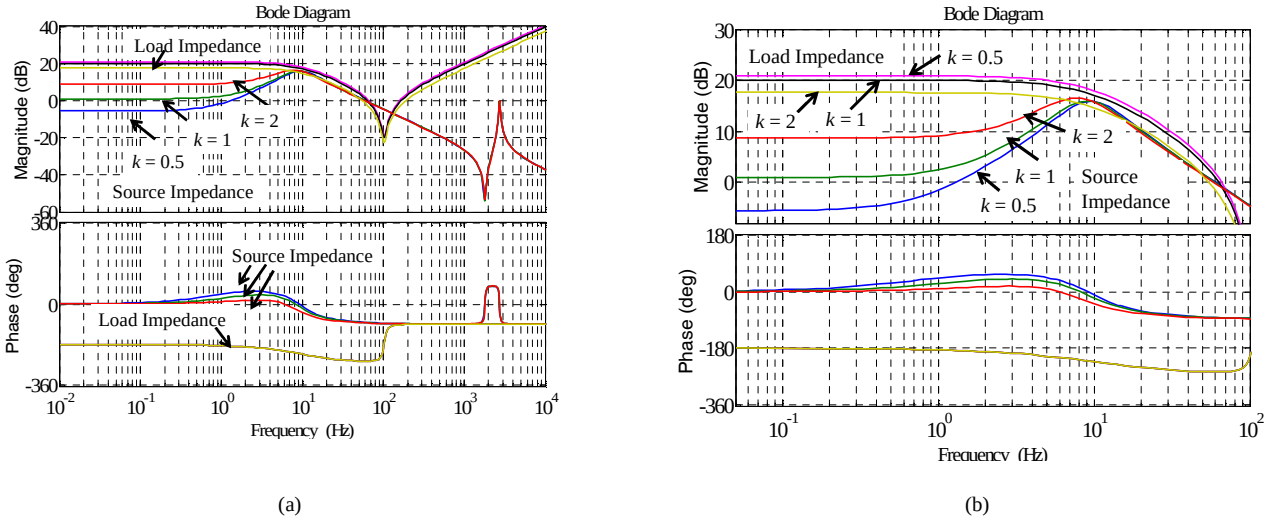


Fig. 18. Bode diagram of source/load impedances with different values of droop gain using the voltage-mode droop control approach (6kW CPL). (a) Overview. (b) Zoomed part of the load impedances.

In summary, the upper boundary of the droop gain is limited by two factors; available equilibrium point and source/load

impedance interaction. In other words, the upper threshold value of the droop gain has to be set in order to ensure the steady-state operating point is achievable, according to the specific system loads, and in order to avoid interaction of the source/load impedance.

(3) Non-minimum phase property-Lower limit

For the *current-mode* droop approach, decreasing the droop gain k reduces the steady-state DC voltage error and increases the voltage-loop bandwidth. However, this also reduces the damping and robustness of the system, leading to a lower boundary for the droop gain. This effect can be explained from the standpoint of control design. Droop control is effectively a proportional controller. As shown in Fig. 8, the inverse of the droop gain can be regarded as the proportional gain of the DC voltage controller. Following the discussion in Section II-B, due to the presence of the RHP zero in G_{Dy_CM}, a high proportional gain (inverse of droop gain $1/k$) will push the non-minimum phase system to instability. This instability is because some of the system eigenvalues will be in the RHP if the inverse of droop gain ($1/k$) increases over a threshold value. Fig. 19 shows the root contour with respect to the proportional gain ($1/k$), demonstrating that the system is unstable when the inverse of droop gain $1/k$ is higher than 40 (k is lower than 1/40).

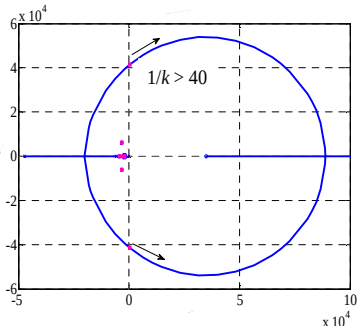


Fig. 19. Root locus with respect to the inverse of the droop coefficient using the current-mode approach.

A distinct characteristic of the voltage-mode droop approach is that the droop gain lies in a feedforward term, as discussed in Section II-B. Hence, a small droop gain k does not deteriorate the system stability. This is a significant advantage of *voltage-mode* droop over *current-mode* droop.

D. Comparison of Stability Boundary

A comparison of the control properties of current-mode and voltage-mode droop control is listed in Table III. Comparing the control schemes in Figs. 7 and 9, three control loops exist in current-mode system whilst only two cascaded loops exist in the voltage-mode system. The local control bandwidth (I_{dc} control bandwidth for current-mode system / V_{dc} bandwidth for voltage-mode system) are limited by the non-minimum phase property (upper boundary) and source/load impedance interaction (lower boundary).

TABLE III

COMPARISON OF THE CONTROL PROPERTIES UNDER CURRENT/VOLTAGE MODE DROOP CONTROL

Control bandwidth / Droop mode	Upper Limit	Lower Limit	Control loops
Current-mode	Non-minimum phase property (Eq. (24))	Source/load impedance interaction (Eq. (23))	DC voltage control + DC current control + Inner current control
Voltage-mode	Non-minimum phase property	Source/load impedance interaction	DC voltage control + Inner current control

The limitations on stability imposed by the droop gain are summarized in Table IV. For current-mode droop control, the RHP zero in G_{Dy_CM} imposes a tighter lower limit for the droop gain and restricts the system stability. In contrast, voltage-mode droop control can operate with a wider range of droop gain, even with zero droop gain, i.e. constant voltage control. However, for both droop approaches a larger droop gain will reduce the stability margin, introduce more voltage deviation and even cause non-operability of the system due to the absence of a steady-state operating point. Furthermore, in the current-mode droop-controlled system, the droop gain will influence the DC voltage control dynamics, however, in the voltage-mode droop-controlled system the DC voltage dynamics are not affected by the droop gain (see Section II-B).

TABLE IV

COMPARISON OF UPPER AND LOWER LIMIT FOR THE DROOP GAIN UNDER CURRENT/VOLTAGE MODE DROOP CONTROL

Droop gain / Droop mode	Upper Limit	Lower Limit	Control block diagram	Influence on DC voltage dynamics
Current-mode	Equilibrium point + Source/load impedance interaction	Non-minimum phase property	Proportional controller in forward channel	Yes
Voltage-mode	Equilibrium point + Source/load impedance interaction	Not less than 0	Feedforward term	No

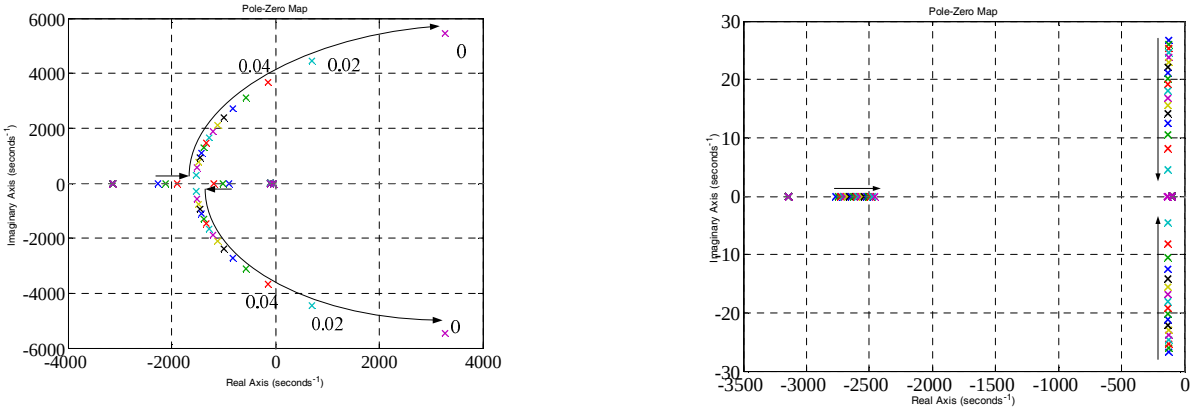
The state-space models of VSCs under *current-mode* and *voltage-mode* droop control are developed as follows:

$$\begin{cases} \dot{\Delta x}_c = A_c \Delta x_c \quad (x_c = \left[v_{dc}, i_d, i_q, X_{id}, X_{iq}, X_{Idci} \right]^T) \\ \dot{\Delta x}_v = A_v \Delta x_v \quad (x_v = \left[v_{dc}, i_d, i_q, X_{id}, X_{iq}, X_{Vdci} \right]^T) \end{cases} \tag{29}$$

where x_c and A_c are the state and matrix of *current-mode* droop-controlled system; x_v and A_v are the state and matrix of the voltage-mode droop-controlled system. $X_{id}, X_{iq}, X_{Idci}, X_{Vdci}$ are the states associated with the PI controllers for the *dq*-axes current controllers, DC current and DC voltage, respectively. The explicit form of the state matrices can be found in the Appendix.

Based on these models, a comparison of eigenvalue contours of the current/voltage-mode droop-controlled systems is shown

in Fig. 20. It can be seen in Fig. 20(a) that some eigenvalues move towards the right half plane (RHP) with decreasing droop gain. In this case the current-mode system is unstable if the droop gain is smaller than 0.03. In contrast, it is shown in Fig. 20(b) that the voltage-mode droop-controlled system is stable even with zero droop gain.



(a) (b)

Fig. 20. Eigenvalue contours with respect to droop gain variation from 0.2 to 0 at each step of -0.02 in (a) current-mode droop-controlled system, (b) voltage-mode droop-controlled system.

The current-mode droop-controlled system will evolve to constant current control if the droop gain k approaches infinity. Alternatively, under the zero droop gain, the voltage-mode droop control effectively becomes constant voltage control. Thus, the developed state-space model can be also applied to the constant current/voltage controlled system.

Depending on the practical application, the required droop method can be chosen appropriately. If constant nominal voltage control is not required, and the main control objective of the VSCs is to inject/absorb current/power, then current-mode droop control is preferred. In this case, the DC voltage will reduce according to the load and the reduction rate will be related to the droop slope. Nevertheless, the nominal voltage (270 V in this study) can not be obtained when the system is loaded since the current-mode droop control approach is not feasible under zero droop gain. In contrast, if DC voltage needs to be tightly regulated, and the nominal voltage is required in full load conditions, then voltage-mode droop control is recommended.

IV. Generalized Multi-Source Multi-Load System

In practical applications, a DC MG is composed of multiple sources and multiple loads, an example of this is shown in Fig. 2. This section will extend the impedance analysis presented in Section III to the general case of multiple sources feeding a common bus with multiple loads. Stability assessment of parallel source operation, including the impact of the power sharing ratio and the number of parallel modules, has been performed.

A. DC Bus V-I Characteristic

Similar to the individual droop line in each parallel module, the V-I characteristic at the DC bus can be expressed as a function of a global equivalent droop gain:

$$V_b = V_o - I_1(k_1 + R_1) = V_o - I_2(k_2 + R_2) = \ldots = V_o - I_n(k_n + R_n) \tag{30}$$

where I_1, I_2, … I_n; k_1, k_2, … k_n are the branch currents and droop gains for the parallel modules. V_o represents the nominal voltage (270V in this study) and V_b is the bus voltage. Thus, the total load current can be expressed as:

$$I_{Lt} = I_1 + I_2 + \ldots + I_n = (V_o - V_b)\sum_{i=1}^{n} \frac{1}{k_i + R_i} \tag{31}$$

which can be reformatted as follows:

$$V_b = V_o - I_{Lt} \frac{1}{\sum_{i=1}^{n} \frac{1}{k_i + R_i}} \tag{32}$$

The global droop gain k_t, which defines the slope of DC bus V-I characteristic, can be expressed as:

$$k_t = \frac{1}{\sum_{i=1}^{n} \frac{1}{k_i + R_i}}, \quad k_t = \frac{1}{\sum_{i=1}^{n} \frac{1}{k_i}} \tag{33}$$

where R_i is the i^{th} branch cable resistance and the droop coefficient is assumed to be much larger than the cable resistance ($k_i >> R_i$). As shown in Fig. 21, the relationship between global droop gain k_t and individual droop gain k_i shows that the global droop curve is stiffer than the individual droop characteristic. This indicates that, under the same load condition, the bus voltage deviation is smaller if more sources with identical droop gain are connected. It can be seen from (32) that the DC bus voltage, V_b, is determined by the global droop gain k_t and total load current I_{Lt}. Even if the individual values of droop gains are different, the bus voltage will be identical as long as the individual droop gains yield the same global droop coefficient, k_t, in (33). As a result, individual droop gains can be selected based on their desired ratio as:

$$k_i = \frac{k_t}{n_i} \quad \left\{ \sum_{i=1}^{N} n_i = 1 \right\} \tag{34}$$

where n_i represents the current sharing percentage of i^{th} module.

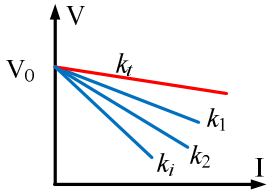


Fig. 21. Relationship between the global droop gain and individual droop gain.

B. Source/Load Impedance

Extending the derivation of Section III to a multiple source system, the overall source impedance can be derived as:

$$\begin{cases} Z_{st\_LVF}=\dfrac{1}{\sum_{i=1}^{n}\dfrac{Y_{ib}(C_i s+\dfrac{G_{Dy\_CMi}}{k_i})}{(Y_{ib}+\dfrac{G_{Dy\_CMi}}{k_i}+C_i s)}+C_b s}, \quad Z_{st\_GVF}=\dfrac{1}{-\sum_{i=1}^{n}\dfrac{Y_{ib}(Y_{ib}-\dfrac{G_{Dy\_CMi}}{k_i})}{(Y_{ib}+C_i s)}+C_b s+\sum_{i=1}^{n}Y_{ib}} & \text{(Current-mode)} \\ Z_{st\_VM}=\dfrac{1}{\sum_{i=1}^{n}\dfrac{1}{(\dfrac{1}{Y_{ib}}+k_i G_{Dyi\_VMi})}+C_b s} & \text{(Voltage-mode)} \end{cases} \tag{35}$$

In DC MGs, there can be a lot of power electronic interfaced loads with CPL behavior, as shown in Fig. 22(a). From the viewpoint of impedance analysis, the parallel CPLs can be modelled as shown in Fig. 22(b) in a small signal manner and the total input load admittance of the cumulative CPL can then be equivalently represented as shown in Fig. 22(c). Therefore, the input impedance of CPL (Z_{CPL}) can be expressed as:

$$Z_{CPLt}=1/Y_{CPLt}=1/\sum_{i=1}^{n}Y_{CPLi}=1/[-(\frac{P_{CPL1}}{V_b^2}+\frac{P_{CPL2}}{V_b^2}+\cdots+\frac{P_{CPLm}}{V_b^2})]=-\frac{V_b^2}{\sum_{i=1}^{m}P_{CPLi}} \tag{36}$$

where P_{CPLi} is the power of i^{th} CPL. Hence, similar to the model of a single CPL in (20), total overall cumulative CPLs can still be represented as a negative impedance ($-R_{CPLt}$) in parallel with a current source (I_{CPLt}):

$$-R_{CPLt}=-\frac{V_b^2}{\sum_{i=1}^{m}P_{CPLi}}, \quad I_{CPLt}=2\frac{\sum_{i=1}^{m}P_{CPLi}}{V_b} \tag{37}$$

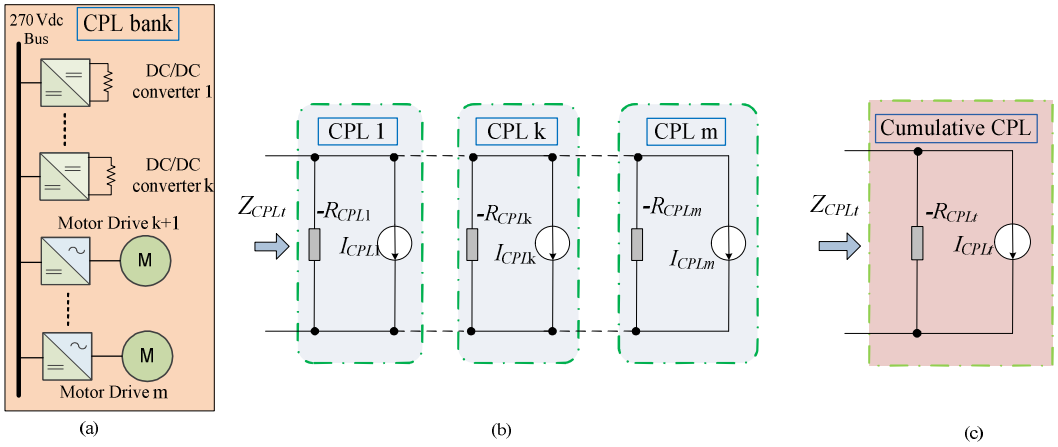


Fig. 22. Multiple CPL modelling. (a) Topology of single bus feeding multiple CPLs. (b) Small signal model of parallel CPLs. (c) Impedance model of cumulative CPL.

C. Sensitivity Analysis

The Nyquist stability criterion has been widely accepted for stability analysis [14]. Fig. 23 shows the Nyquist plots of the minor loop gain for the current-mode droop-controlled system under a 6 kW CPL. Since each individual droop gain is set to 1, the global droop gain k_t decreases with an increasing number of parallel sources. As a consequence, the voltage across the main bus increases and the magnitude of the load impedance is reduced (helpful for improving stability). It can also be seen from Fig. 23(a) that the Nyquist diagram of the single source system encircles the critical point (-1, j0) and the Nyquist contour dramatically moves further towards the RHP with an increasing number of parallel sources, which indicates that a higher stability margin is achieved by increasing the number of parallel modules.

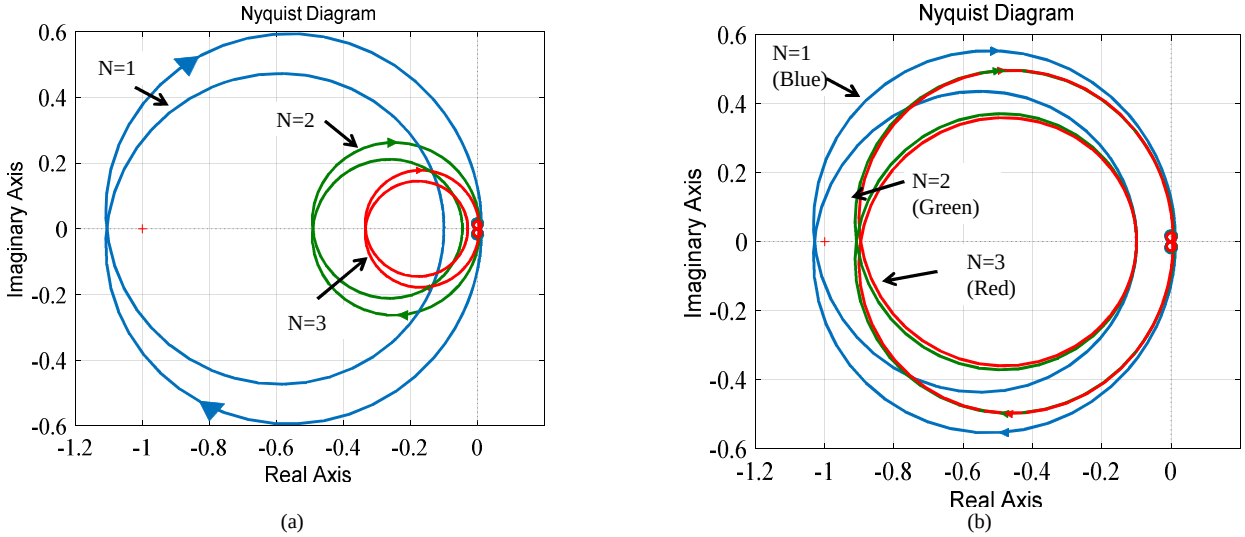
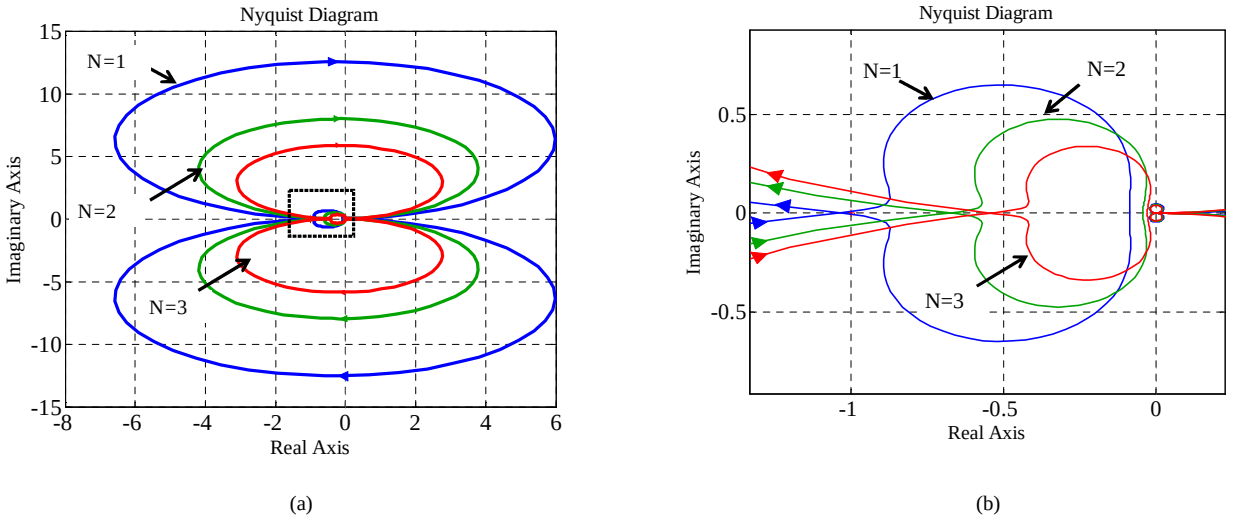


Fig. 23. Nyquist contours for the current-mode droop-controlled systems (a) $k_i = 1$. (b) $k_t = 1$.

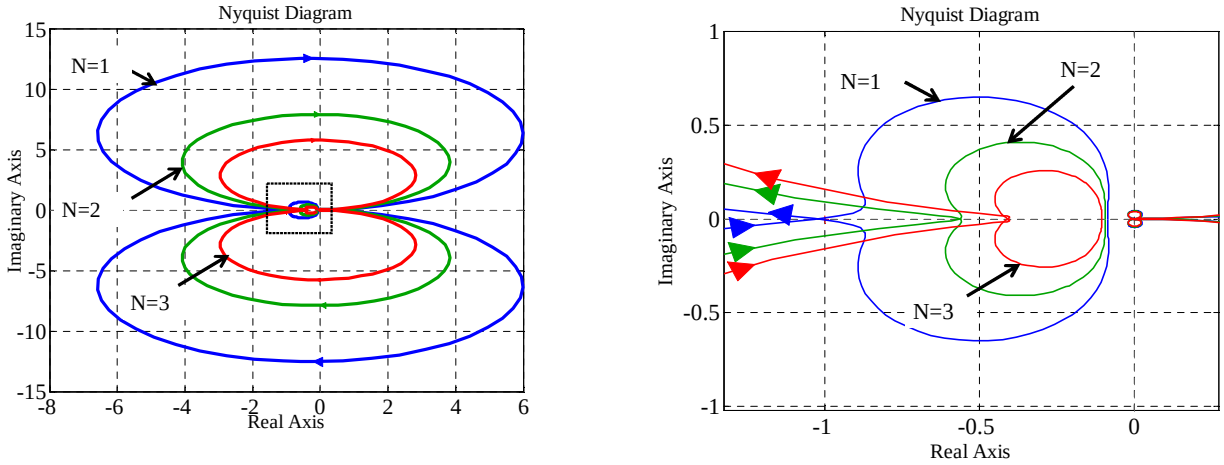
Fig. 23(b) shows the Nyquist plots of the minor loop gain for various current-mode droop-controlled systems with identical global droop gain. It can be observed that the Nyquist contour moves towards right with increasing the number of parallel sources, which reveals that system stability could be still improved.

For a 6 kW CPL, the Nyquist diagrams of the minor loop gain for a voltage-mode droop-controlled system are shown in Fig. 24. An overview of the Nyquist contours is shown in Fig. 24(a) and it can be clearly seen from the zoomed version in Fig. 24(b) that the Nyquist contour of the single source system encircles the (-1, j0) whilst the systems with more parallel sources do not encircle the critical point. This indicates that the stability is improved by increasing the number of modules with the same individual droop gain. In addition, Fig. 25(b) shows that under parallel operation, with the same global droop gain, the system shows a larger stability margin.



(a) (b)

Fig. 24. Nyquist contours for the voltage-mode droop-controlled system with individual droop gain k_i = 1. (a) Overview. (b) Zoomed part around (-1, j0).



(a) (b)

Fig. 25. Nyquist contours for the voltage-mode droop-controlled system with global droop gain k_t = 1. (a) Overview. (b) Zoomed part around (-1, j0).

To summarize, the global droop gain is an important factor when evaluating the stability of a multiple source system which feeds a single bus. With an increased number of parallel modules the global droop gain reduces, and as a consequence, the stability margin is improved for both current-mode and voltage-mode droop controllers. For both modes, paralleling sources while maintaining identical global droop gain shows a higher stability margin than the single source system.

V. Experimental Verification

The schematic of the experimental system is shown in Fig. 26. A test rig was used to validate the analytical findings based on three active front-end converters (SEMIKRON's IGBTS Power Stack-SEMIKUBE: SKM400GB12E4) with a programmable AC source (CHROMA QuadTech 31120) providing the AC inputs. The system was isolated by three step-down transformers to avoid circulating currents between parallel modules. Control algorithms and signal conditioning are implemented in custom

DSP/FPGA boards. The load is represented by a buck converter which is tightly controlled as a CPL, as illustrated in Fig. 27. The experimental setup is shown in Fig. 28 and the parameters of the experimental system are listed in Table V.

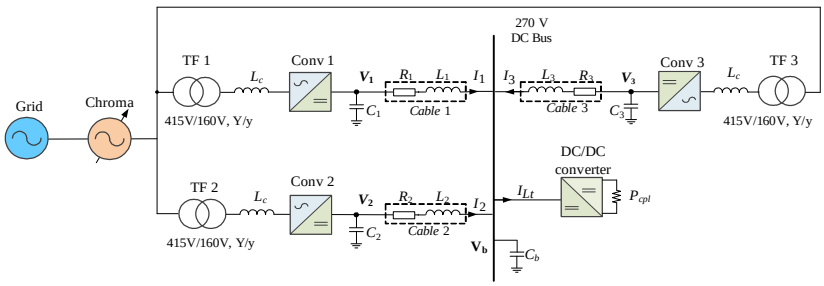


Fig. 26. Schematic of experimental system.

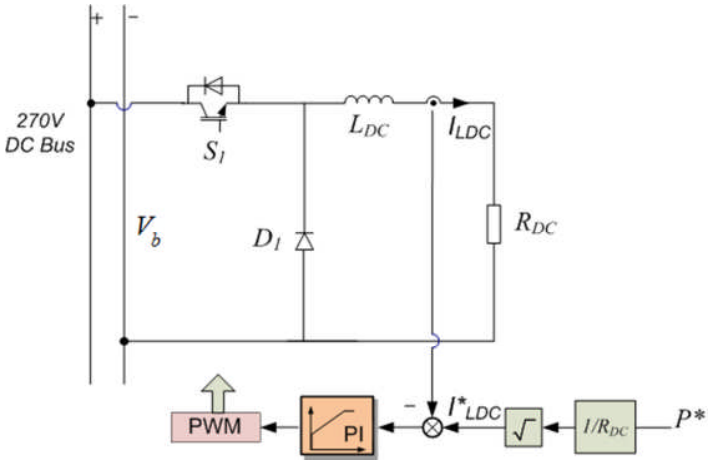


Fig. 27. Control scheme for the DC/DC converter as a CPL.

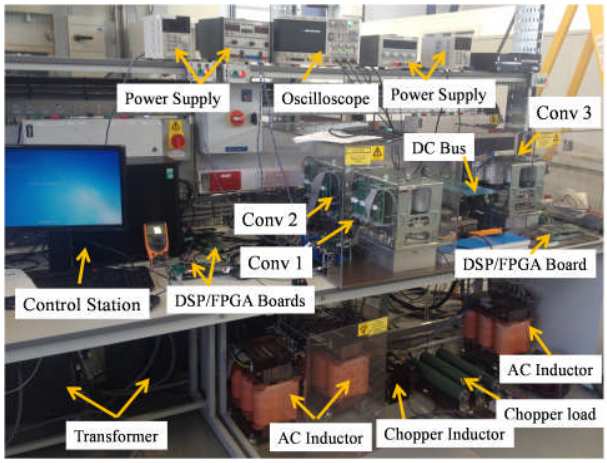


Fig. 28. Experimental setup.

TABLE V

EXPERIMENTAL SYSTEM PARAMETERS

Category	Parameter	Value
Three phase grid	Grid source voltage	415 V line-to-line RMS
Transformer TF 1, 2, 3	Transformation ratio	415 V/160 V, Y/y
	Rated capacity	20 kVA
AC Side Inductor	AC side inductance L_c	1.2 mH
	Parasitic resistance	0.1 Ω
DC/DC Converter	Load R_{DC}	9.2 Ω
	Inductance L_{DC}	1.3 mH
VSC (Conv 1, 2, 3)	Switching frequency	10 kHz
	Local capacitance C_i	1.2 mF
DC Link	DC link capacitance C_b	0.8 mF
	Nominal bus voltage V_o	270 V
Cable	Cable resistance R_i	0.02 Ω
	Cable inductance L_i	2 μH

A. Current-mode Droop Control – Single Source

In this subsection, current-mode droop control is employed and the effect of both the local DC current control bandwidth and the droop gain are validated experimentally. First, the current-mode droop control (Fig. 4) is tested with a single converter feeding the CPL and the droop gain k_1 is set to 2. The bus voltage and current behavior while increasing the power of the CPL are shown in Fig. 29. Fig. 29(a) shows the system response to increasing the power of the CPL with a 5 Hz local I_{dc} control bandwidth. This demonstrates the system is stable until a 3 Hz oscillation appears at 3 kW, confirming the analysis in Fig. 14. This experimentally verifies that high power CPLs deteriorate the system stability and demonstrates the impact of the low frequency resonance peak under low bandwidth control. Fig. 29(b) shows that the system can be stabilized by increasing the control bandwidth (in this case to 50 Hz) while also improving the dynamic response.

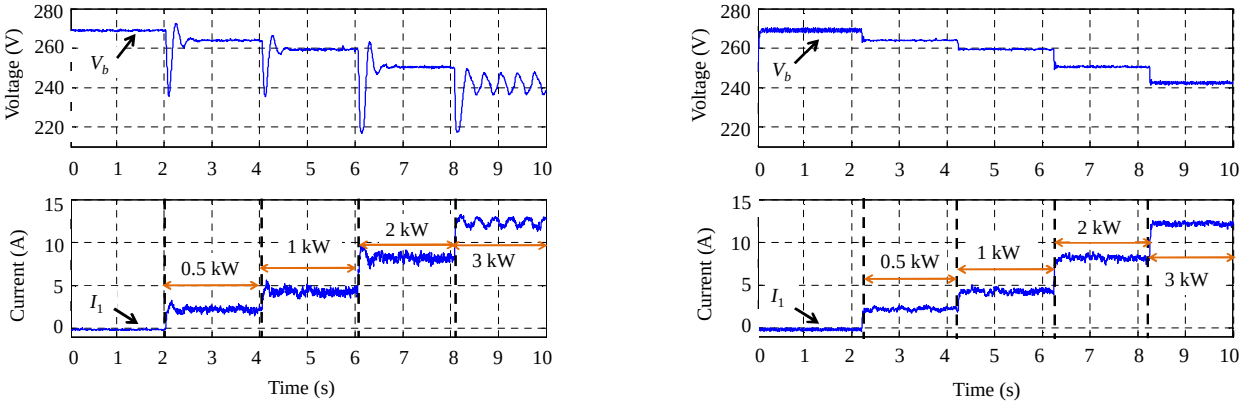


Fig. 29. Experimental results with different local control bandwidth. (a) 10 Hz control bandwidth. (b) 50 Hz control bandwidth.

Fig. 30 shows the effect of the I_{dc} control bandwidth on stability when the system has a 3 kW CPL. It can be seen that increasing the I_{dc} control bandwidth results in attenuation of the low frequency oscillation in bus voltage. These results match the analytically predicted effect of the control bandwidth on stability which was discussed in Section III-B. Fig. 31 shows the impact of reduced droop gain. Due to the non-minimum phase property of the system, oscillation and eventual instability can be observed when k_1 becomes equal to 0.03. The result matches the stability prediction regarding the effect of droop gain in Section III-C and D, as previously discussed, it is the RHP zero which poses a challenge to system stability under small droop gain.

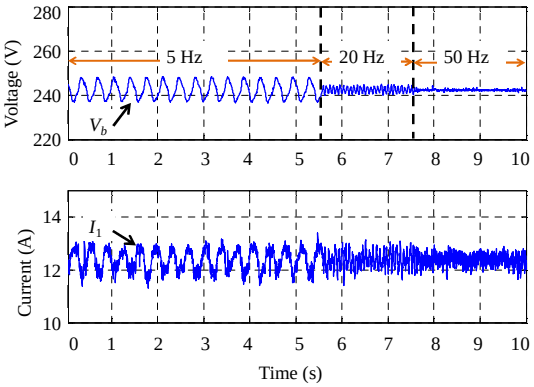


Fig. 30. Experimental results with varying control bandwidth.

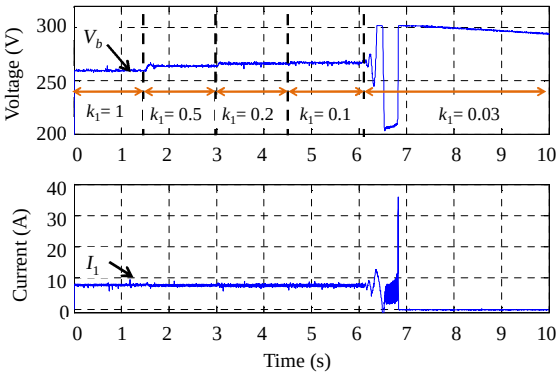


Fig. 31. Experimental results with decreased droop gain.

Fig. 32 shows the impact of current-mode droop control on the bus voltage control dynamics when the system is subjected to a load power step from 2 kW to 3 kW. In terms of the transient response, it can be seen in Fig. 32(a) that the transient time is 0.32 s for a droop gain, *k*, equal to 2, whilst the bus voltage reaches steady state much faster (0.2 s) if the droop gain is set to 1. This experimentally verifies that that the droop gain will affect the voltage loop bandwidth when utilizing the *current-mode* approach and confirms the discussion in Section III-B and C.

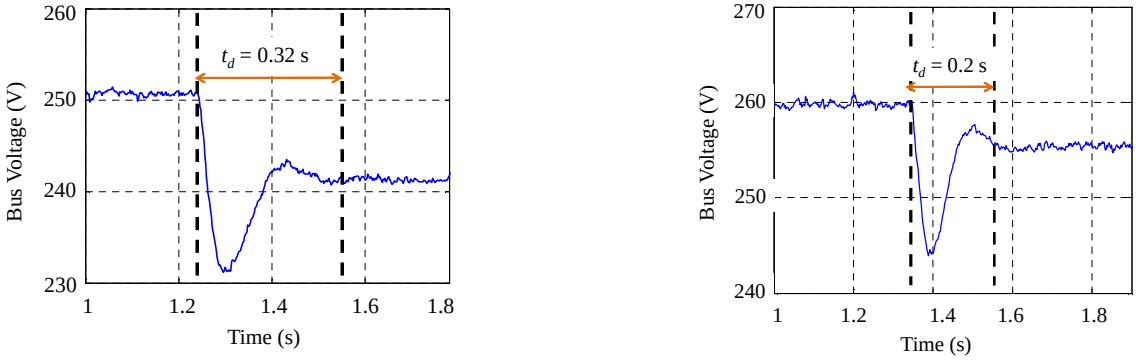


Fig. 32. Bus voltage dynamics in the current-mode droop-controlled system when subjecting to a load power step from 2 kW to 3 kW. (a) k = 2; (b) k = 1.

B. Voltage-mode Droop Control – Single Source

The voltage-mode droop control strategy (shown in Fig. 5) has also been tested with a single converter to observe the effect of the V_{dc} control bandwidth, and the droop gain, on the system stability. Due to the RHP zero, the V_{dc} control bandwidth needs to be limited for stable operation. Fig. 33 shows the experimental results with different V_{dc} control bandwidths. It can be seen that with a 10 Hz control bandwidth the system is stable over a CPL power ranging from 0 to 3 kW whilst with a 100 Hz control bandwidth the system shows significant oscillation when the load is around 3 kW. This result supports the instability discussion in Section III-B.

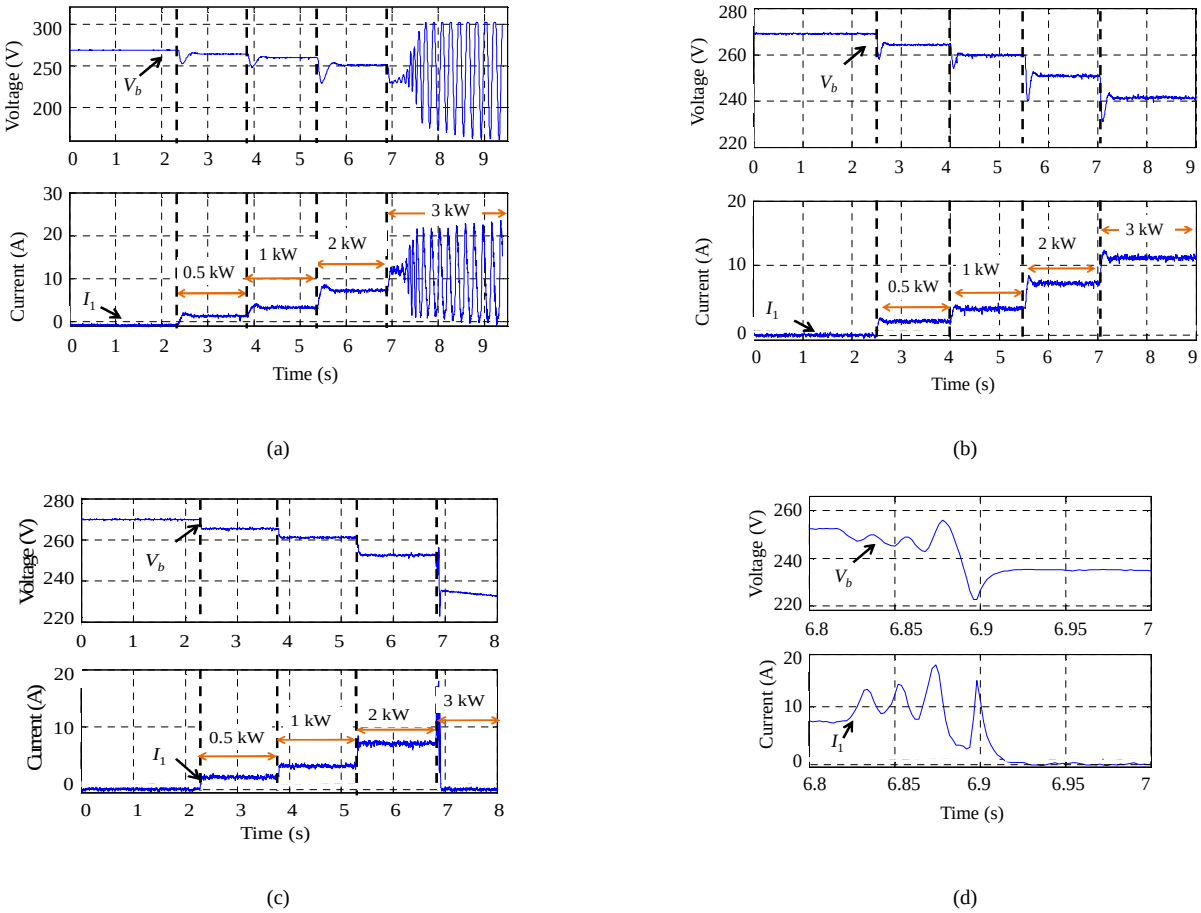


Fig. 33. Experimental result with different control bandwidths. (a) 3 Hz; (b) 10 Hz; (c)100 Hz; (d) Zoomed of oscillation part in (c).

Since the droop gain belongs to a feedforward path within the voltage-mode droop control scheme, the system stability will not be degraded by small droop gains. It can be seen from Fig. 34 that under voltage-mode droop control the system shows stability improvement under small droop gains in comparison with current-mode droop control (see Fig. 31). Again, this result is in accordance with the theoretical discussions in Section III-C and D.

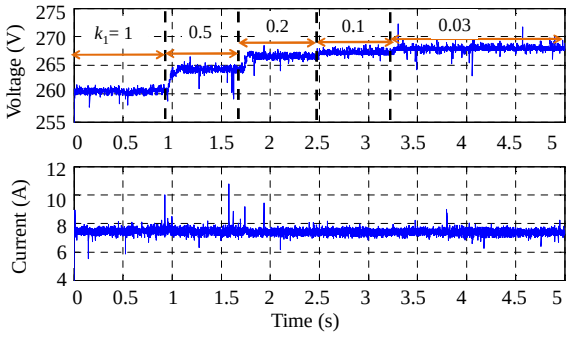
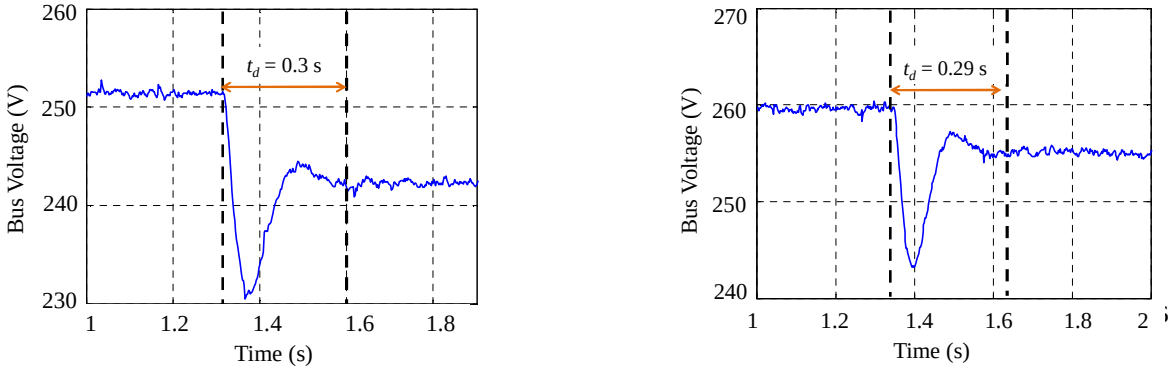


Fig. 34. Experimental result with varying droop gains at 10 Hz control bandwidth.

As a counterpart of Fig. 32, Fig. 35 shows the impact of voltage-mode droop control on the bus voltage dynamics when the system is subjected to a load power step from 2 kW to 3 kW. The steady-state bus voltage is identical in both Fig. 32 and Fig. 35;

251 V under 2 kW load and 260 V under 3 kW load. However, unlike the current-mode approach, for the voltage-mode droop-controlled system the transient time is very similar under different droop gains, supporting the analysis of DC voltage control dynamics presented in Section II-B.



(a) (b)

Fig. 35. Bus voltage dynamics in the voltage-mode droop-controlled system when subjecting to a load power step from 2 kW to 3 kW. (a) k = 2; (b) k = 1.

C. Parallel Operation

Parallel operation of multiple sources with identical global droop gain has also been tested to validate the expected stability improvements. The experimental results are shown in Fig. 36. It can be seen in Fig. 36(a) that under single source operation the system becomes unstable under a CPL of 6 kW. However, with the same global droop gain, stable operations of a twin source system and three source system are achieved, as shown in Fig. 36(b) and (c). The experimental results verify the discussion of system stability under parallel operation in Section IV-C (see Fig. 23(b)), and confirm that using the *current-mode* droop control approach, parallel operation with identical global droop gain can improve the system stability.

The effect of parallel operation with the same individual droop gain (k_i = 1) has been also tested and the results are shown in Fig. 37. As discussed in Section IV-C, the global droop gain reduces as the numbers of parallel modules with the same individual droop constant increases. The overall source impedance reduces and consequently, stability is improved by parallel operation. In Fig. 37, at t = 0 s, the load is set at 3 kW and only Conv 1 is operating. The instability point is predicted at 6 kW CPL (see Fig. 36(a)). At t = 1.1 s, Conv 2 is connected and begins to operate in parallel with Conv 1. As a result, the global droop gain reduces and the bus voltage increases. It can be seen that the twin source system is stable until the CPL reaches 7 kW. Again, this demonstrates that compared with single source operation, parallel operation with the same individual droop gains significantly improves the system stability (consistent with Fig. 23(a)).

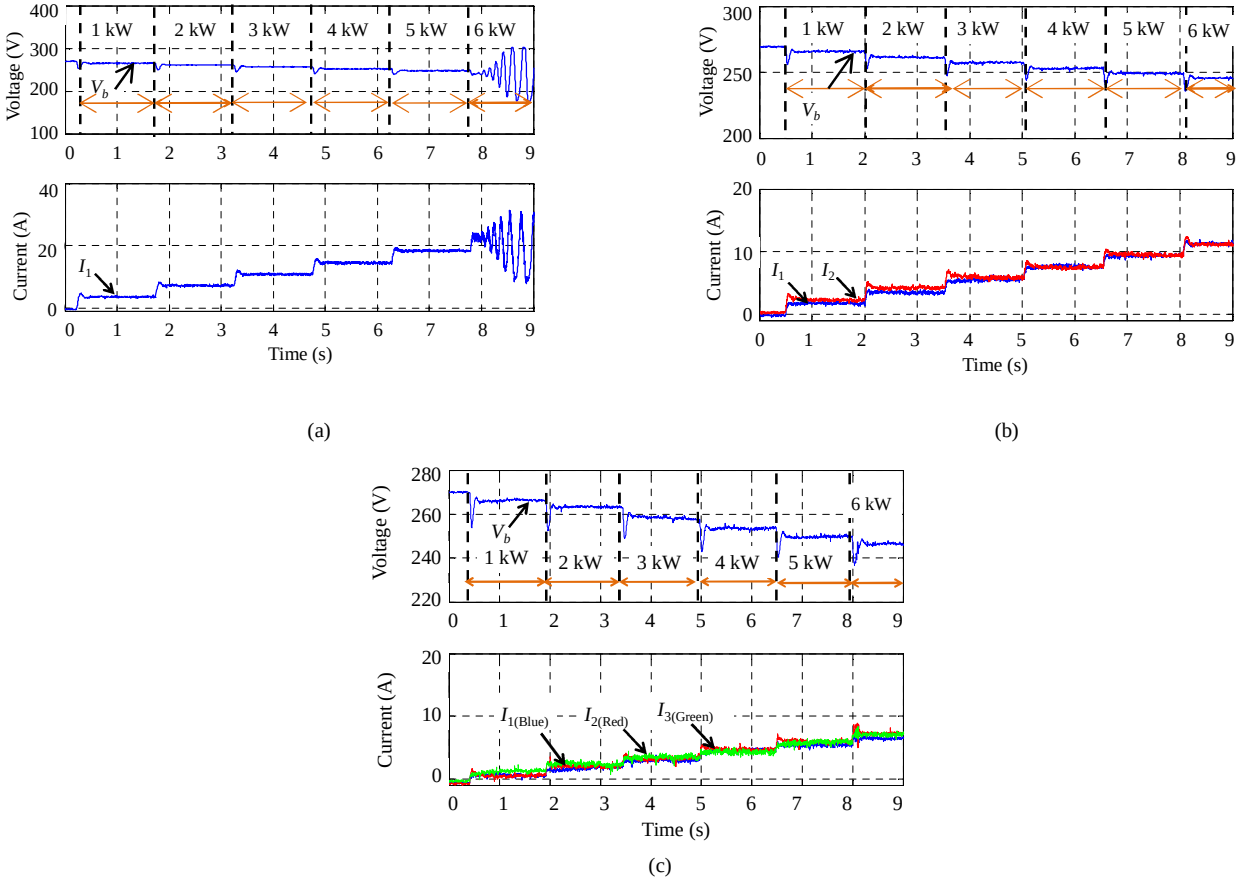


Fig. 36. Experimental results for parallel operation using the current-mode approach under 50 Hz control bandwidth. (a) Single source operation: Conv 1 operates at $k_1 = 1$, and Conv 2, 3 are disconnected. (b) Twin source operation: Conv 1, 2 operate at $k_1 = k_2 = 2$ ($k_t = 1$). (c) Three source operation: Conv 1, 2, 3 operate at $k_1 = k_2 = k_3 = 3$ ($k_t = 1$).

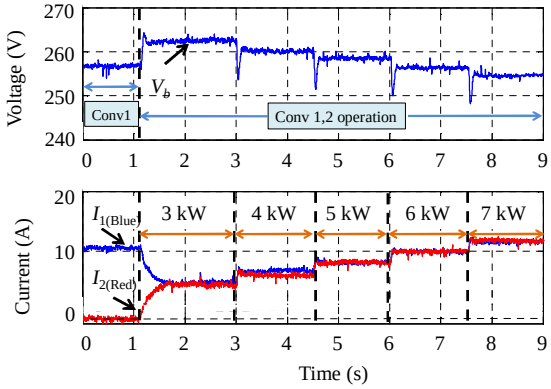


Fig. 37. Experiment result for parallel sources with identical individual droop gains ($k_1 = k_2 = 1$, $k_t = 0.5$).

VI. Conclusion

In this paper, current-mode (using the I-V characteristic) and voltage-mode (using the V-I characteristic) droop control schemes in VSC-based DC MGs were compared in terms of power sharing and stability. The equivalent source and load impedance have been derived and stability assessment of a generalized multi-source multi-load DC MG system has been carried

out to explore the impact of parallel operation. The theoretical analysis was supported by experimental results from a 7 kW lab prototype. The main findings of the paper can be highlighted as follows:

(1) Current-mode droop control uses a DC current controller to regulate the injected current from each terminal based on the voltage measurements. Among the *current-mode* droop control schemes, GVF shows better power sharing performance but additional sensors or communication lines are needed which compromises the modularity and reliability of droop control. LVF and GVF methods display similar stability performance when taking the converter dynamics into account.

(2) When utilizing current-mode droop control, increased DC current control bandwidth is helpful for stability enhancement of the system since it avoids the source/load impedance interactions. However, the upper boundary of DC current control bandwidth is limited by the RHP zero. For the current-mode droop-controlled system, the DC voltage dynamics are affected by the DC current control bandwidth and the droop gain. It has been demonstrated that increasing the droop gain will reduce the voltage loop bandwidth.

(3) In contrast to the current-mode approach, voltage-mode droop control regulates the terminal voltage based on current measurements. The RHP zero causes high gain instability within the V_{dc} controller, i.e. the system will easily go unstable when the V_{dc} controller has a high gain. When utilizing voltage-mode droop control, the voltage loop bandwidth is mainly determined by the voltage controller rather than the droop gain.

(4) Assuming the existence of a steady state operating point, and the absence of source/load impedance interactions, an upper boundary for the droop gain can be defined in both techniques. Under current-mode droop control, a lower boundary is imposed due to the RHP zero, whilst voltage-mode droop control is feasible for wider droop gain settings even under zero droop gain (constant DC voltage control).

(5) Global droop gain, a crucial factor to show the main bus V-I characteristic, was proposed in this paper to compare and analyze the stability of multi-source multi-load system. It has been shown both analytically and experimentally that parallel operation improves the system stability for both droop strategies.

APPENDIX

The state matrix of the current-mode droop-controlled system A_c discussed in Section III-D is shown as follows:

$$\begin{bmatrix} A_{c11} & A_{c12} & A_{c13} & A_{c14} & A_{c15} & A_{c16} \\ 0 & A_{c22} & 0 & 0 & A_{c25} & 0 \\ A_{c31} & A_{c32} & A_{c33} & A_{c34} & A_{c35} & A_{c36} \\ A_{c41} & A_{c42} & A_{c43} & A_{c44} & A_{c45} & A_{c46} \\ 0 & -K_{Idi} & 0 & 0 & 0 & 0 \\ A_{c61} & A_{c62} & A_{c63} & A_{c64} & A_{c65} & A_{c65} \end{bmatrix} \tag{A-1}$$

The matrix elements are shown below.

$$A_{c11}=\frac{3(-1/k*V_{dco}I_{qo}K_{Iqp}K_{Idcp}+I_{do}V_{do}+I_{qo}V_{qo})}{C_bV_{dco}\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)},\ A_{c12}=\frac{3(I_{do}K_{Idp}-V_{do}-\omega_eL_dI_{qo})}{C_b\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)},\ A_{c13}=\frac{3(I_{qo}K_{Iqp}-V_{qo}+\omega_eL_qI_{do})}{C_b\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)}$$

$$A_{c14}=\frac{3I_{qo}K_{Iqp}}{C_b\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)},\ A_{c15}=\frac{-3I_{do}}{C_b\left(3I_{qo}k_{Iqp}K_{Idcp}+2V_{dco}\right)},\ A_{c16}=\frac{-3I_{qo}}{C_b\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)}$$

$$A_{c22}=-\frac{K_{Idp}+R_s}{L_d},\ A_{c25}=\frac{1}{L_d}$$

$$A_{c31}=\frac{2K_{Iqp}K_{Idcp}V_{dco}^2+3kK_{Iqp}K_{Idcp}(I_{do}V_{do}+I_{qo}V_{qo})}{kL_qV_{dco}\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)},\ A_{c32}=\frac{3K_{Iqp}K_{Idcp}(I_{do}K_{Idp}-V_{do})+2\omega_eL_dV_{dco}}{L_q\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)}-\frac{\omega_eL_d}{L_q},\ A_{c33}=\frac{-2K_{Iqp}V_{dco}-3K_{Iqp}K_{Idcp}V_{qo}+3I_{do}K_{Iqp}K_{Idcp}\omega_e}{L_q\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)}-\frac{R_s}{L_q}$$

$$A_{c34}=-\frac{2K_{Iqp}V_{dco}}{L_q\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)},A_{c35}=-\frac{3I_{do}K_{Iqp}K_{Idcp}}{L_q\left(3I_{qo}K_{Iqp}K_{Vdcp}+2V_{dco}\right)},A_{c36}=\frac{2V_{dco}}{L_q\left(3I_{qo}K_{Iqp}K_{Vdcp}+2V_{dco}\right)}$$

$$A_{c41}=-\frac{K_{Idci}}{k}+\frac{3K_{Idci}(1/k*V_{dco}I_{qo}K_{iqp}K_{Idcp}-I_{do}V_{do}-I_{qo}V_{qo})}{V_{dco}\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)},\ A_{c42}=\frac{3K_{Idci}(-I_{do}K_{Idp}+V_{do}+I_{qo}\omega_eL_d)}{\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)},\ A_{c43}=\frac{3K_{Idci}(-I_{qo}K_{Iqp}+V_{qo}-I_{do}\omega_eL_q)}{\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)}$$

$$A_{c44}=\frac{-3I_{qo}K_{Iqp}K_{Idci}}{3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}},\ A_{c45}=\frac{3I_{do}K_{Idci}}{3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}},\ A_{c46}=\frac{3I_{qo}K_{Idci}}{3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}}$$

$$A_{c61}=\frac{K_{Iqi}K_{Idcp}K_{Iqi}}{k}+\frac{3K_{Iqi}K_{Idcp}(-1/k*V_{dco}I_{qo}K_{Iqp}K_{Idcp}+(I_{do}V_{do}+I_{qo}V_{qo}))}{V_{dco}\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)},\ A_{c62}=\frac{3K_{Iqi}K_{Idcp}(I_{do}K_{Idp}-V_{do}-I_{qo}\omega_eL_d)}{\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)},\ A_{c63}=-K_{Iqi}+\frac{3K_{Iqi}K_{Idcp}(I_{qo}K_{Iqp}-V_{qo}+I_{do}\omega_eL_q)}{\left(3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}\right)}$$

$$A_{c64}=-K_{Iqi}+\frac{3I_{qo}K_{Iqi}K_{Iqp}K_{Idcp}}{3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}},\ A_{c65}=\frac{-3I_{do}K_{Iqi}K_{Idcp}}{3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}},\ A_{c66}=\frac{-3I_{qo}K_{Iqi}K_{Idcp}}{3I_{qo}K_{Iqp}K_{Idcp}+2V_{dco}}$$

K_{Idp}, K_{Idi} are the proportional and integral gain of the *d*-axis current controller; K_{Iqp}, K_{Iqi} are the proportional and integral gain of the *q*-axis current controller; K_{Idcp}, K_{Idci} are the proportional and integral gain of dc current controller.

The state matrix of the voltage-mode droop-controlled system A_{v} discussed in Section III-D is shown as follows:

$$\begin{bmatrix} A_{v11} & A_{v12} & A_{v13} & A_{v14} & A_{v15} & A_{v16} \\ 0 & A_{v22} & 0 & 0 & A_{v25} & 0 \\ A_{v31} & A_{v32} & A_{v33} & A_{v34} & A_{v35} & A_{v36} \\ A_{v41} & A_{v42} & A_{v43} & A_{v44} & A_{v45} & A_{v46} \\ 0 & -K_{Idi} & 0 & 0 & 0 & 0 \\ A_{v61} & A_{v62} & A_{v63} & A_{v64} & A_{v65} & A_{v66} \end{bmatrix} \tag{A-2}$$

The matrix elements are shown below.

$$A_{v11}=\frac{3(-V_{dco}I_{qo}K_{Iqp}K_{Vdcp}+I_{do}V_{do}+I_{qo}V_{qo})}{C_bV_{dco}\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)},\ A_{v12}=\frac{3(I_{do}K_{Idp}-V_{do}-\omega_eL_dI_{qo})}{C_b\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)},\ A_{v13}=\frac{3(I_{qo}K_{Iqp}-V_{qo}+\omega_eL_qI_{do})}{C_b\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)}$$

$$A_{v14}=\frac{3I_{qo}K_{Iqp}}{C_b\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)},A_{v15}=\frac{-3I_{do}}{C_b\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)},A_{v16}=\frac{-3I_{qo}}{C_b\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)}$$

$$A_{v22}=-\frac{K_{Idp}+R_s}{L_d},\ A_{v25}=\frac{1}{L_d}$$

$$A_{v31}=\frac{2K_{Iqp}K_{Vdcp}V_{dco}^2+3kK_{Iqp}K_{Vdcp}(I_{do}V_{do}+I_{qo}V_{qo})}{L_qV_{dco}\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)},A_{v32}=\frac{3kK_{Iqp}K_{Vdcp}(I_{do}K_{Idp}-V_{do})+2\omega_eL_dV_{dco}}{L_q\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)}-\frac{\omega_eL_d}{L_q},A_{v33}=-\frac{2K_{Iqp}V_{dco}}{L_q\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)}$$

$$A_{v34}=-\frac{2K_{Iqp}V_{dco}}{L_q\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)},\ A_{v35}=-\frac{3I_{do}kK_{Iqp}K_{Vdcp}}{L_q\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)},\ A_{v36}=\frac{2V_{dco}}{L_q\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)}$$

$$A_{v41}=-K_{Vdci}+\frac{3kK_{Vdci}(V_{dco}I_{qo}K_{iqp}K_{Vdcp}-I_{do}V_{do}-I_{qo}V_{qo})}{V_{dco}\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)},\ A_{v42}=\frac{3kK_{Vdci}(-I_{do}K_{Idp}+V_{do}+I_{qo}\omega_eL_d)}{\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)},\ A_{v43}=\frac{3kK_{Vdci}(-I_{qo}K_{Iqp}+V_{qo}-I_{do}\omega_eL_q)}{\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)}$$

$$A_{v44}=\frac{-3I_{qo}kK_{Iqp}K_{Vdci}}{3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}},\ A_{v45}=\frac{3I_{do}kK_{Vdci}}{3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}},\ A_{v46}=\frac{3I_{qo}kK_{Vdci}}{3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}}$$

$$A_{v61}=K_{Iqi}K_{Vdcp}+\frac{3kK_{Iqi}K_{Vdcp}(-V_{dco}I_{qo}K_{Iqp}K_{Vdcp}+(I_{do}V_{do}+I_{qo}V_{qo}))}{V_{dco}\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)},\ A_{v62}=\frac{3kK_{Iqi}K_{Vdcp}(I_{do}K_{Idp}-V_{do}-I_{qo}\omega_eL_d)}{\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)},\ A_{v63}=-K_{Iqi}+\frac{3kK_{Iqi}K_{Vdcp}(I_{qo}K_{Iqp}-V_{qo}+I_{do}\omega_eL_q)}{\left(3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}\right)}$$

$$A_{v64}=-K_{Iqi}+\frac{3I_{qo}kK_{Iqi}K_{Iqp}K_{Vdcp}}{3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}},A_{v65}=\frac{-3I_{do}kK_{Iqi}K_{Vdcp}}{3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}},\ A_{v66}=\frac{-3I_{qo}kK_{Iqi}K_{Vdcp}}{3I_{qo}kK_{Iqp}K_{Vdcp}+2V_{dco}}$$

where K_{Vdcp}, K_{Vdci} are the proportional and integral gain of dc current controller.

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