Microelectronics Reliability 59 (2016) 73–83

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Quantification of cracked area in thermal path of high-power multi-chip modules using transient thermal impedance measurement

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ARTICLE INFO

Article history:
Received 7 August 2015
Received in revised form 23 November 2015
Accepted 9 January 2016
Available online 25 January 2016

Keywords:
Structure function
Reliability
Power modules
Solder fatigue

ABSTRACT

Transient thermal impedance measurement is commonly used to characterize the dynamic behaviour of the heat flow path in power semiconductor packages. This can be used to derive a "structure function" which is a graphical representation of the internal structure of the thermal stack. Changes in the structure function can thus be used as a non-destructive testing tool for detecting and locating defects in the thermal path. This paper evaluates the use of the structure function for testing the integrity of the thermal path in high power multi-chip modules. A 1.2 kV/200 A IGBT module is subjected to power cycling with a constant current. The structure function is used to estimate the level of disruption at the interface between the substrate and the baseplate/case. Comparison with estimations of cracked area obtained by scanning acoustic microscopy (SAM) imaging shows excellent agreement, demonstrating that the structure function can be used as a quantitative tool for estimating the level of degradation. Metallurgical cross-sectioning confirms that the degradation is due to fatigue cracking of the substrate mount-down solder.

1. Introduction

Degradation of the thermal conduction path is among the dominant failure mechanisms of power semiconductor packages. Typically, solder fatigue results from the thermo-mechanical stresses at the interfacing contacts due to mismatched coefficient of thermal expansions (CTEs) between different materials which constitute the heat flow path causing cracking. The correlation between solder fatigue and the degradation in the thermal performance of power semiconductor packages has been previously reported in the literature [1–4]. Increase in thermal resistance occurs because heat dissipation through the package is compromised by the disruption in interconnection resulting from solder fatigue. There have been some attempts to quantify the correlation between the increment in thermal resistance and the cracked area of solder layers [5–8]. However, all of these studies focused on single chip packages (e.g. TO-247), none of which considered high power multi-chip semiconductor packages. In addition, most of these studies relied on finite-element modelling (FEM) to quantify the relationship between unattached area and thermal resistance.

Thermal transient measurement is a common characterization method of the heat conduction path of power semiconductor packages. Many researchers have reported that the thermal impedance of a thermal stack is representative of the internal structure of the thermal stack [9,10]. This fact legitimizes the use of thermal impedance as a non-destructive evaluation tool to detect structural defects in the heat conduction path. Szekely [11] proposed an accurate systematic procedure which allows a mapping of the internal structure based on the thermal impedance measurement. The proposed procedure produces a "structure function" which is a graphical tool that represents the internal structure of the thermal stack of an encapsulated semiconductor package. The structure function can therefore be used as a failure analysis tool to detect, locate and estimate cracking and voiding which results from solder fatigue in power semiconductor packages [11]. This method has been recognized by the "JEDEC" standards series "JESD51" for thermal characterization of packaged semiconductor devices [12].

In this work, the validity of the structure function as a non-destructive evaluation tool for high power multi-chip semiconductor packages is investigated. Junction-to-case thermal resistance R_{thjc} and cracked area, estimated by structure function, are compared to the cracked and unattached area estimated by Scanning Acoustic Microscopy (SAM). For this purpose, a conventional 1.2 kV/200 A IGBT power module is actively power-cycled to degrade the solder at the substrate-base plate interface. SAM imaging is performed at regular intervals at multiple stages of the power cycling test to observe the gradual degradation of the

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http://dx.doi.org/10.1016/j.microrel.2016.01.002

solder layer. Thermal impedance measurements are also recorded regularly during the power cycling test and the structure function is calculated. The junction-to-case thermal resistance R_{thjc} and detached area estimated by the structure function are then compared to the cracked area estimated from the SAM images.

2. Theoretical background

To facilitate the interpretation and discussion of the results, it is helpful to briefly review the theoretical background regarding the structure function. It is common for the heat flow path to be represented by an equivalent electrical RC Cauer network. This Cauer-type model is considered to be a physical description of the heat flow path [13]. The structure function is a graphical representation of the components of the Cauer network which represents the heat flow path [11]. The most common methods of Cauer network parameterization rely on material and geometrical properties [14] or on experimental measurement [13] and typically produce models up to the 6th order. However, in order to get an accurate representation of the physical structure by the structure function, a higher order Cauer network is required.

Fig. 1. Mentor Graphics Power Tester 1500A used for power cycling test.

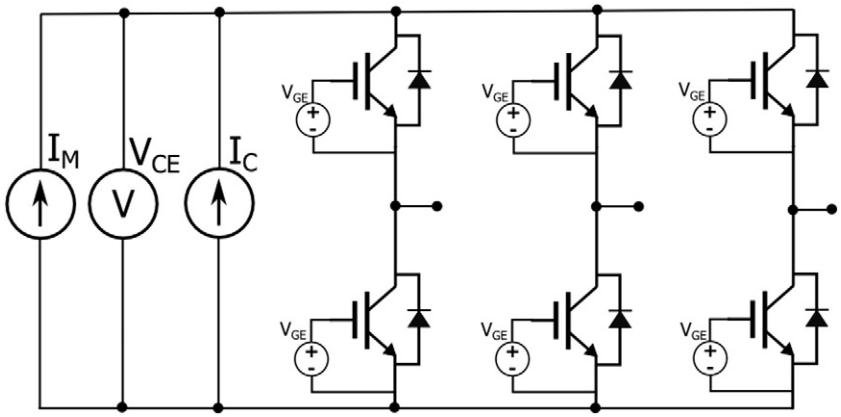

Fig. 2. All 6 IGBTs are biased with a Voltage $V_{GE.}$ Cycling Current I_C and Measurement Current I_M are shared among all IGBTs. V_{CE} measurement is a global measurement averaged among all IGBTs.

Szekely [15] presents a method which allows a high order Cauer network model to be identified from an experimental measurement of the thermal impedance. The method is based on extracting the time constants τ and thermal resistances R of the network from the thermal impedance. These two values constitute a function called the time-constant spectrum $R(\tau)$ [15] which is continuous for a distributed network. The discretization of $R(\tau)$ results in a finite number of τ values and their corresponding amplitudes R which can be used to identify a high order Foster type network. The transformation of Foster–Cauer [16] then produces the high order Cauer network required for the structure function. The original work can be found in [11,15,17] and the references therein.

2.1. Cumulative structure function

This form of structure function is a representation of the cumulative thermal capacitances C_Σ as a function of the cumulative thermal resistances R_Σ of the Cauer network, where the vertical axis C_Σ and the horizontal axis R_Σ are defined as:

$$C_\Sigma = \sum_{i=1}^{n} C_i, \quad R_\Sigma = \sum_{i=1}^{n} R_i \tag{1}$$

where C_i and R_i are the thermal capacitance and thermal resistance of the Cauer network respectively and n is the number of RC components. This function is also called the "Protonotarios–Wing function" after the authors of the original work [18].

2.2. Differential structure function

This form of structure function represents the derivative of the cumulative capacitance C_Σ as a function of the cumulative thermal resistances R_Σ. For a one-dimensional homogenous thermal conduction path, the derivative K_Σ is expressed by [17]:

$$K_\Sigma = \frac{dC_\Sigma}{dR_\Sigma} = \lambda c A^2 \tag{2}$$

where c is the specific heat capacity ($W \cdot s/K$) and $\boldsymbol{\lambda}$ is the thermal conductivity ($W \cdot m^{-1} \cdot K^{-1}$). Therefore, the cross-sectional area as well as the thickness of the layers can be calculated if the thermal conductivity $\boldsymbol{\lambda}$ and specific heat capacity c of the materials are known [17].

3. Experimental procedure

The power cycling test was performed using a "MentorGraphics" Power Tester 1500 A [19] shown in Fig. 1. The IGBT module subjected to cycling is an off-the-shelf 3-phase module rated at 1.2 kV/200 A. The module was mounted on a cold plate with a 25 μm thick Kapton film used as an interfacing material between the cold plate and the baseplate. The purpose of the Kapton film was to increase the case-to-ambient thermal resistance in order to achieve a temperature swing at

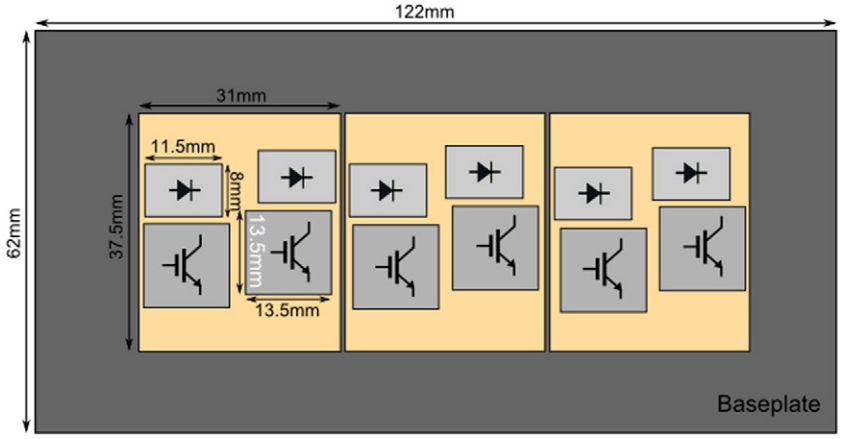

Fig. 3. A drawing of the layout of the module under test. Three substrates are mounted on a copper baseplate. Each substrate tile has 2 IGBT chips and 2 Diodes.

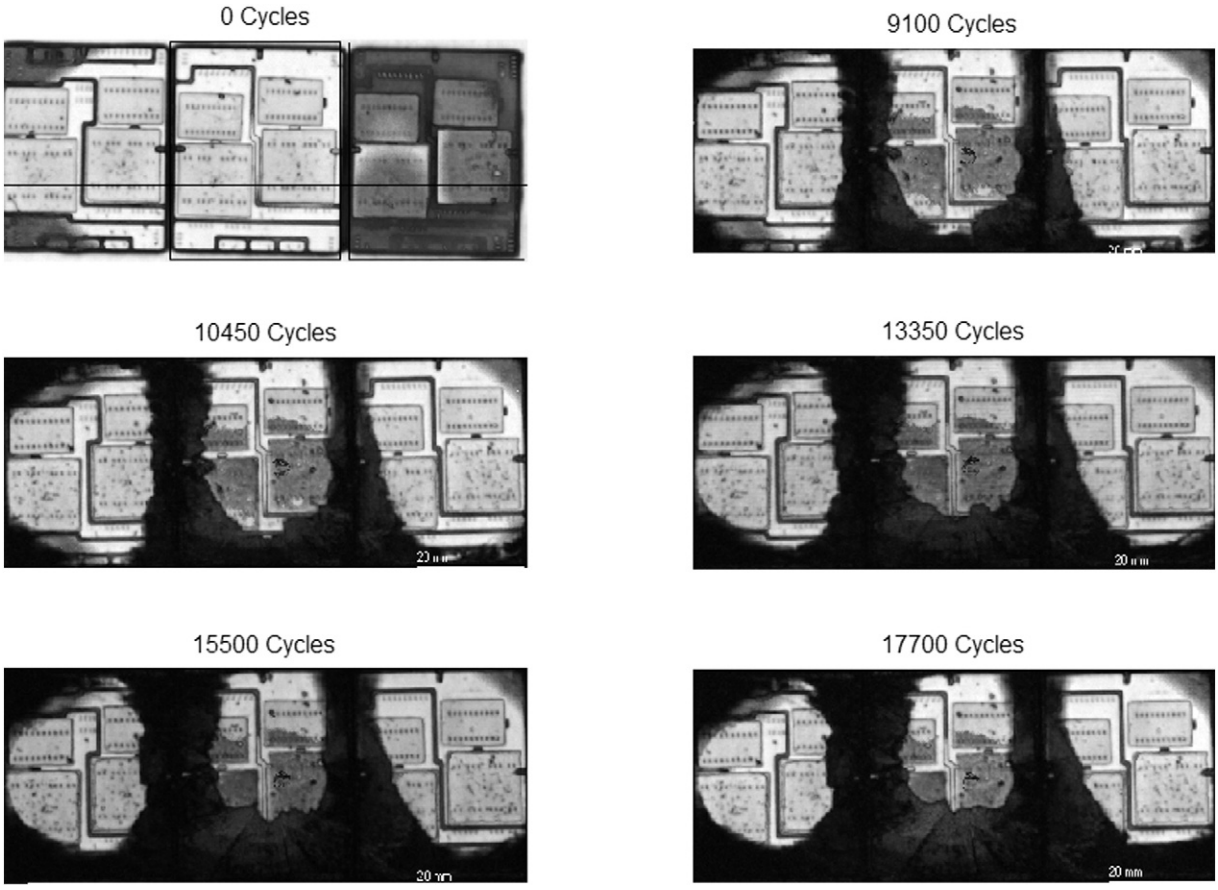

Fig. 4. Scanning acoustic microscopy images at different cycles during the power cycling test.

the substrate-case interface and so accelerate the degradation of substrate mount-down solder layer compared to other failure mechanisms.

The module was set up for power cycling in the configuration shown in Fig. 2. The tested module contains 6 IGBT devices and 6 freewheeling diodes mounted on three substrate tiles. The layout of the tested module is shown in Fig. 3. All IGBTs were biased with a gate-emitter voltage $V_{GE} = 15$ V such that the cycling current I_C as well as the measurement current I_M were shared between the three legs of the module. The collector–emitter voltage V_{CE} is a global measurement across the whole module and therefore, it represents an "average" measurement of the three legs.

The module junction temperature T_J was estimated using the collector-emitter voltage drop V_{CE} as a thermo-sensitive electrical parameter. A calibration curve $T_J = f(V_{CE})$ at a constant measurement current of $I_M = 200$ mA was used to calculate junction temperature T_J. Since the V_{CE} value is a global measurement across the whole module, the junction temperature T_J is a global temperature which is a representative temperature of all the IGBTs rather than an estimate of the actual temperature of any given device in the module. An actual measurement of the temperature at the substrate was obtained via the module integrated NTC (negative temperature coefficient) temperature sensor.

The cycling current I_C was regulated by the power tester to preserve a constant $\Delta T_J = 120$ K with $T_{Jmax} = 140$ °C and $T_{Jmin} = 20$ °C as estimated from V_{CE} where the water temperature was maintained at 20 °C. The heating time and cooling time were fixed at 50 s, and 60 s, respectively. This achieved a ΔT of 70 K at the substrate with $T_{max} = 90$ °C and $T_{min} = 20$ °C. The test started with an initial cycling current $I_C = 236$ A which resulted in a power dissipation $P_D = 704$ W. As the thermal resistance increased during the test due to solder fatigue, the cycling current was regulated to keep the ΔT_J constant. As a result, the cycling current decreased to $I_C = 213$ A by the end of the test, resulting in a power dissipation $P_D = 600$ W. Under these conditions, the wire-bond lift-off mechanism is not the dominant mechanism and the substrate mount-down solder degrades before any wire-bond lift-off is observed.

The power cycling was paused regularly every 1000 cycles, at which time a thermal impedance measurement was made with the module in situ. That resulted in a total of 17 thermal impedance measurements. A heating current of 150 A was used for the thermal transient measurement

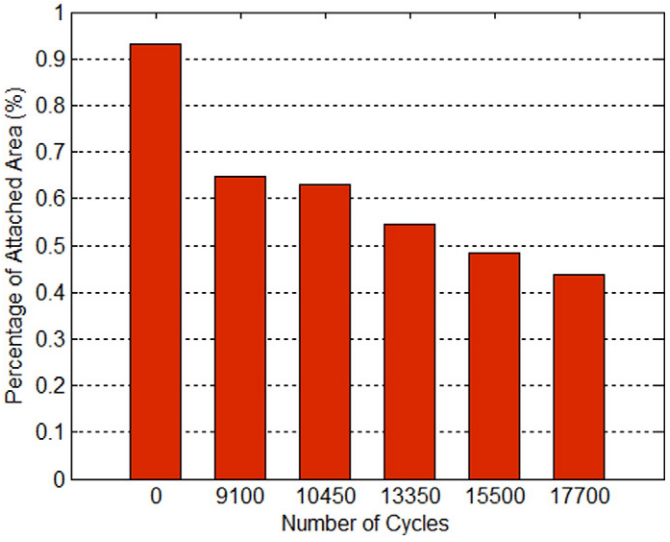

Fig. 5. Attached area of solder layer during the power cycling test as estimated from SAM images.

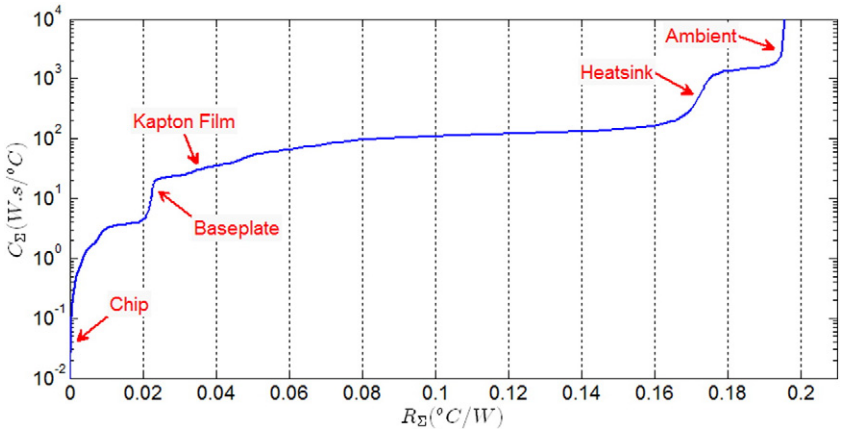

Fig. 6. The cumulative structure function. Different layers of the thermal stack can be identified.

which produced a power dissipation of 360 W. The junction temperature T_J was calculated using the common method $T_J = f(V_{CE})$ and the structure function extracted from the thermal transient measurements using the "T3Ster-Master" evaluation tool provided by "MentorGraphics".

SAM characterization was carried out during the power cycling test using a PVA TePla AM300. Scanning acoustic microscopy is a non-destructive technique to image the internal features of a specimen and can detect discontinuities and voids of sub-micron thickness. C-mode scanning (interface scan) was conducted with a 35 MHz transducer to provide planar view on several focused depths, from the base-plate, corresponding to specific internal layers. This creates 2D greyscale images from the reflected ultrasonic echoes. Defects at any of the internal layers cause discontinuity in the structure and block the ultrasonic signal preventing it from penetrating through the layers beneath the defected areas. Thus, defects in the substrate solder result in a black shadow appearing in the C scan images taken from the chip level. In this way, the C scan images were used to obtain distinct boundaries between the attached and discontinuous areas. However, the exact location of the defects within the structure can be unclear from SAM images, and therefore, correlative metallurgical cross-sectioning is necessary.

The power cycling test was terminated after 17,700 cycles by which time the total junction-to-ambient thermal resistance R_{thja} had increased by 14% from its original value. After examination, all IGBT devices were still electrically functional. Following the final SAM observation, metallurgical cross-sections were prepared and examined under an optical microscope in order to confirm the degradation mode.

4. Estimating the attached area from SAM images

The module was imaged in its original state, i.e. prior to power cycling. No cracks or voids were observed in the internal layers at that stage. The power cycling test was interrupted for SAM imaging at 9100, 10,450, 13,350, and 15,500 cycles. At 17,700 cycles, the test was terminated and a final scan was performed. The SAM images are shown in Fig. 4.

The attached area of the solder layer is estimated as a percentage of the total area from the SAM images shown in Fig. 4. This is realized in MATLAB. The image was transformed into a black/white image where the white pixels indicate attached area and the black pixels indicate cracked area. The percentage of attached area is calculated as:

$$\text{Attached area}(\%) = \frac{\text{number of white pixels}}{\text{total number of pixels}}.$$

Fig. 5 shows the estimated attached area of the solder layer at different cycle numbers during the cycling test. At zero cycles, the attached area is estimated to be 93%. This is because the processing algorithm recognizes the separation lines between different substrates and between copper tracers and the wire bond footprints as black (cracked) pixels. However, this error does not affect the observed trends as it is persistent in the remaining images. As the number of cycles increases, cracking propagates through the solder causing the attached area to be reduced gradually until it reaches 43% test after 17,700 cycles.

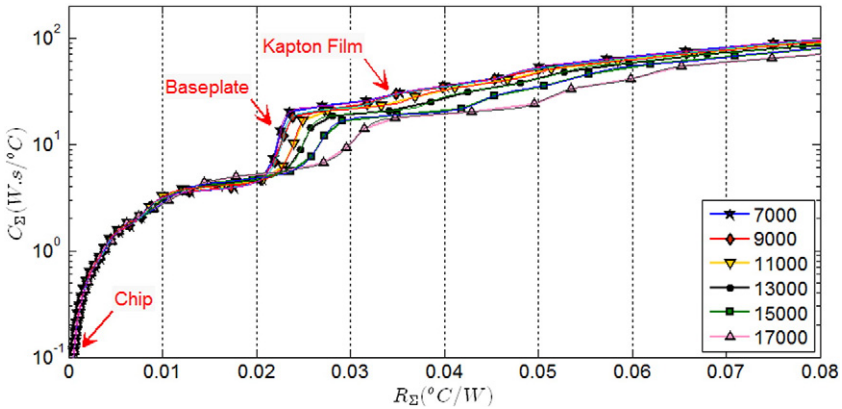

Fig. 7. A magnification of the substrate-baseplate interface region showing the effect of solder fatigue.

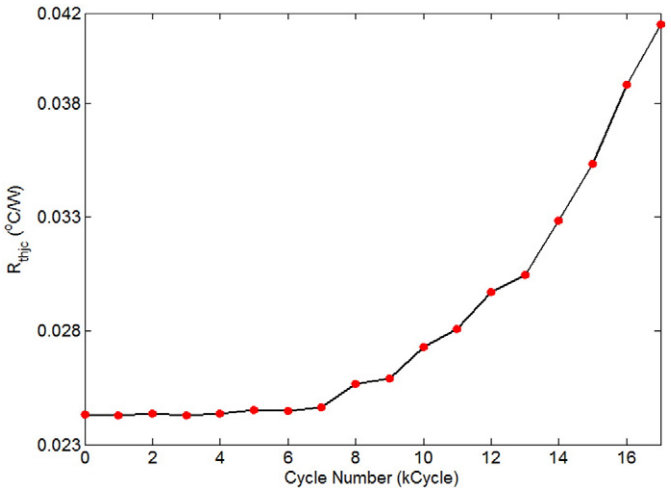

Fig. 8. The change in the junction-to-case thermal resistance R_{thjc} during the power cycling test as a result of solder fatigue.

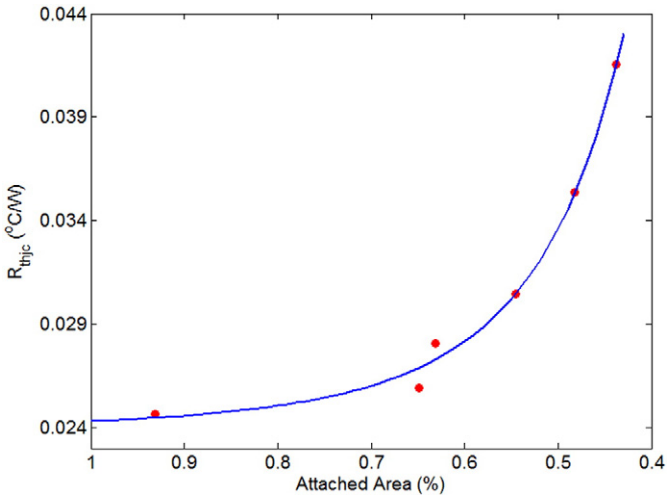

Fig. 10. R_{thjc} is correlated to the cross-sectional area of the solder layer. A reduced attached area results in a higher R_{thjc}.

5. Evaluation of structure function

5.1. Cumulative structure function

Fig. 6 shows the cumulative (integral) structure function obtained at 7000 cycles. With this structure function, different layers in the thermal stack can be identified starting with the ambient (water) at the right-hand side, which appears as a vertical line indicating a theoretical infinite thermal capacitance. To its left, another significant vertical rise can be seen which indicates the large thermal capacitance of the heatsink. The flat region between the two lines relates to the thermal resistance of the heatsink. From this region, the thermal resistance of the heat sink can be estimated. However, because of the variability in both the water temperature and the flow rate of the water in the heatsink, the thermal resistance of the heatsink is not constant. Therefore, it is estimated during the test to be within a range [0.021–0.027]°C/W.

The next vertical inflexion to the left indicates the thermal capacitance of the thermal interfacing material which is, in this case, the Kapton film. Then there is another significant vertical drop which indicates the module copper base plate. It can be seen that the thermal capacitance of the Kapton film is small compared to the thermal capacitance of the baseplate and the heatsink. A wide flat region over the x-axis can be seen between the Kapton film and the heatsink. This region indicates the high thermal resistance of the Kapton film which is estimated from the structure function to be 0.142 °C/W.

The thermal resistance of this thermal interface is variable since the module is demounted at multiple stages during the power cycling test to perform SAM scanning and remounted afterwards. This mounting/demounting process disturbs the thermal resistance of the thermal interface. Every time the module is mounted after performing the SAM scanning, the thermal contact between the interfaces (baseplate-to-Kapton and Kapton-to-coldplate) is different. As a result of this, the junction-to-ambient thermal resistance R_{thja} is different every time. This adds to the variability in the heatsink thermal resistance explained above. And therefore, the junction-to-ambient thermal resistance R_{thja} becomes variable and inconsistent during the test. On the contrary, the junction-to-case thermal resistance R_{thjc} is not affected by mounting/dismounting of the module, so changes internal to the package which can be characterized using the junction-to-case thermal resistance R_{thjc} are not affected by the variability of the heatsink and the thermal interface. Therefore, the region of the structure function from the chip to the baseplate forms the focus of these studies, whereas the variable region related to the thermal interface and the heatsink is ignored.

No change was observed in the structure function from the beginning of the test until 7000 cycles. Therefore, the data presented for 7000 cycles also represents the structure function of the module in its original state. After 8000 cycles a gradual change is clear. Fig. 7 shows that a change develops in the structure function as the number of cycles increases. This change appears as an increasing thermal resistance since the curve is shifting to the right over the x-axis with the increasing number of cycles. The change starts at the interface between the baseplate region and substrate where an expansion over the x-axis can be spotted. However, it is difficult to conclude from this plot alone exactly where in the solder interface region the cracking is happening.

The junction-to-case thermal resistance R_{thjc} can be measured from the structure function at the end of the baseplate region and before the start of the Kapton film region. Fig. 8 shows R_{thjc} as a function of number of cycles. It can be seen that R_{thjc} stays unchanged until 8000 cycles, and from this point onwards it increases progressively until the end of the test. The total increment in R_{thjc} is about 70% from its original value which is estimated as 0.024 °C/W. This increment is a result of cracks in the solder at the substrate-base-plate interface which is confirmed by metallurgical cross-sectioning as shown in Fig. 9.

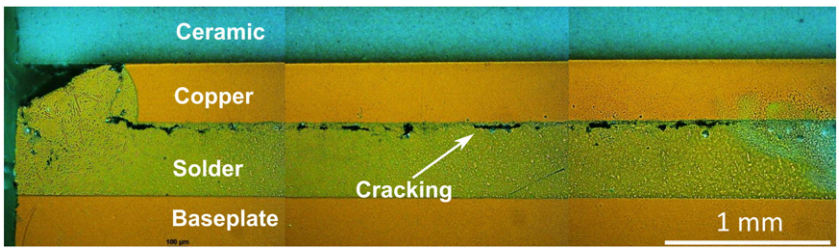

Fig. 9. Image of metallurgical cross-section shows the cracking resulting from power cycling at the substrate-baseplate interface.

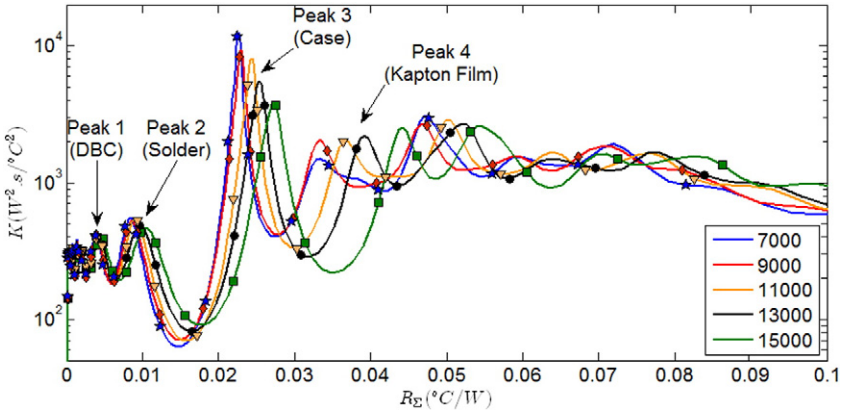

Fig. 11. The differential structure function during the power cycle test. Different peaks indicate different layers.

Fig. 10 shows values of R_{thjc} measured at 7000, 9000, 11,000, 15,000, and 17,000 cycles plotted as a function of the percentage of attached area as estimated from the SAM images of Fig. 4. It can be seen that as the attached area decreases the thermal resistance increases rapidly.

It can be noted from Fig. 10 that the sensitivity of the structure function for structural defects is dependent on the location of the semiconductor chip relative to the location of the defect. That is, it has higher sensitivity for defects located directly below the chip such that the defect has a direct thermal effect on the chip, whereas a defect located far from the chip would result in lower sensitivity of the structure function for that defect. That is the reason why no change in the structure function is seen until 35% of the substrate-case solder layer is cracked through. Cracking of the solder starts at the corners of the substrate and initially this has little effect on the heat flowing from the semiconductor chips towards the heatsink. With propagation of the cracking towards the center of the substrate, the heat flow is obstructed and only then does the structure function start to indicate the presence of a defect.

5.2. Differential structure function

Fig. 11 shows the differential structure function $K(R_\Sigma)$ between 7000 cycles and 15,000 cycles. As noted in Section 2, the differential structure function $K(R_\Sigma)$ is proportional to the squared cross-sectional area A^2. Each peak in this plot indicates a new layer of material with a different cross-sectional area. A decrease in the amplitude of a peak indicates a reduction in cross-sectional area of the layer related to that peak. The shift in the location of the peak along the x-axis indicates a change in the thermal resistance of this layer. Therefore, the thermal resistance of the individual layers can be identified. In addition, the thickness can be identified if the material properties are known [17].

In Fig. 11 the most significant peak is Peak 3, which is related to the baseplate layer. Peak 1 is related to the Direct-Bonded Copper substrate (DBC), Peak 2 is related to the solder layer and Peak 4 is related to the Kapton film. The most significant changes can be seen in the amplitude of peaks 2 & 3, which are decreasing. Peak 1 and Peak 4, on the other hand, remain at almost constant amplitude. This decrease in the amplitude signifies a reduced cross-sectional area of the solder layer which is at the interface between the DBC substrate and the baseplate. This is accompanied by an increase in the thermal resistance of the solder layer which is indicated by a shift in the location of Peak 2 and Peak 3 along the positive x-axis.

The K-value of Peak 3 plotted against number of cycles is shown in Fig. 12. The decrease in the K-value is clear as the number of cycles increases, and is indicative of reduced cross-sectional area. In order to reveal the relationship between the two quantities, the cross-sectional area estimated earlier from the SAM images is compared to the K-value given by the differential structure function as shown in Fig. 13. It can be seen that the K-value is linearly correlated to the cross-sectional area squared. This is in agreement with the theoretical relationship in Eq. (2).

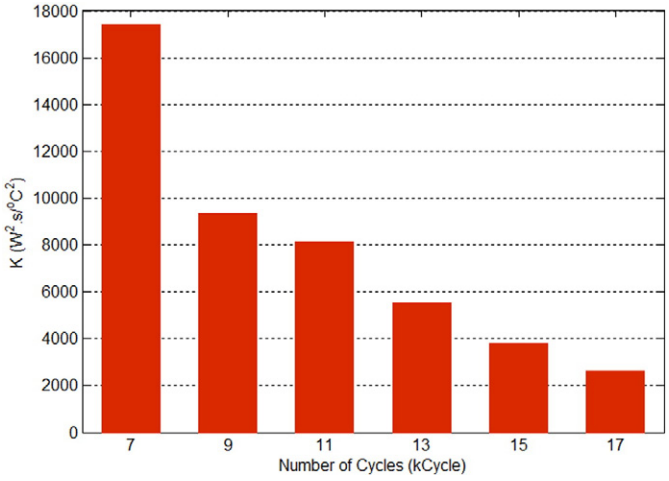

Fig. 12. The K-value of the case region shows a steady decline over the power cycling test. This indicates a decreasing cross-sectional area.

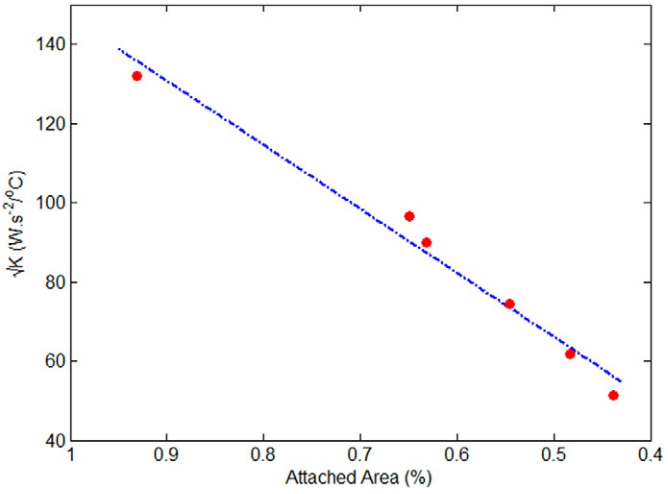

Fig. 13. K-value given by the differential structure function at the baseplate region has a linear correlation to the square of the fractional cross-sectional area of the solder layer.

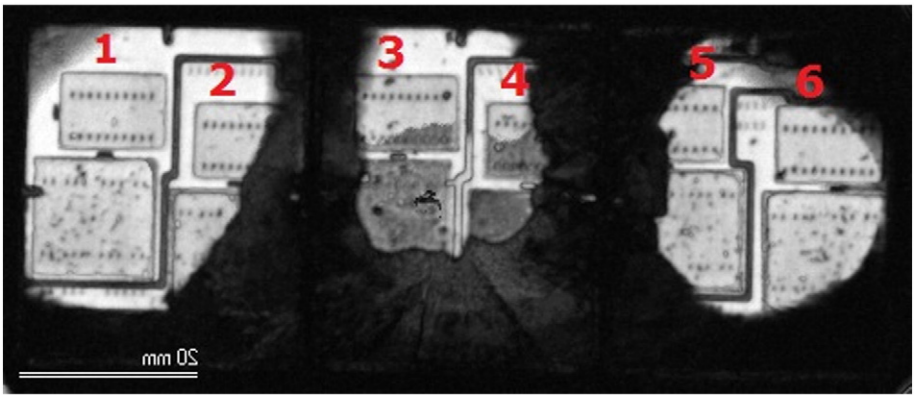

Fig. 14. SAM image of the cycled module at 17,700 cycles shows different levels of delamination under different IGBT devices.

6. Local structure function of individual IGBT devices

All the IGBT devices were still functional at the end of the power cycling test (17,700 cycles). At 17,700 cycles, the SAM image shows different levels of discontinuity beneath the different IGBT devices. Therefore, an investigation has been carried out to examine whether this non-uniformity in heat flow can be observed in the structure functions for the individual IGBT chips. For this investigation, thermal paste was used as the interface material instead of the Kapton film used during the power cycling test. The local thermal impedance of each individual IGBT in the module was measured and the structure function was calculated.

The attached area under each individual IGBT is estimated from the SAM image at 17,700 cycles which is shown in Fig. 14. The IGBT devices are numbered from 1 to 6 and the area under each IGBT is cropped to calculate the attached area in the same way described earlier in Section 5. The cropped images are shown in Fig. 15. The percentage attached area under each device is shown in Fig. 16. According to the percentage of attached area local to the IGBTs, devices are sorted from the lowest to the highest as: Device 4, Device 2, Device 3, Device 5, Device 6, and Device 1.

Fig. 17 shows the cumulative structure function for the individual IGBTs. A large difference can be seen between the curves as a result of the different levels of discontinuity in the substrate to baseplate interface area below each IGBT. The different layers can be most easily identified on the curve related to Device 1 and Device 6 as they are the least affected by the solder fatigue. The features of the different layers in the structure start to disappear as the level of the local delamination increases. Device 4 is the worst affected by cracking and the different layers' features cannot be distinguished.

This can be seen clearly in the differential structure function of the IGBTs shown in Fig. 18. Peak 3 and Peak 4 related to the baseplate and heatsink respectively are barely visible on the curves of Device 2 and

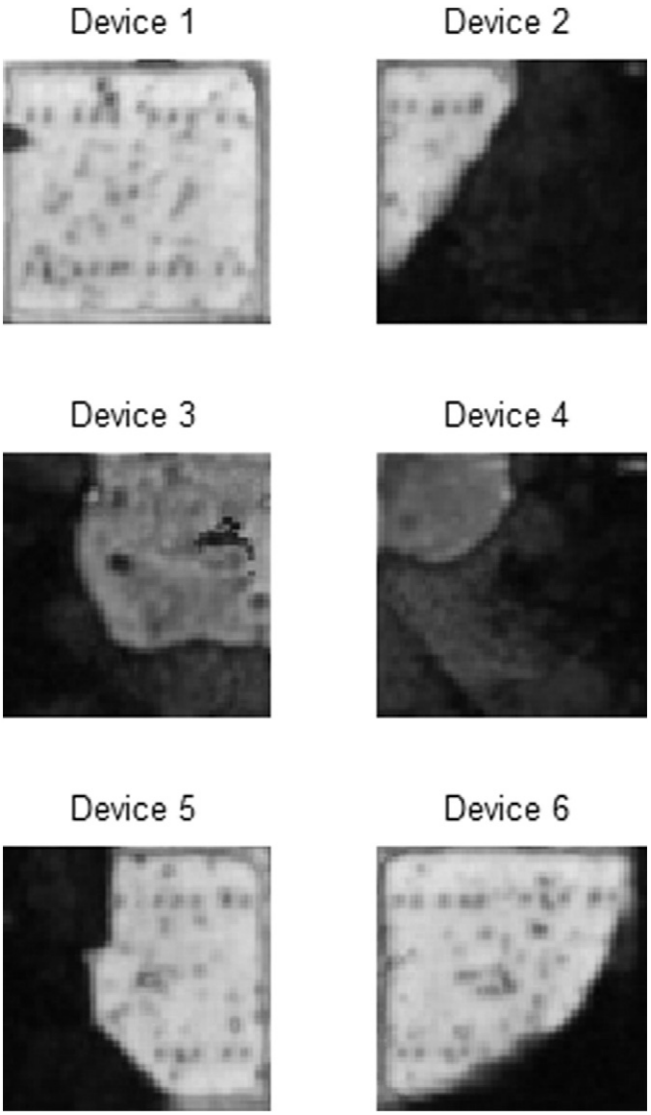

Fig. 15. Cropped images used to estimate attached area local to the IGBT devices.

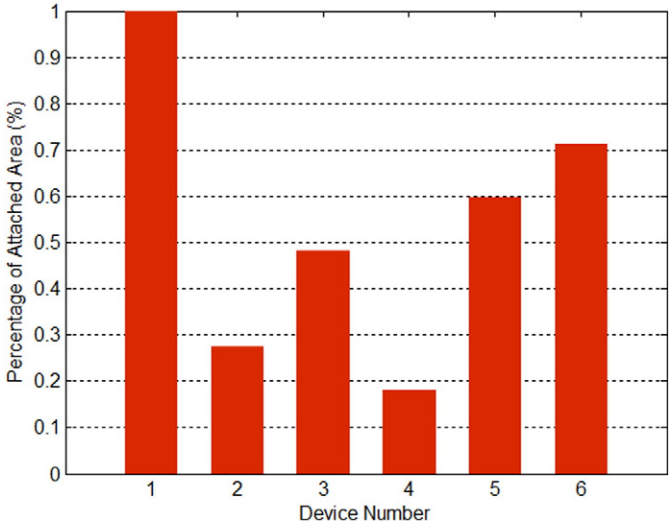

Fig. 16. Percentage of attached area local to the IGBT devices after 17,700 cycles.

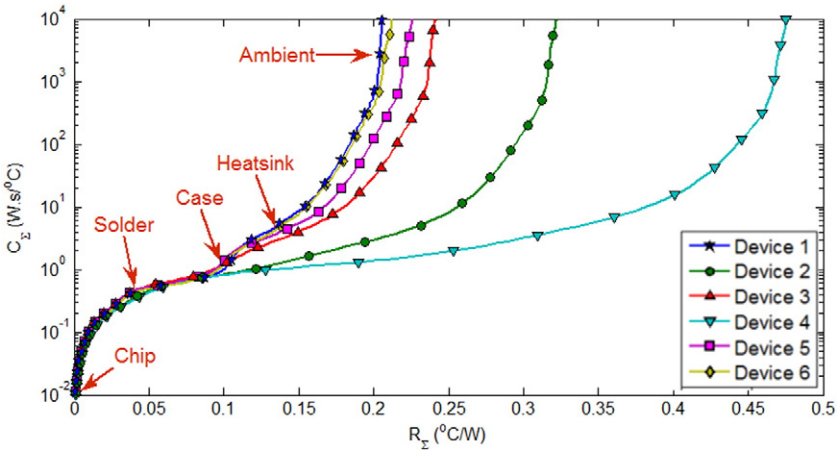

Fig. 17. The cumulative structure function of individual IGBT devices after 17,700 cycles.

Device 4. A decline in the amplitude of most of the peaks can be identified corresponding to an increase in the level of cracked area under each IGBT. However, cross-sectioning has only identified cracking in the substrate to baseplate solder layer.

Because the thermal impedance measurements of the individual IGBTs are taken at the same time for all the devices, the variability in the heatsink thermal resistance due to water temperature and the flow rate is trivial. Therefore, the junction-to-ambient thermal resistance R_{thja} is may be directly compared with the percentage of attached area below the individual IGBTs. Fig. 19 shows R_{thja} for individual IGBT devices as estimated from the structure functions. It can be seen that there is a correlation between the attached areas shown in Fig. 16 and the estimated R_{thja} per IGBT.

Fig. 20 shows R_{thja} of the individual IGBTs as a function of attached area of the solder under each IGBT. Similar to the result shown in Fig. 10, it can be seen that the R_{thja} is correlated to the attached area.

Fig. 21 shows the K-value of the baseplate region (Peak 3) of the individual IGBTs as extracted from the differential structure function in Fig. 18. Device 1 has the highest K-value, whereas the lowest K-value is for Device 4. This is in good agreement with the attached area of the solder layer below the individual IGBTs. Plotting K-value against the square of the percentage of attached area shows a clear linear correlation as shown in Fig. 22.

The scattering of the data around the fitted curve in Fig. 22 can be justified by the effect of heat spreading on the measured thermal impedance. The attached area below the individual IGBTs is estimated as a rectangular heat flow path of a size equal to the chip size. Typically, the effective area of the heat flow path is larger due to the lateral heat spreading which accompanies the vertical flow of heat. This results in a cone-shaped heat flow path where the area of the bottom surface (case) is larger than the area of the top surface (chip). However, because of the solder fatigue, this path is disturbed by an irregular discontinuity below the devices which consequently results in an irregular heat flow path. The effective attached area is thus not equal to the area estimated from SAM images. This effect is less obvious in the global case in Fig. 13 where data points follow the fitted curve more precisely. This is because the total area of the module is considered in the calculation and consequently the heat spreading effect is inherently taken into consideration which reduces the difference between the K-value and the squared estimated attached area from SAM images.

7. Conclusion

An evaluation of the use of the structure function as non-destructive testing tool for examining the integrity of the heat flow path in high power multi-chip semiconductor modules has been presented. A

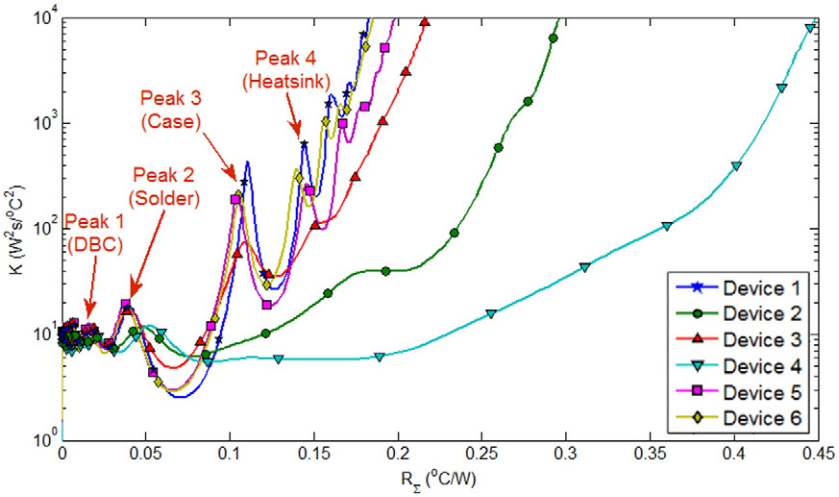

Fig. 18. The differential structure function of individual IGBT devices after 17,700 cycles.

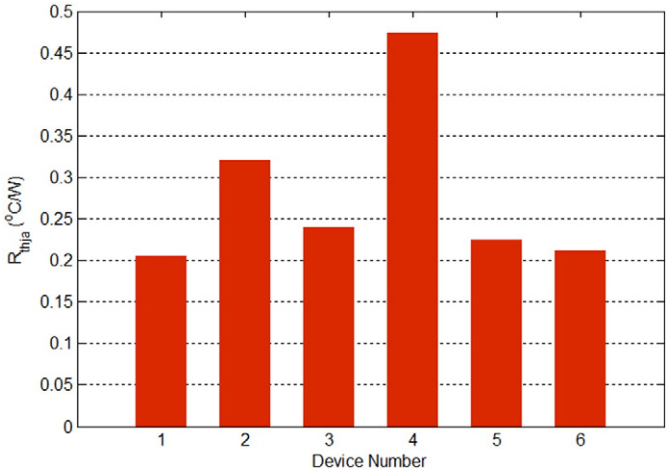

Fig. 19. The junction-to-ambient thermal resistance R_{thja} of the individual IGBTs after 17,700 cycles.

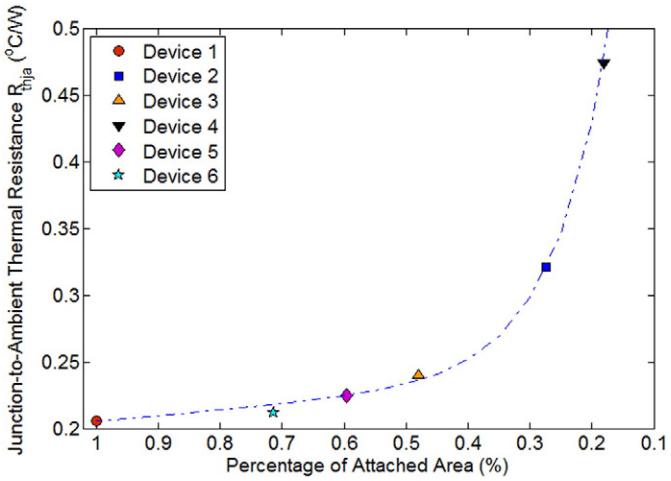

Fig. 20. The junction-to-ambient thermal resistance R_{thja} of the individual IGBTs after 17,700 cycles as a function of the attached area below each IGBT.

1.2 kV/200 A IGBT power module was power cycled to activate the solder fatigue failure mechanism at the substrate–baseplate interface. Thermal impedance measurements and SAM imaging were performed

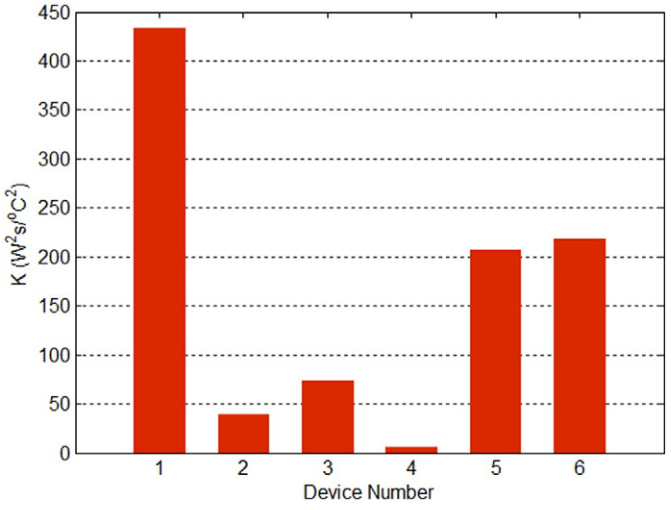

Fig. 21. The K-value of the case region of the individual IGBTs after 17,700 cycles. This value is indicative of the cross-sectional area below the IGBT.

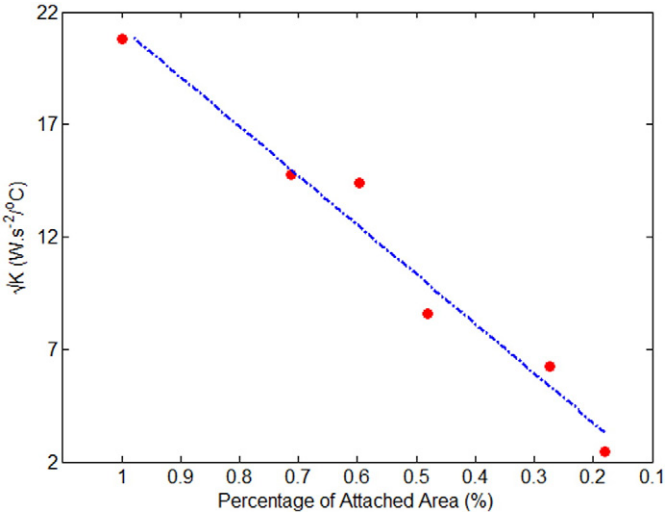

Fig. 22. The K-value as a function of the square of the fractional attached area of the individual IGBTs.

at regular intervals during the power cycling test. From this data, the thermal structure function was calculated and the cracked area in the solder layer was estimated. Failure analysis by cross-sectioning confirmed the location of the discontinuity at the substrate–baseplate solder layer.

A clear correlation was found between the change in the junction-to-case thermal resistance R_{thjc} estimated from the structure function and the remaining attached area of the solder layer calculated from the SAM images. It was shown that the K-value obtained from the differential structure function was linearly related to the square of the percentage of attached area estimated from SAM images. Similar results are found for the structure function calculated from the local measurement of the thermal impedances of individual IGBT devices.

The presented results reveal the capability of the structure function as a non-destructive evaluation tool of the heat flow path of high power multi-chip semiconductor packages. It can be used to estimate degradation in specific layers of the power module as a whole and also for individual devices. Consequently, it can be used as a primary inspection tool to rapidly test the integrity of the heat flow path in power modules before deciding whether further but potentially time-consuming, non-destructive (e.g. SAM scanning) or destructive analysis is required.

Acknowledgment

This work was supported by the Engineering and Physical Sciences Research Council (EPSRC) grant numbers EP/I031707/1 and EP/K034804/1.

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