Hybrid HVDC Circuit Breaker with Self-Powered Gate Drives

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Abstract: The ever increasing electric power demand and the advent of renewable energy sources have revived the interest in high-voltage direct current (HVDC) multi-terminal networks. However, the absence of a suitable circuit breaker or fault tolerant VSC station topologies with the required characteristics (such as operating speed) have, until recently, been an obstacle in the development of large scale multi-terminal networks for HVDC. This paper presents a hybrid HVDC circuit breaker concept which is capable of meeting the requirements of HVDC networks. Simulation results are presented which are validated by experimental results taken from a 2.5kV, 700A rated laboratory prototype.

1. Introduction

The interest in HVDC multi-terminal systems has been revived in recent years. The ever increasing demand for electric power and the advent of renewable energy sources such as off-shore wind power [1] – [3] and solar thermal generation in deserts [4] require an electric transmission system that bridges very long distances with low losses. Most of the HVDC lines realised so far have been point-to-point links [5]. Linking more than two HVDC terminals to form a meshed multi-terminal HVDC network would have several advantages which makes the realization of HVDC networks very attractive [6], [7]. The renewed interest in HVDC networks was initiated by the advances in HVDC technology, such as the availability of the voltage source converter (VSC) HVDC. However, the acceptance of HVDC networks with respect to efficiency, reliability, and controllability will strongly depend on the availability of HVDC circuit breakers and fault tolerant VSC topologies making them both important enabling technologies [8-11]. This paper focusses on a particular type of Hybrid DC circuit breaker with self-powered gate drives.

Compared with AC networks, DC current interruption is inherently difficult, mainly due to the absence of a natural current zero crossing in DC systems. Furthermore, DC circuit breakers are required to clear a fault very quickly, typically within a few milliseconds, and to dissipate the large amount of energy which is stored in the system inductances [5]. Commercially existing high voltage DC switches have operating times of several tens of milliseconds, which although suitable for load current switching, is too slow for clearing faults to meet the needs of a reliable HVDC network [12]. Therefore, new technologies for fast and reliable HVDC circuit breakers are required.

A purely solid-state circuit breaker for HVDC networks was proposed and patented in 1997 [13]. Although a very fast response time can be achieved, this arrangement cannot be considered as a practical solution, due to the high steady-state losses which are dissipated in the high voltage switching branch. In 2011, a hybrid circuit breaker solution was demonstrated at CIGRE, Bologna [12]. This topology can be considered as an updated version of that considered in [13], i.e. a low voltage (LV) branch consisting of ultra-fast mechanical switch and an insulated gate bipolar transistor (IGBT) is introduced to carry the nominal current and thus avoid the high steady-state losses. The solution presented however, does not have self- powered gate drives for the auxiliary arm. This would be advantageous since powering such circuits in HVDC systems is a well-known challenge. Other solutions have also been proposed in this highly active research area [14-17].

This paper presents an alternative hybrid HVDC circuit breaker topology based on [16]. This topology has a fast response time, thus enabling its use with state of the art switching hardware and furthermore it utilises self-powered gate drives in the high voltage branch, thus eliminating the need for external gate power supplies for the circuit breaker.

 Simulation results, using PLECS software, are presented and validated using experimental results taken from a 2.5kV, 700A rated laboratory prototype.

## 2. Principles of hybrid circuit breakers

A circuit breaker (CB) is required to accomplish the following basic requirements: 1) large current handling capability without excessive losses; 2) capability of very fast transition from the conducting to the blocking state in case of a fault, without damaging itself in the process; and 3) after current interruption, when it is open, the dielectric strength must be built up in order to block any current despite the high potentials at the terminals [18-24]. Traditional mechanical circuit breakers (MCBs) have a very small contact resistance in the closed position, with galvanic separation in the open state. However, they have a long reaction time due to the need to extinguish the fault in an arc chute [18-22].

Solid–state circuit breakers (SSCBs), based on high-power semiconductors, offer many advantages when compared to conventional solutions. In SSCBs, due to the absence of moving parts, there is no arcing, contact erosion, or bounce. SSCBs are therefore faster, minimizing fault duration. However, because of the semiconductor's on-state resistance resulting in heating and power loss, the SSCBs fail as far as the first basic requirement of a CB mentioned above is concerned.

Since a SSCB (MCB) can still perform admirably for one of these requirements where an MCB (SSCB) fails, a parallel combination of semiconductor(s) and an MCB can combine the advantages of both, resulting in a hybrid circuit breaker. A hybrid circuit breaker allows a combination of the MCB's current-carrying function and SSCB's high-speed arc-less interrupting function. This concept of a hybrid DC circuit breaker is shown in Fig.1a., where the parallel combination of a semiconductor and mechanical breaker branch is clear.
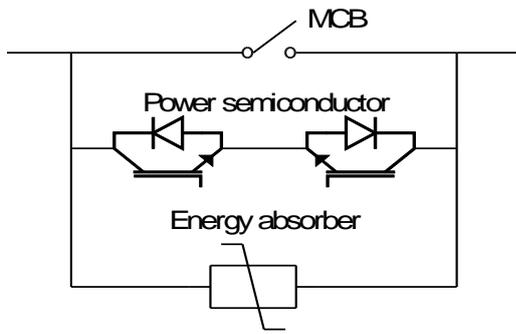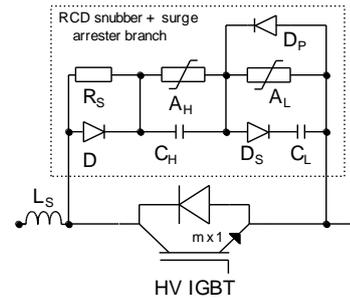
Fig.1a. *DC hybrid circuit breaker*
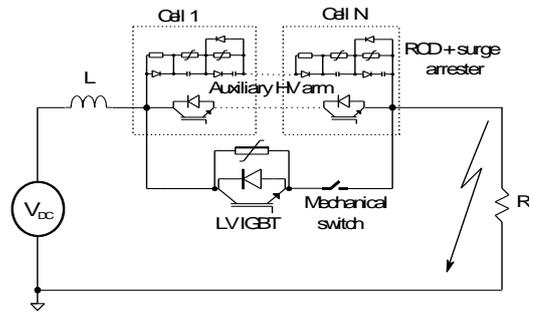
Fig.1b. *The proposed hybrid HVDC circuit breaker concept*
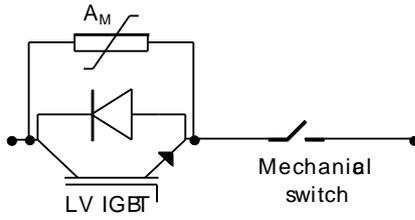
Fig.1c. *Detailed structure of unidirectional main branch*

Fig.1d. *Snubber circuit and surge arrester branch*

The normal current flows through the main contact for low power dissipation. The semiconductor device connected in parallel to the main contact operates after a fault occurrence and performs the fault current interruption. It is to be noted that as the semiconductor device is turned off to finally clear the fault, the voltage across it rises due to the stored energy in the line inductance. This voltage may reach a very high value and destroy the hybrid circuit breaker if no additional components are used for reducing the voltage. As shown in Fig. 1a, an overvoltage protection device is connected in parallel to the semiconductor device to reduce the peak voltage. Therefore, by limiting the voltage magnitude during turn-off, the energy absorber protects the hybrid circuit breaker from damage and also dissipates the energy stored in the line inductance to reduce the current to zero.

3. The proposed hybrid HVDC circuit breaker

Figure 1b shows the proposed hybrid HVDC circuit breaker in an HVDC grid, where L represents a DC reactor, the value of which should be chosen to give the desired rate of rise of fault current; V_{DC} and R are the voltage and equivalent load resistance of the grid, respectively.

The hybrid circuit breaker consists of three main sections: main low voltage (LV) branch, auxiliary high voltage (HV) branch and extinguishing RCD snubber plus surge arrester branch. A brief description of each part is given in the following subsections. Considering a 120kV HVDC system, Table 1 gives a typical specification for the proposed hybrid HVDC circuit breaker [25].

Table 1 Specification for proposed hybrid HVDC circuit breaker [25]

Symbol	Description	Value
V_{DC}	HVDC supply voltage	120kV
I_{DC}	HVDC load current	1.5kA
v	Rate of rise of fault current	10kA/ms
I_{TH}	Fault threshold level	2kA
I_{MAX}	Maximum breaking current	7.5kA

3.1. Main branch

The main LV switching branch consists of a semiconductor based commutating switch, e.g. an IGBT, and an ultra-fast mechanical switch. A surge arrester A_M is employed in parallel with the commutating IGBT, in order to provide a bypass at the beginning of a fault current commutation. Figure 1c shows the detailed structure of the main branch for unidirectional current flow. The arrangement of the mechanical switch may vary depending on the voltage and switching requirements of the system.

Recent publications indicate that contact opening times for mechanical switches are in the region of 2ms and that this is likely to be improved in the future [12-17,23]. In this paper, it is assumed that the mechanical switch takes 500µs to operate and a further 300µs for the contacts to open and support full voltage. These values are based on extrapolation of current state of the art mechanical switch capabilities to the near future. Based on this capability, the shape of the transient recovery voltage produced by the HV surge arrester string can be profiled to be a gentle ramp rather than a steep voltage ramp as in the usual approach, in order to fully utilise the capability of the mechanical switch. Using such a gentle voltage ramp, i.e. voltage rising from zero to its target level from the time range 500-800µs, brings a significantly lower peak current seen by the HV IGBTs and less energy dissipated by the HV surge arresters.

The commutating LV IGBT switch is used to commutate the fault current from the main branch to the auxiliary HV switching branch when a fault occurs, in order to reserve a sufficient time (i.e. at least 500µs) for an actuator to open the mechanical switch. During normal operation, the current flows only through the main branch, resulting in a relatively low on-state voltage. Therefore, the issue of high steady-state losses, normally associated with solid state devices in the main current path is successfully overcome. When a fault occurs, the LV commutating switch is turned off and the current commutates to the auxiliary HV branch (assuming it is gated at the appropriate time). When the main LV branch is no longer carrying current, the mechanical switch opens, thus protecting the LV switch from the voltage that builds up across the auxiliary branch. The required voltage rating of the LV switch is thus significantly reduced in comparison to a component that remains in the main current path throughout the switching cycle. Its voltage rating is dictated by the clamping voltage of the parallel-connected surge arrester. Considering the nominal load current level, a suitably rated single or a number of parallel IGBTs can be used to construct the LV commutating switch.

The surge arrester, A_M, is used to clamp the voltage across the commutating switch at a safe level, it also generates a driving voltage for the current pulse required for the "self-powered" gate drive circuits of the auxiliary branch.

3.2. Auxiliary branch

When a fault is detected in the HVDC grid, the fault current is transferred from the main LV branch to the auxiliary HV branch. After the fault current has been successfully transferred the fast mechanical switch is opened and the cells of the auxiliary branch are turned off to allow the HV surge arresters to extinguish the current.

The counter voltage produced by the HV surge arrester is typically 1.5 times the supply voltage. To withstand it, a large number of HV switch modules need to be connected in series. For a self-powered implementation, it is preferable to use only one series IGBT switch in each module. Hence, considering a 3.3kV, 1.2kA IGBT switch and additional 30% headroom, the number of auxiliary modules for each circuit breaker, n, can be calculated by (1).

$$n = \frac{1.5*120kV}{0.7*3.3kV} = 80 \qquad\qquad (1)$$

Although a large reactor L is employed to limit the rise rate of the fault current, the peak current endured by the auxiliary branch is still quite high, i.e. 7.5kA. To carry this current safely, a suitably rated IGBT or parallel connection of IGBTs is required. An extensive cooling system is not required, since the current will only flow through the auxiliary branch under fault conditions.

3.3. Extinguishing branch

Each cell of the HV auxiliary branch is connected in parallel with a capacitive snubber and surge arrester arrangement as shown in Fig. 1d where L_S represents a lumped stray inductance of the circuit; R_S is a discharge resistor of the RCD snubber; A_H, A_L, C_H and C_L represent a high voltage surge arrester, low

voltage surge arrester, high voltage capacitor and low voltage capacitor, respectively. The energy stored in C_L is used to gate the devices of the associated HV auxiliary module.
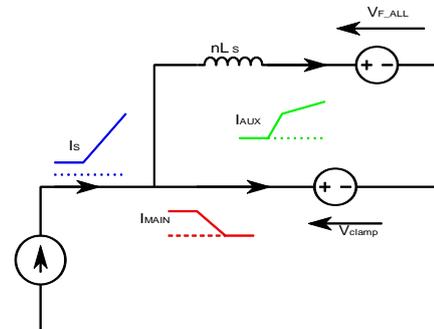
3.3.1 HV surge arrester A_H: The high voltage arrester, A_H, is responsible for producing the counter voltage which in combination will reduce the fault current to zero. Considering the system requirement and total auxiliary module number, the rating of each A_H can be determined.

3.3.2 LV surge arrester A_L: The low voltage arrester, A_L, is used to limit the voltage across C_L at a safe level to drive low voltage level electronics. The low voltage limb (including C_L and A_L) in each cell provides a means of powering the gate drive circuitry of the HV IGBTs. This eliminates the need to continuously power the control unit of the auxiliary HV branch.

3.3.3 Stray inductance L_S: When the auxiliary HV branch is switched on, the fault current starts to commutate to it. Once the current is fully transferred, the mechanical switch is turned off at zero current with low voltage stress. Figure 2a shows the theoretical current waveform of the circuit breaker during the commutation event, where I_{MAIN} and I_{AUX} represent the main branch and auxiliary branch currents, respectively. I_{COM_1} and I_{COM_2} represent the initial and post commutation currents.
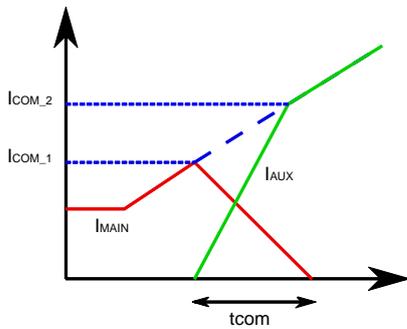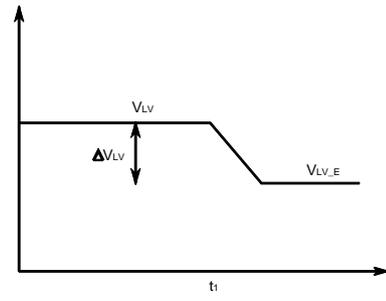

Fig.2a. Theoretical current waveform during commutation   *Fig.2b. Equivalent circuit for the commutation analysis*
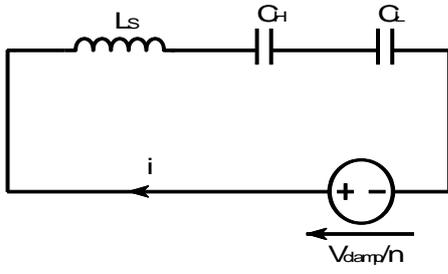
Fig.2c. *Equivalent charging circuit of each module*

Fig2d. *Assumed voltage waveform of the LV capacitor during IGBTs turn-on process*

The initial commutation current is given by (2), where I_{TH} and v are the threshold level of fault detection and the rate of rise of fault current, respectively, as given in Table 1; $t_{CHARGING}$ is the charging time of the LV capacitors (the duration after fault detection before the auxiliary branch is gated on).

$$I_{COM\_1} = I_{TH} + t_{CHARGING} * v \qquad (2)$$

Figure 2b shows an equivalent circuit used for the commutation analysis, where V_{clamp} is the clamping voltage of the main branch (i.e. 2.5kV); nL_S is the lumped stray inductance of the n auxiliary modules; V_{F_ALL} is the lumped forward voltage of all the HV IGBTs.

From [26], the forward voltage of the selected HV IGBT is taken as 2.8V. Considering a 20μs charging time and a total of 80 auxiliary modules, the current commutation time and the post commutation current can be calculated by (3) and (4).

$$t_{COM} = \frac{I_{COM\_1}}{\frac{V_{clamp} - V_{F\_ALL}}{n * L_S} - v} \qquad (3)$$

$$I_{COM\_2} = I_{COM\_1} + t_{COM} * v \qquad (4)$$

A large stray inductance results in a long commutation time and thus a high post commutation current. As a result, the time left for opening the mechanical switch is reduced accordingly. It may be even shorter than the minimum requirement (800μs) for opening the mechanical switch when the fault current reaches the maximum breaking threshold (7.5kA). To reserve sufficient time for an actuator to open the

mechanical switch, a relatively short commutation time is required. This provides an upper limit for the allowable stray inductance of each auxiliary module. Due to the large number of modules required, the effect of the IGBT forward voltage drop on the commutation time should be taken into account (2.8Vx80=224V).

Based on these considerations, the stray inductance L_S for each auxiliary module is taken to be 0.5µH. This is a conservative design (i.e. is readily achievable in practice), and the value is sufficiently large to highlight its influence in the simulation results.

3.3.4 RCD snubber: Diodes D_S and D_P ensure that the energy stored in capacitor C_L is protected and reserved for further switching (re-closing) actions. Such an event may be required if the fault has not been cleared. The state of the transmission line can be checked by re-triggering the entire auxiliary arm IGBTs. A faulted line would then be opened again; a safe transmission line would have conduction passed back to the main branch before turning the auxiliary branch off. The selection of R_S is only determined by the peak discharging current endured by the HV IGBT, which occurs at the re-closing event, given by (5).

$$I_{peak} = \frac{V_{DC}}{nR_S} \qquad (5)$$

The aim of employing the low voltage limb (including C_L and A_L) in each auxiliary module is to provide a means of powering the gate drive circuitry. This obviates the need to continuously power the control unit of the auxiliary HV switching branch with obvious implications for cost reduction.

Initially, when the 2kA threshold level is triggered, the LV IGBT switch of the main branch is switched off. Hence, the current flows through the surge arrester A_M as a bypass, creating a charging voltage for each capacitor in the auxiliary branch. Considering one auxiliary module, an equivalent charging circuit can be drawn as shown in Fig. 2c, where V_{clamp}/n is the effective charging voltage; L_S represents the lumped stray module inductance; C_H and C_L are the HV and LV capacitors, respectively.

Once C_L is charged, the energy stored in it is used to turn on the associated auxiliary HV switching module (i.e. to provide power to the gate drive and associated circuitry). As each auxiliary module may

contain a number of IGBTs in parallel, C_L must provide enough charge to gate all of these devices. Figure 2d shows the voltage waveform assumed on the LV capacitor C_L during the IGBTs turn on process (the charge is assumed to be taken from the capacitor at a constant current during the turn-on time). After providing the required gate charge, the voltage across C_L, V_{LV}, drops to voltage V_{LV_E} (which must be high enough to assure proper turn-on and correct operation of the associated electronic circuitry).

The C_H and C_L capacitors are designed by considering the resonant circuit formed by the capacitors and the stray inductance, L_S, shown in Fig.2c. Since C_L needs to be quickly charged to enable a fast response time of the auxiliary branch to the occurrence of a fault, the impedance of C_H can be set much smaller than that of C_L.

With the aim of achieving a compact system volume, the relationship between the two capacitors is further analysed to find the minimum value of the HV capacitor. Assuming the break down voltage of the LV arrester is relatively large, i.e. the LV capacitor voltage will not be clamped during the charging event, then the prospective voltage across the two capacitors is given by (6) and (7).

$$V_P = V_{LV} + V_{HV} = 2V_{clamp}/n \qquad (6)$$

$$V_{HV}C_H = V_{LV}C_L \qquad (7)$$

Considering the gate charge requirement, Q, the voltage across the LV capacitor, V_{LV}, drops to the end point voltage V_{LV_E} (i.e. $\geq 15V$) after the IGBT turn-on process.

$$V_{LV\_E} = V_{LV} - \Delta V_{LV} = V_{LV} - \frac{Q}{C_L} \qquad (8)$$

From (6) to (8), the relationship between the two capacitors can be derived as (9).

$$C_H = \frac{C_L{}^2 V_{LV\_E} + QC_L}{(V_P - V_{LV\_E})C_L - Q} \qquad (9)$$

As both C_L and C_H must be positive, the minimum of C_L can be found,

$$C_{L\_MIN} = \frac{Q}{V_P - V_{LV\_E}} \qquad (10)$$

Taking the derivative of C_H with respect to C_L (9), the corresponding value of C_L that yields the minimum value for C_H is given by

$$C_{L\_COR} = \frac{Q}{V_P - V_{LV\_E}}(1 + \sqrt{\frac{V_P}{V_{LV\_E}}}) \qquad (11)$$

Substituting (11) into (9) yields,

$$C_{H\_MIN} = \frac{QV_P}{(V_P - V_{LV\_E})^2} \cdot (1 + \sqrt{\frac{V_{LV\_E}}{V_P}})^2 \qquad (12)$$

To reserve some charge for associated logic gate circuits and in this case assuming four parallel connected IGBTs, a charge of Q equal to 240µC is considered [26]. The corresponding C_H and C_L are obtained by solving (11) and (12), which yields approximately 15µF for both. Table 2 summarises the design results for each auxiliary module. The charging time of the LV capacitor can also be found,

$$t_{CHARGING} = \frac{2\pi\sqrt{L_S C_L}}{2} = 8.6\mu s. \qquad (13)$$

Table 2 Design results of auxiliary module

Symbol	Description	Value
L_S	Lumped stray inductance	0.5µH
R_S	Discharge resistor	1Ω
C_H	High voltage capacitor	15µF
C_L	Low voltage capacitor	15µF
V_{LV}	Voltage after charging	31.25V
ΔV_{LV}	Voltage drop of one	8V

	switching action	
V_{HV_CLAMP}	Clamping voltage of	2.25kV
	HV surge arrester	
V_{LV_CLAMP}	Clamping voltage of	55V
	LV surge arrester	

4. Simulation results

Figure 3a shows the schematic used to simulate the breaking of fault current by the proposed hybrid HVDC circuit breaker. An ideal switch (i.e. Fault Switch) emulates a short circuit fault or an open circuit condition according to the control order received.
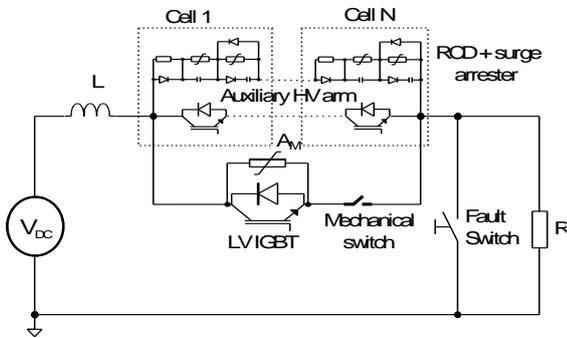

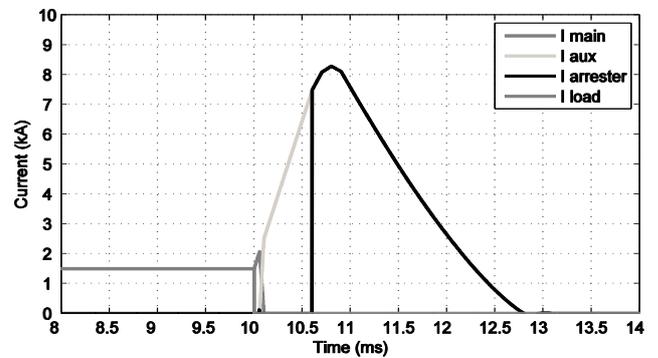*Fig.3a. Hybrid breaker performing current breaking action*

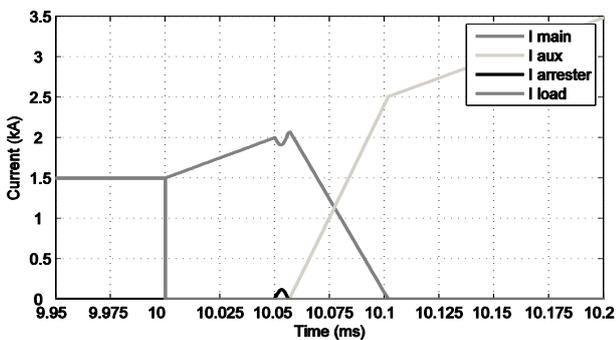*Fig3b. Current waveforms of the circuit breaker*

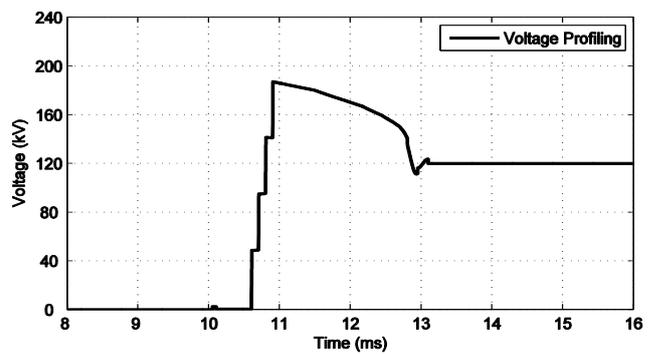*Fig.3c. Zoomed Current waveforms of the circuit breaker*

Fig.3d. Voltage profiling of the circuit breaker

During normal operation, the LV IGBT and mechanical switch are closed, thereby supplying current to the load, R. A fault is created by closing the Fault Switch. When a fault threshold is reached, the LV

commutating IGBT is turned off. This causes the current to flow through the arrester, A_M, as a bypass. The current pulse generated by A_M is used to charge the two capacitors of each cell. The energy stored in C_L is then used for turning on the HV IGBT in the auxiliary branch. Once the auxiliary branch is turned on, the current is fully commutated to it in a time determined by the value of the stray inductance. The mechanical switch is then turned off at zero current. When the mechanical switch is fully off, the HV IGBTs are turned off to commutate the current to the extinguishing branch, which reduces the current to zero.

Figures 3b and 3c show the current waveforms when the circuit breaker performs a fault current breaking action, where the curves represent the current through the main branch, the current through the auxiliary HV switch branch, the current through the extinguishing branch and the load side current. A fault occurs at a simulation time of 10ms, and the current starts to build up at the rate of 10kA/ms. Once the threshold of 2kA is met, the LV commutating IGBT is turned off. Therefore, the fault current flows through the surge arrester A_M, and the two capacitors of each snubber circuit are charged by a current pulse. Once the auxiliary HV branch is turned on (after the LV capacitor is charged), the fault current is fully commutated to it in about 50μs, and the mechanical switch can then be opened at zero current with low voltage stress. After 500μs, the 80 auxiliary modules are turned off sequentially, in order to commutate the fault current into the extinguishing branch. As a result, the high voltage surge arrester string forces the fault current to reduce to zero. The total fault clearing time is about 2.75ms.

Figure 3d shows the corresponding voltage across the circuit breaker during this fault clearing event. The total 80 auxiliary modules have been further divided into 4 groups. When the mechanical switch contacts begin to open these 4 groups are sequentially switched off within 300μs. Therefore, a step-like voltage ramp is applied, which brings a significantly lower peak current seen by the HV IGBTs and less energy dissipated by the HV arresters.

Figure 4 shows the detailed voltage waveform of one auxiliary module, where curves represent the voltage across the auxiliary module, the voltage across C_H, the voltage across C_L and the voltage across the

snubber diode D. Figures 4b and 4c show the zoomed-in details indicating that the voltage across C_L remains constant so we can use it for switching on the auxiliary arm cells.
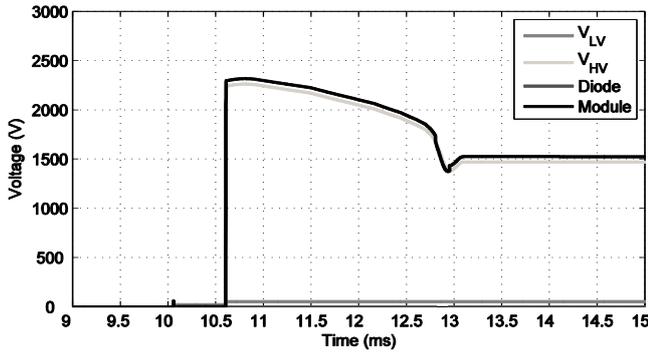

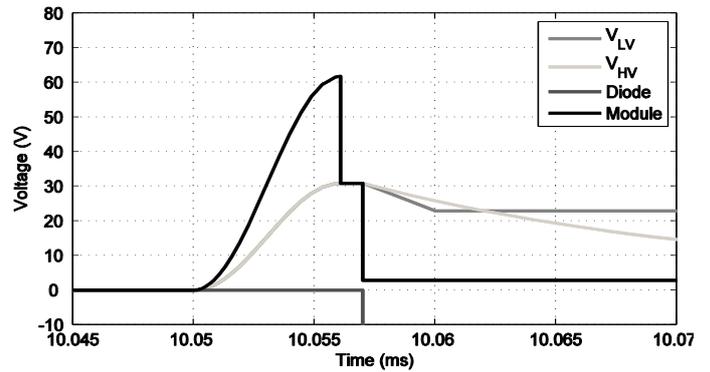*Fig.4a. Voltage waveforms of one auxiliary module*
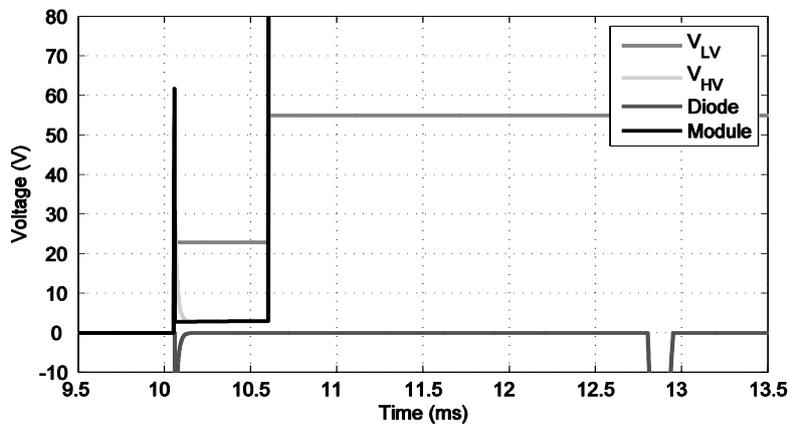

Fig.4b. Zoomed-in detail A

Fig.4c. Zoomed-in detail B

As shown in figure 4b, when the extinguishing branch sees the current pulse, the two capacitors are charged to 31V quickly, due to their identical capacitance. The energy stored in each C_L is used to turn on associated auxiliary HV switches. A 3μs, 40A current pulse has been employed to represent the IGBT gate charge which results in an 8V voltage droop on the LV capacitor voltage. Once the auxiliary HV switches are turned on, the voltage across each module drops to 3V (i.e. the IGBT forward voltage), and the HV capacitor C_H is quickly depleted. Owing to the series diode Ds, C_L is protected from being discharged, allowing for a re-triggering operation, if required.

At a simulation time of 10.6ms, as shown in figure 4c, the HV IGBTs are turned off (staggered as discussed above). The fault current is then commutated to the associated RCD snubber plus surge arrester branch. C_L is quickly charged and the voltage across it is clamped at 55V by A_L, while the HV capacitor C_H is charged to the breakdown level of A_H. When the voltage produced by the circuit breaker equals the supply voltage 120kV, the fault current reaches its peak (i.e. at time 10.8ms).

The counter voltage produced by the surge arrester string is 1.5 times the supply voltage V_{DC} (at the peak current) and forces the fault current to reduce to zero. When the fault current is cleared, the voltage across each module is 1.5kV (i.e. 1.5kVx80=V_{DC}). Each C_L is protected from discharge by the associated D_S and D_P.

Figure 5a shows the total energy dissipation of the HV surge arrester during the current breaking action. Figure 5b compares the energy absorption of each auxiliary module in the different groups.
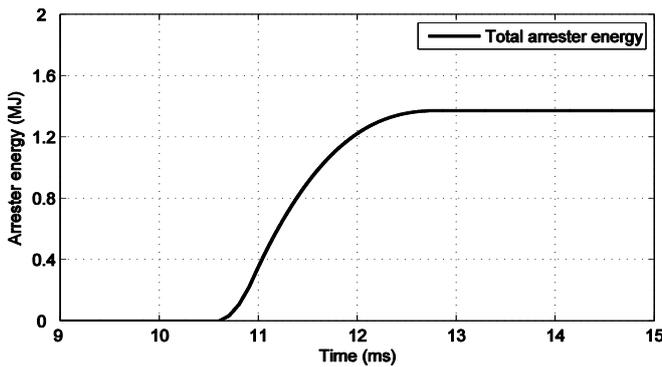
Fig. 5a. *Total energy absorption by HV surge arrester string*
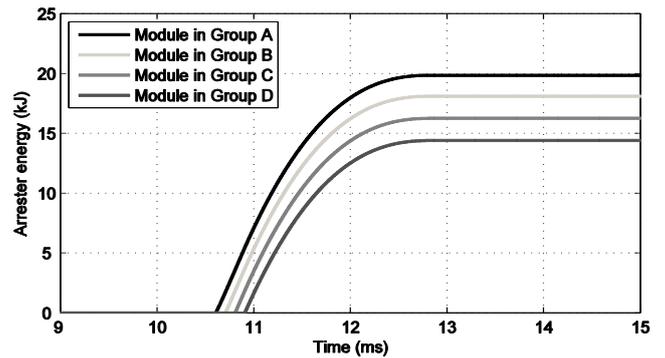
Fig.5b. *Energy absorption of each module in different groups*

When the mechanical switch is initially open, the 20 auxiliary modules of Group A are first turned off. Following that, the modules of Group B, C and D are sequentially switched off after every 100μs. Consequently, the HV surge arresters of Group A consume the maximum energy and that of Group D the least.

5. Validation of the proposed hybrid HVDC circuit breaker

A scaled-down laboratory prototype of the proposed hybrid HVDC circuit breaker was used to validate the simulation results. The basic test set-up is as shown in Fig.6a. For simplicity and ease of implementation, a series connection of five HV cells was used for the auxiliary branch, with each HV auxiliary cell using a single IGBT.

Operation of the circuit is as follows. A capacitor bank is charged to the operating voltage (V_{DC}) from a rectifier source. Following isolation of the source from the capacitor bank, a semiconductor switch is used to emulate a fault and current rises in the main branch (which is already gated on) limited by the inductor. When the threshold current is detected, the LV IGBT of the main branch is turned off. Hence, the fault current flows through the surge arrester, A_M, as a bypass resulting in a charging voltage to charge the capacitors C_L and C_H of each cell. A summary of the parameters used for the experimental validation is given in Table 3.

The LV switching device is implemented using a 3.3kV/1.2kA IGBT from Dynex Semiconductor Ltd.. A similar device is used to emulate the operation of the ultra-fast mechanical switch. An auxiliary arm comprising five HV IGBTs rated at 1.7kV, 800A is used to demonstrate the capabilities of the hybrid HVDC circuit breaker. A PCB was used to interface the HV IGBTs with surge arresters and RCD snubber circuit as shown in Fig.6b.

A self-powered gate drive (SPGD) has been designed using a complete discrete device based solution. In contrast with the standard gate drive, the SPGD has no externally derived power supply but relies on the energy stored locally on the LV capacitor to turn the auxiliary branch HV IGBTs on and off. Figure 6c shows the circuit diagram of the SPGD used in this work. As discussed before, when the main branch LV IGBT is turned off, a current pulse quickly charges the LV capacitor to about 25V. During the charging period, the voltage on the LV capacitor is monitored and the status sent to the controller. As soon

as the voltage requirement is achieved, the controller sends an acknowledgment signal to the circuit to gate the IGBT. A push-pull arrangement is used to achieve the required current gain to drive the IGBT.

Fig.6a. Test rig outline

Fig.6b. Auxiliary branch module

Fig.6c. Self-powered gate drive circuit

Table 3 Parameters used for validation

Symbol	Description	Value
V_{DC}	DC supply voltage	2.5kV
L	DC inductor	2.5mH
C_{BANK}	Capacitor bank	2mF

|		
I_{BREAK}	Breaking current	600A
C_L	LV capacitor	15μF
C_H	HV capacitor	15μF
A_{AUX}	Auxiliary arm surge arrestors in cells 1-5	EPCOS 340V, 595V, 1025V, 1025V, 1025V

6. Experimental results

Experimental results are presented in this section to validate the operation of the proposed hybrid HVDC circuit breaker. A capacitor bank is charged to the operating voltage (2.5kV) from a source. Following the isolation of the source from the capacitor bank, the fault switch is engaged and current rises in the main branch (which is already gated on). When the threshold for fault current is detected (200A in this case), the LV IGBT of the main branch is turned off, while the auxiliary branch remains off. Hence, the fault current flows through the surge arrester A_M as a bypass resulting in a charging voltage for the C_L and C_H capacitors in the auxiliary arm. The charging time is approximately 20μs - 30μs representing a half cycle of the resonant period created by the series combination of the two 15μF capacitors and the loop inductance (about 5μH). No additional inductance was used, since the inherent stray inductance in the construction was adequate. Clearly, in a circuit breaker built at full voltage the self-inductance created by the valve layout would likely be large enough that no inductance would need to be added- care must be taken to limit the inductance, however, since it affects the commutation time from the main branch onto the auxiliary branch.

Once C_L is charged to around 20V, the energy stored in it is used to turn on the associated HV IGBT. After turning on the IGBTs the fault current commutates from the main branch to the auxiliary branch in approximately 20μs. The commutation time is dictated by the current at the point of commutation (about 300A), the loop inductance (5μH) and the clamping voltage of the LV switch (165V) giving a theoretical value of (600x5/165 = 18μs) which agrees well with the observations.

Figure 7a shows the current through the main branch, auxiliary branch and the voltage across the LV capacitor during the current build-up, resonant charging, current commutation and breaking periods. A detailed view of the current build-up, resonant charging and current commutation events is shown in Fig. 7b. It should be noted that the spikes and notches in the LV capacitor voltage waveform are a result of the high dv/dt and changes in common mode voltage which cannot be rejected by the differential probe used. The results in Figs. 7a and 7b are consistent with those shown in Fig. 3b and 3c, and therefore validate these simulation results.
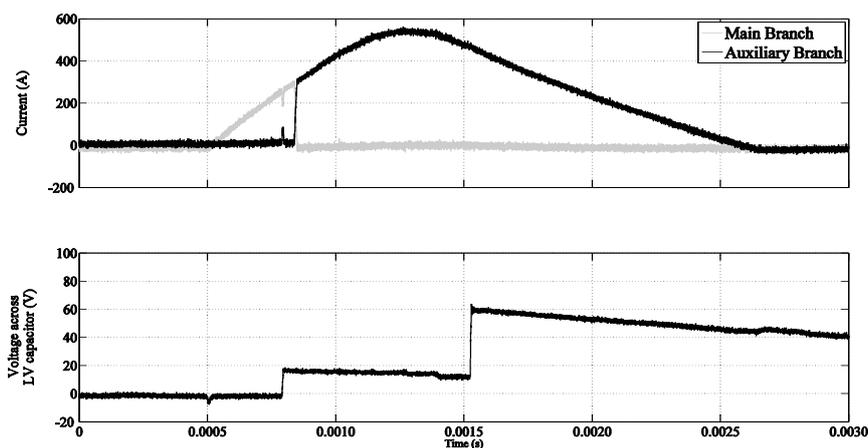
Fig.7a. Experimental main branch and auxiliary branch currents and LV capacitor voltage
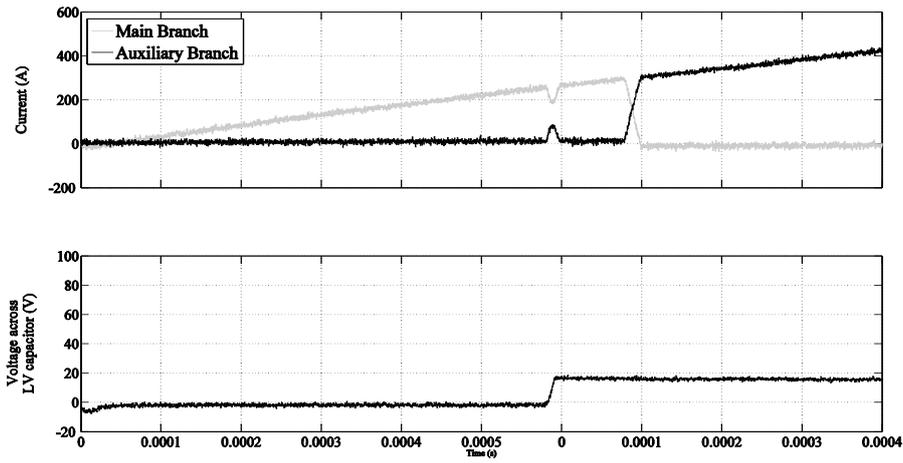
Fig.7b. *Zoomed-in detail of main branch current, auxiliary branch current and LV capacitor voltage*
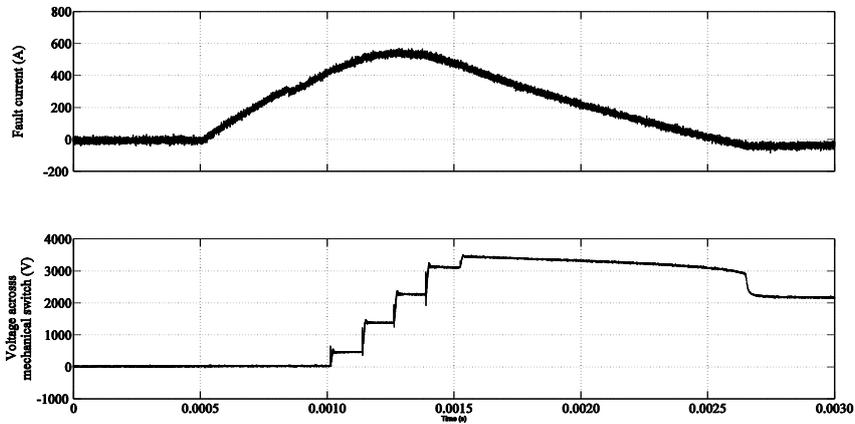
Fig.7c. *Experimental reactor current and mechanical switch voltage*

The fault current through the DC reactor and voltage seen by the mechanical switch during the fault clearing event are shown in Fig.7c. Five cells were used for the auxiliary branch. When the mechanical switch is ready, these five cells are switched off within 400μs, i.e. 100μs delay between each other. Thus, a step-like voltage ramp is applied as shown in the lower plot of Fig. 7c.

Figure 8 shows the relevant waveforms of the complete hybrid HVDC circuit breaker. These include the currents through the main and auxiliary branches, the voltages across the mechanical switch and DC reactor and the voltage across C_L and SPGD demand voltage.
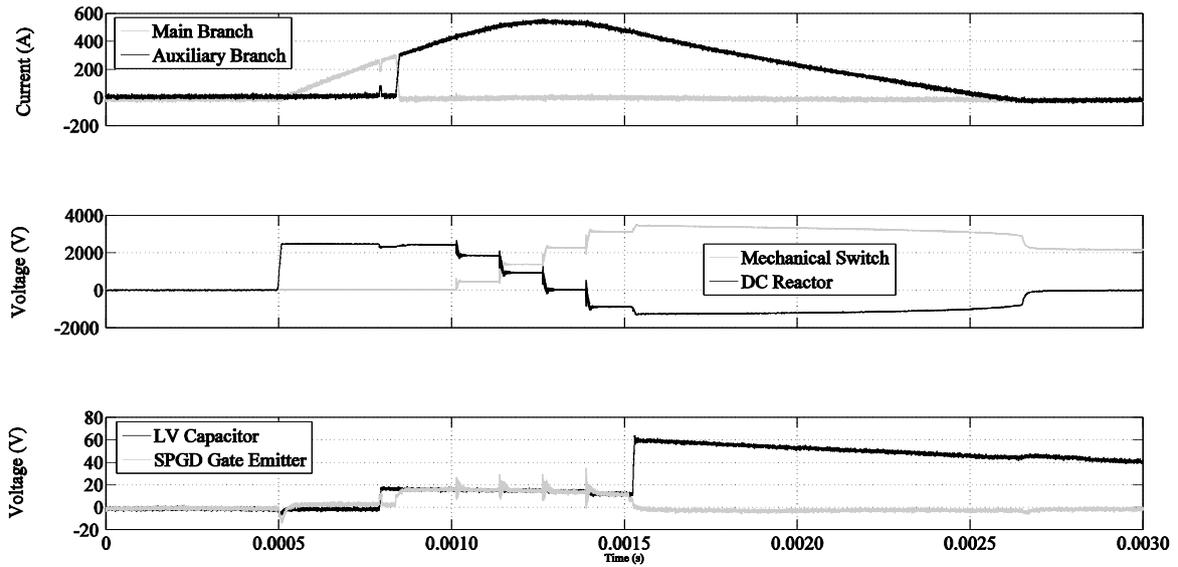
Fig.8. *Complete experimental waveforms*

7. Conclusion

This paper has presented a novel hybrid HVDC circuit breaker with self-powered gate drives. This circuit breaker has a very fast response in breaking fault currents. The auxiliary HV branch switches are gated by using energy stored in the LV capacitors thereby eliminating the need to continuously power the gate drive circuitry of this branch. The operation of the hybrid breaker has been shown through simulations and validated with experimental results taken from a 2.5kV, 700A rated scaled down laboratory prototype. Extension of the design for system voltages and currents can be readily achieved by adding more cells in series and parallel to meet the voltage and current requirements respectively. It should be noted that the clearing time of the proposed technique is strongly affected by the switching time of the disconnector switch and the current state of the art has switching speeds of around 2ms. The reliability of such a device is subject to further work and it is likely that a crowbar system would be used to bypass faulty cells [16].

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