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Performance Evaluation of a 3-Level ANPC Photovoltaic Grid-Connected Inverter with 650V SiC Devices and Optimized PWM

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***Abstract*—Photovoltaic (PV) energy conversion has been on the spotlight of scientific research on renewable energy for several years. In recent years the bulk of the research on PV has focused on transformerless grid-connected inverters, more efficient than traditional line transformer-based ones, but more critical from a power quality point of view, especially in terms of ground leakage current. Neutral point clamped (NPC) inverters have recently gained interest due to their intrinsically low ground leakage current and high efficiency, especially for MOSFET-based topologies. This paper presents an active NPC (ANPC) topology equipped with 650 V SiC MOSFETs, with a new modulation strategy that allows to reap the benefits of the wide-bandgap devices. An efficiency improvement is obtained due to the parallel operation of two devices during the freewheeling intervals. Simulations and experimental results confirm the effectiveness of the proposed converter.**

I. Introduction

In recent years, an increment of production from renewable resources was registered in the energy mixes of several countries. Among renewables, the photovoltaic (PV) represents one of the most mature technologies. One of the major characteristics favoring PV over other renewable resources is the possibility to be employed in low power plants, easily integrated in the environment and directly connected to the low voltage distribution line. Many types of single-phase PV inverters were developed, both in industry and in academia [1]–[5]. Transformerless inverters are those that can achieve the highest efficiency levels, but their use in grid-connected systems is not straightforward.

In fact, due to the absence of galvanic isolation, undesired phenomena, such as ground leakage currents, can arise in transformerless plants [6]. Different architectures of inverters that address this issue were presented in literature; therefore transformerless inverters can be subdivided in two major families: full-bridge based and half-bridged based topologies [7]. The latter have the disadvantage of needing twice the value of the DC source voltage respect to the full-bridge based family, but, on the other hand, may achieve better performance in terms of ground leakage current rejection. The Neutral Point Clamped (NPC) converter architecture belongs to the family of half-bridge/based converters¡ it was first proposed in [8] for three-phase systems, but has been largely studied also for PV single-phase transformerless applications.

The structure of a single-phase NPC converter is shown in Fig. 1(a)). It relies on 4 switches and 2 diodes, synthesizing a three-level output voltage waveform. In [9] the diodes were replaced by power switches, realizing the so-called Active Neutral Point Clamped converter, ANPC (Fig. 1(b)). Three-level ANPC claims better loss distribution and equal stress across the devices in comparison to conventional three-level NPC. Several PWM patterns and architectural variations were proposed for ANPC converters. In [10] an auxiliary circuit was added to the NPC structure to achieve soft switching commutation. A modulation technique was proposed in [11] for doubling the apparent switching frequency of the output voltage. A feedback controlled loss balancing system has been proposed for ANPC converters in [12]. In this case an online estimation of the devices' junction temperature was used to select the appropriate switching technique for reducing the switching stress of the hottest devices.

Moreover, in [13] the authors introduced the concept of the stacked neutral point clamped (SNPC) converter, in which an additional branch, constituted by two anti-series devices, is inserted between the converter output and the mid-point of the DC source (Fig. 2(a)). The concept was enhanced in [14], enabling a better loss distribution by substituting diodes with power switches (active SNPC, ASNPC) (Fig. 2(b)). In [15] a high-efficiency three-level SNPC architecture, using hybrid CoolMos and IGBT power modules, was proposed and applied to nonisolated grid-tied PV converters.

All the solutions above were limited to the use of silicon devices, and were optimized for IGBTs as well as for MOSFETs. In the latter case the modulations were optimized to avoid the conduction of the antiparallel MOSFET body diodes, therefore the active rectification capabilities of the MOSFETs was not yet exploited.

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This paper proposes an improved modulation to exploit the emerging silicon carbide devices. In order to take advantage of the low conduction losses and resistive on-state characteristic of the MOSFETs, the parallel conduction of the MOSFETs will be used during the freewheeling phases of the output current. This can be achieved employing silicon carbide (SiC) instead of silicon devices. SiC MOFETS have negligible antiparallel diode reverse recovery time, therefore the diodes can effectively carry the current during the dead time intervals.

A version of this paper was presented at the ECCE 2014 conference [16]. The paper has been extended and improved, and an extensive power loss analysis has been added.

II. State of the Art and Proposed High-Efficiency PWM Strategy

The original NPC converter structure is reported in Fig. 1(a). The DC link is composed of two series capacitors that share equal voltage, with $V_{DC} = V_{C1} + V_{C2}$. The neutral wire of the grid is connected to the mid-point of the DC voltage source, whereas the phase wire is connected to the filter inductor. It presents only three commutation states: P, 0 and N in Table I. Switches S_1 and S_2 commutate complementary to S_{1C} and S_{2C} respectively. During the positive half-wave of v_{grid}, S_2 is always ON whereas S_1 and S_{1C} commutate at high frequency (switching frequency f_{sw}). On the contrary, when v_{grid} is negative, S_{1C} is ON and S_2 and S_{2C} commutate complementary at f_{sw}. Therefore, when S_1, S_2 are ON the load is directly connected to the DC source and v_{out} is equal to $V_{DC}/2$ (state P). In the same way, during state N, S_1, S_2 are turned OFF and $v_{out} = -V_{DC}/2$. In 0 state both the inner switches, S_2 and S_{1C}, are ON and the load current (grid current) can pass through two different paths depending on its sign: positive grid current passes through D_1 and S_2, while the negative grid current passes through D_2 and S_{1C}.

Using this modulation technique, for each device the average switching frequency over a v_{out} period (f_{av}) is equal to $f_{sw}/2$, while the apparent switching frequency of the output voltage is $f_{ap} = f_{sw}$.

The power loss distribution among the devices is highly unbalanced and strongly dependent on the operating point and on the PWM strategy adopted [11]. For low values of the PWM duty cycle the most stressed devices are the inner switches and diodes, while for high value of the duty cycle the outer switches (S_1, S_{2C}) present the highest conduction losses.

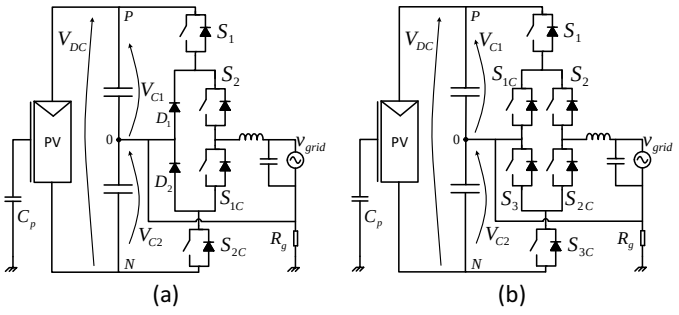

Fig. 1. NPC (a) and ANPC (b) in PV grid-tied transformerless applications.

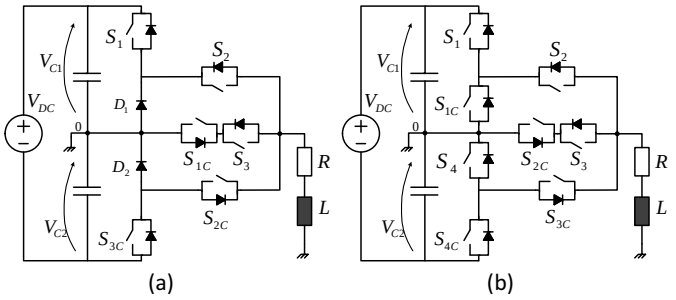

Fig. 2. SNPC (a) and ASNPC (b) architectures.

TABLE I. Switching Sequences of a NPC converter

Output Voltage	Switching State	Switching Sequence			
		S_1	S_{1C}	S_2	S_{2C}
$V_{DC}/2$	P	1	0	1	0
0	0	0	1	1	0
$-V_{DC}/2$	N	0	1	0	1

The unequal distribution of the power losses among the devices is the main drawback of the NPC topology, and its effects are particularly severe in case of medium and high power applications [17]. The ANPC converter was proposed to overcome this issue (Fig. 1(b)). Using power switches instead of diodes increases the number of degrees of freedom for the control, since it is possible to obtain more than one zero state. This redundancy can be exploited to distribute losses more evenly among the devices, as well as to improve the efficiency of the converter. It has to be noted that equalizing the loss distribution among the power devices is not the main focus of this paper. Although a better loss distribution was obtained relative to NPC, the modulation pattern proposed in this paper is mainly focused on loss reduction, as will be clear in the following.

Several PWM techniques were proposed for ANPC converters in [11]. Among them, an interesting solution doubles the apparent switching frequency of the converter output voltage ($f_{ap} = 2f_{sw}$). This modulation is taken in this paper as a benchmark to evaluate the performance of the proposed improved PWM pattern against. Employing the technique in [11] the switches S_2 and S_{2C} in Fig. 1(b) commutate complementarily at f_{sw} over the entire cycle of the sinusoidal output voltage, whereas the control of the other devices depends on the sign of v_{grid}. During the positive half-wave of the output voltage S_1 and S_{1C} commutate complementarily, S_3 is controlled synchronously with S_1, and S_{3C} is always OFF. The gate signals of S_1 and S_2 are obtained comparing the same modulation index with two different triangular carriers, phase shifted of $T_{sw}/2$. Therefore, 4 transitions between positive (negative) and zero states are obtained during a single switching period. When the converter output voltage is 0 two paths are possible for the output current: through S_{1C} and S_2 (state 0_1^+), or through S_{2C} and S_3, called state 0_2^+. The behaviour of the system during the negative half-wave is dual. The average device switching frequency is higher than in the previous case. Nevertheless, since some commutations happen in zero-voltage or zero-current conditions, f_{av} can be effectively considered

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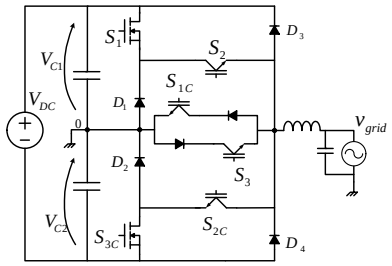

Fig. 3. Topology proposed in [15].

equal to $f_{sw}/2$ [14].

The same modulation can be used for SNPC and ASNPC converters (Fig. 2). In such cases, due to the presence of two additional devices with respect to ANPC, more converter states and configurations are possible. A solution specifically designed for PV grid-tied applications was proposed in [15] (Fig. 3). Employing CoolMOSes and IGBTs, the architecture differs from a traditional SNPC in order to avoid the conduction of the IGBTs antiparallel body diode. Only IGBTs without body diode are used, thus 4 external diodes are added with respect to Fig. 2(a), for guaranteeing the load current free-wheeling paths. Moreover, CoolMOSes are employed for the outer devices, S_1 and S_{3C} in Fig. 3, in order to achieve higher efficiency at low output power.

During the zero state the output current is divided into two parallel paths, each with a diode and an IGBT in series, thus reducing the conduction losses. The same basic concept is adopted in this paper, but the reduction of power losses is further improved by means of converter structure simplifications and the use of SiC MOSFETs.

The use of MOSFETs is particularly appealing for PV applications, since the converter efficiency is evaluated not only at the nominal converter power, but over a wide range of different load conditions. In fact, the production of energy from renewable sources is expected to be highly variable and weighted efficiency indexes, such as CEC Efficiency and EU Efficiency, that evaluate the performance of the converter at different percentage of its nominal power, are preferred. In this context, the use of MOSFETs instead of IGBTs allows to achieve high efficiency even at low output power levels, thus improving the overall converter performance. Nevertheless, due to the poor performances of MOSFET body diodes, the solutions proposed in literature adopt techniques to avoid the conduction of MOSFET body diodes, adding devices and complexity to the converter structure [18], [19]. The conduction of the body diode has proven to be not only a source of losses, but also a serious reliability issue [20]. The use of SiC MOSFETs can overcome this issue. The reverse recovery performance of SiC MOSFET body diodes is much better if compared with their Si counterparts. The modulation proposed in this paper relies on a full-SiC MOSFET ANPC structure to achieve high converter efficiency and higher European efficiency with respect to the solutions proposed so far for ANPC converters.

The proposed ANPC full-SiC MOSFET converter is presented in Fig. 4 along with the driving signals of the power

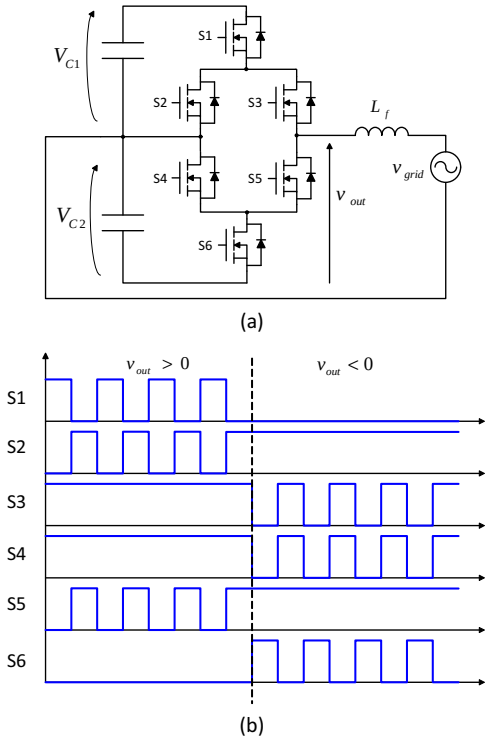

Fig. 4. ANPC Topology (a) and PWM strategy (b).

devices.

Depending on the driving signals, the possible operating states of the converter are four and are depicted in Fig. 5. During the positive half-wave of the desired output voltage, when S_1 and S_3 are ON, the converter feeds positive voltage to the output (active-state), state P in Fig. 5. The current flows through two devices in series. S_4 is ON, but it is not conducting current. When S_1 switches off, S_5 and S_2 switch on simultaneously, thus the current is divided in two paths in parallel: S_2-S_3, and S_4-S_5 (state 0^+ in Fig. 5). The voltage at the output of the converter is zero (zero-state). Similarly, when the converter feeds negative voltage, S_5 and S_6 are ON (state N). Since S_2 is also ON, the v_{ds} voltages for S_1 and S_3 are equal to $V_{DC}/2$. When S_6 is switched off the whole H-bridge composed by S_2-S_3-S_4-S_5 acts as a conduction path (state 0^-). As MOSFETs exhibit good current sharing capability, this method can ensure low conduction losses.

The fact that three devices are commutated during a switching period does not imply an increase of switching losses. As a matter of fact two devices are kept ON during the whole grid voltage half-period (e.g. S_3 and S_4 during the positive half-wave of the output voltage), while the other two (S_2 and S_5 under the same hypothesis) are gated under zero voltage switching (ZVS) conditions. Therefore this PWM strategy theoretically implies very low switching losses ($f_{av} = f_{sw}/2$) and low conduction losses as well. As in all NPC derived structures, the drawback resides in the fact that the DC link voltage must be greater than twice the grid voltage peak. As a consequence, comparatively high switching frequencies or

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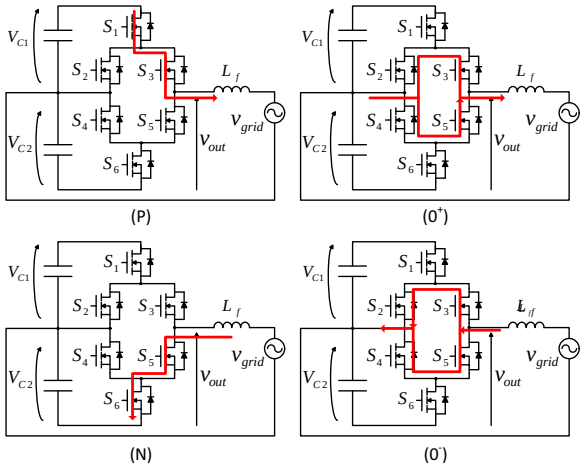

Fig. 5. Converter states.

TABLE II. SUMMARY OF THE CONVERTER'S CHARACTERISTICS

Converter topology	f_{av}	f_{ap}	number of devices
NPC	$f_{sw}/2$	f_{sw}	4 IGBTs + 2 Diodes
ANPC in [11]	$f_{sw}/2$	$2f_{sw}$	6 IGBTs
SNPC in [15]	$f_{sw}/2$	f_{sw}	2 CoolMOSs + 4 IGBTs + 6 Diodes
Full-SiC MOSFET converter with proposed modulation	$f_{sw}/2$	f_{sw}	6 MOSFETs

bulky output filter inductors must be employed to limit the output current ripple with respect to a full-bridge based PV inverter. Again, the use of SiC MOSFETs for this architecture allows to operate at high switching frequencies while keeping a fairly small inductive filter.

Moreover, it is important to note that the maximum voltage across the devices during converter operation is $V_{DC}/2$; therefore 650V SiC MOSFETs can be used, since a minimum of 700V for the DC-link voltage is required for injecting current into the grid.

The characteristics of the Full-SiC-MOSFET converter with the proposed modulation technique are resumed in TABLE II, along with characteristics of the converters taken as benchmarks for this work.

III. THEORETICAL POWER LOSS ANALYSIS

Since the efficiency of PV transformerless inverters is normally assessed using weighted efficiency measures such as CEC Efficiency and EU Efficiency, it is critical to evaluate power semiconductor device losses at different load conditions rather than at nominal load condition.

The device power losses can be divided in conduction and switching losses. The voltage drop across the device during a conduction stage can be expressed as in (1) [4]:

$$v_{con} = \begin{cases} MOS : v_{ds} = i(t)R_{ds} \\ IGBT : v_{ce} = V_t + i(t)R_{ce} \\ Diode : v_{ak} = V_f + i(t)R_{ak} \end{cases} \quad (1)$$

where v_{ds} is the MOSFET drain-source voltage drop, R_{ds} is the MOSFET drain-source on resistance, v_{ce} is the IGBT collector-emitter voltage drop, V_t is the IGBT equivalent voltage drop under zero current condition, R_{ce} is the IGBT on resistance, v_{ak} is the diode anode-cathode voltage drop, V_f is the diode equivalent voltage drop under zero current condition, R_{ak} is the diode on resistance, and $i(t)$ is the current through the device.

Considering only the positive half-wave of the output voltage active-state, the power losses over a single device are given by (2), where $i(t) = I_m sin(\omega t + \theta)$, with I_m as the peak of the inverter output current, ω its angular frequency and θ the phase displacement between grid current and voltage. D_{active} is the duty ratio for the active stage. For a grid-connected inverter the duty ratio for active state and zero-state can be expressed as (3), where M has a value comprised between 0 and 1. Combining (2) with (3) and (1), the conduction losses for a single device during the active state can be expressed as (4) for MOSFETs and IGBTs.

Conversely, the conduction power loss for a single device during zero-state is given in (5), where $i_{zero}(t)$ is used to indicate the current flowing through the device. $i_{zero}(t)$ is used for generality since, according to the adopted modulation strategy, $i_{zero}(t)$ can be equal to $i(t)$ or $i(t)/2$. Finally, in (6) the zero-state conduction losses are given for MOSFET, IGBT and diode cases, with I_{m_zero} as the peak of $i_{zero}(t)$ (I_m or $I_m/2$ depending on the modulation strategy).

$$P_{con\_act} = \frac{1}{2\pi}\int_0^{\pi} v_{con} i(t) D_{active}(t) \mathrm{d}(\omega t) \quad (2)$$

$$\begin{aligned} D_{active}(t) &= M sin(\omega t) \\ D_{zero}(t) &= 1 - M sin(\omega t) \end{aligned} \quad (3)$$

$$P_{con\_act} = \begin{cases} MOS : \frac{I_m^2 R_{ds} M}{2\pi}(1 + \frac{1}{3}cos(2\theta)) \\ IGBT : \; I_m V t \frac{M}{4} cos(\theta) \\ \qquad + \frac{I_m^2 R_{ce} M}{2\pi}(1 + \frac{1}{3}cos(2\theta)) \end{cases} \quad (4)$$

$$P_{con\_zero} = \frac{1}{2\pi}\int_0^{\pi} v_{con} i_{zero}(t) D_{zero}(t) \mathrm{d}\omega t \quad (5)$$

$$P_{con\_zero} = \begin{cases} MOS : I_{m\_zero}^2 R_{ds}(\frac{1}{4} - \frac{M(1+\frac{1}{3}cos(2\theta))}{2\pi}) \\ IGBT : \; I_{m\_zero} V_t(\frac{1}{\pi} - \frac{M}{4}cos(\theta)) \\ \qquad + R_{ce} I_{m\_zero}^2 \cdot \\ \qquad (\frac{1}{4} - \frac{M(1+\frac{1}{3}cos(2\theta))}{2\pi}) \\ Diode : \; I_{m\_zero} V_f(\frac{1}{\pi} - \frac{M}{4}cos(\theta)) \\ \qquad + R_{ak} I_{m\_zero}^2 \cdot \\ \qquad (\frac{1}{4} - \frac{M(1+\frac{1}{3}cos(2\theta))}{2\pi}) \end{cases} \quad (6)$$

For the switching losses, data sheets usually report the turn-on/turn-off energy losses of the devices, measured under precise test conditions at different junction temperatures and for given values of the switching voltage and current (V_{test}, I_{test}). In particular, for MOSFET devices, the main loss source for switching transitions is the capacitive turn-on energy loss (E_{oss}) resulting from the discharge of the

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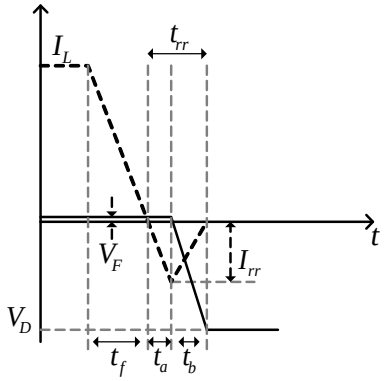

Fig. 6. Simplified diode switching waveforms during turn-off. Voltage (solid line), current (dashed).

junction capacitor C_{oss} of MOSFETs, which is dependent on the switched drain-source voltage across the device before the switch-on transition. Moreover, it is important to note that, in the case of the converters under exam, the switching voltage to consider for the calculations is $V_{DC}/2$, since the commutations happen with half the DC-link voltage. Therefore, the switching losses for a single device (MOSFET or IGBT) during a period of v_{grid} can be expressed as in (7), considering E_{on} and E_{off} from the data sheets, and normalizing them to the switching conditions considered for the measurements.

Additional switching losses in the outer devices of the ANPC/NPC structure are caused by the reverse recovery current of the inner diodes. The extra turn-on energy loss can be expressed as in (8), where t_a, t_b and I_{rr} are defined in Fig. 6, and I_L is the switched load current. Considering a sinusoidal current, the extra power losses for one outer device over a grid period are given in (9).

Conversely, the switch-off losses for the diode can be expressed as in (10), whereas the turn-on losses are neglected.

$$\begin{aligned} P_{ON} &= (\tfrac{I_m}{\pi}\tfrac{V_{DC}}{2}) f_{sw} \tfrac{E_{on}}{V_{test} I_{test}} \\ P_{OFF} &= (\tfrac{I_m}{\pi}\tfrac{V_{DC}}{2}) f_{sw} \tfrac{E_{off}}{V_{test} I_{test}} \end{aligned} \tag{7}$$

$$E_{extra\_ON} = \frac{V_{DC}}{2}(I_L + \frac{I_{rr}}{2})t_a + \frac{V_{DC}}{2}\frac{I_{rr}}{3}t_b \tag{8}$$

$$\begin{aligned} P_{extra\_ON} &= \tfrac{1}{2\pi}\int_0^{\pi} E_{extra\_ON} f_{sw} \mathrm{d}\omega t \\ &= \tfrac{V_{DC}}{4} f_{sw}((\tfrac{2I_m}{\pi} + \tfrac{I_{rr}}{2})t_a + \tfrac{I_{rr}}{3}t_b) \end{aligned} \tag{9}$$

$$\begin{aligned} P_{Diode\_OFF} &= \tfrac{1}{2\pi}\int_0^{\pi} \tfrac{1}{6} t_b I_{RR} \tfrac{V_{DC}}{2} f_{sw} \mathrm{d}\omega t \\ &= \tfrac{1}{12} t_b I_{RRM} \tfrac{V_{DC}}{2} f_{sw} \end{aligned} \tag{10}$$

A. Power Losses in NPC converters

During the active states two IGBTs in series conduct the current, whereas the current passes through one diode and one IGBT during zero states (I_{m_zero}=I_m in (6)). The outer switches S_1, S_{2C} commutate in hard switching conditions. Moreover, when they turn on, additional losses, due to the reverse recovery currents of D_1 and D_2 respectively, are present. The turn-off losses during a passage from zero to an active state have to be considered, but the turn-on losses at the beginning of a zero state can be neglected, as well as the low frequency switching losses of the inner IGBTs. All the above considerations yield the total power loss over a grid voltage period, as given in (11).

$$\begin{aligned} P_{con\_act} &= 2(2P_{con\_act}(IGBT)) \\ P_{con\_zero} &= 2(P_{con\_zero}(Diode) + P_{con\_zero}(IGBT)) \\ P_{sw} = \; & 2(P_{ON} + P_{OFF} \\ & + P_{Diode\_OFF} + P_{extra\_ON}) \end{aligned} \tag{11}$$

B. Power Losses in ANPC

With the modulation strategy proposed in [11], during a switching period, 2 active states and 2 zero states are present. Considering the positive half-wave of the desired output voltage, the succession of states 0_1^+, P, 0_2^+, P is repeated at the switching frequency. The zero-states differ because the path for the output current is different, but in both cases one IGBT and one IGBT antiparallel diode in series carry the current. During state P two IGBTs in series are ON, therefore the total conduction losses are equal to the previous case of NPC converter.

Analyzing the switching losses, it can be noted that during a transition from 0_1^+ to P, the reverse recovery losses of the antiparallel diode of S_{1C} are added to the switch-on losses of S_1 (Fig. 1b), whereas S_3 turns on under zero current switching (ZCS) conditions. When the transition from P to 0_2^+ happens, S_2 commutates in hard switching, while S_{2C} in ZVS as its antiparallel diode turns on before the device is gated. In the subsequent passage from 0_2^+ to P, the reverse recovery of the antiparallel diode of S_{2C} must be considered in the calculation of the switch-on losses of S_2. Finally, in the commutation between P and 0_1^+, only the switch-off losses of S_1 are taken into account since the turn-on of the S_{1C} antiparallel diode is considered ideal.

Therefore, it is possible to state that the total switching losses are doubled with respect to the case of NPC converter. Nevertheless, the apparent switching frequency of the output voltage is twice the previous case, and the losses are evenly distributed among all devices. The ANPC power losses are summarized in (12).

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$$
\begin{aligned}
P_{con\_act} &= 2(2P_{con\_act}(IGBT)) \\
P_{con\_zero} &= 2(P_{con\_zero}(Diode) + P_{con\_zero}(IGBT)) \\
P_{sw} = \quad & 2 \times 2(P_{ON} + P_{OFF} \\
& + P_{Diode\_OFF} + P_{extra\_ON})
\end{aligned} \tag{12}
$$

C. Power Losses in SNPC converters

For the converter proposed in [15], during active states two devices, a CoolMOS and an IGBT, are ON. During the zero state the current flows in two parallel paths, each containing a diode and an IGBT; therefore in (5), $i_{zero}(t)$ is equal to $i(t)/2$ and $I_{m\_zero} = I_m/2$.

For the switching losses, particular attention must be paid to the reverse recovery behaviour of the diodes. In this case, during a transition from zero to active states, two diodes switch off instead of only one as in the previous cases. Nevertheless, it has to be considered that the reverse recovery current amplitude (I_{rr}) depends on the amplitude of the current that is passing through the device before the switching transition; since each device conducts half of the total load current, it is possible to approximate the switching losses related to the diodes' commutations as equal to the previous cases. Furthermore, considering the presence of a CoolMOS as outer device, the total losses are given in (13)

$$
\begin{aligned}
P_{con\_act} &= 2(P_{con\_act}(IGBT) + P_{con\_act}(MOS)) \\
P_{con\_zero} &= 2 \times 2(P_{con\_zero}(Diode) + P_{con\_zero}(IGBT)) \\
P_{sw} = \quad & 2(P_{ON} + P_{OFF} \\
& + P_{Diode\_OFF} + P_{extra\_ON})
\end{aligned} \tag{13}
$$

D. Power Losses with the Proposed Modulation

During the active states two devices are on, as before. During the zero-state the devices S_2, S_3, S_4, S_5 are ON, the current is equally divided in two parallel paths: through the series S_2-S_3, and the series S_4-S_5 ($I_{m\_zero} = I_m/2$). Therefore, it is possible to account the conduction power losses as the current would flow through a single device with on-state resistance equal to R_{ds}. Furthermore, as a dead time is inserted in the commutation signals, there is a short interval in which the current is flowing through the MOSFET antiparallel diode, causing additional losses. Considering a dead time t_{dt} of 250 ns the additional losses for a half period of the grid voltage are expressed in (14).

$$
\begin{aligned}
P_{con\_dt} = \quad & (I_{m\_zero} V_f (\tfrac{1}{\pi} - \tfrac{M}{4}) \\
& + I^2_{m\_zero} R_{ak} (\tfrac{1}{4} - \tfrac{2M}{3\pi})) t_{dt} f_{sw}
\end{aligned} \tag{14}
$$

For the switching losses, considerations are similar to the SNPC converter. The main difference in this case resides in the use of SiC devices, that have a less marked reverse recovery behavior with respect to traditional Si devices; therefore the total switching losses are expected to be very low.

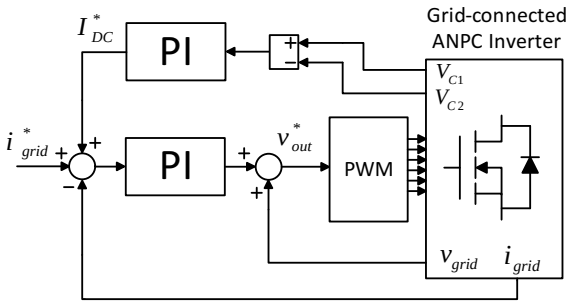

Fig. 7. Block scheme of the current control.

The total losses are resumed in (15).

$$
\begin{aligned}
P_{con\_act} &= 2(2P_{con\_act}(MOS)) \\
P_{con\_zero} &= 2 \times 2(2P_{con\_zero}(MOS) + P_{con\_dt}) \\
P_{sw} = \quad & 2(P_{ON} + P_{OFF} \\
& + P_{Diode\_OFF} + P_{extra\_ON})
\end{aligned} \tag{15}
$$

IV. Simulation Results and Power Loss Calculations

The proposed modulation was simulated in the MATLAB/Simulink environment with the PLECS toolbox. The simulation circuit reflects the schematic of Fig. 4(a), with $L_f = 1$ mH, the equivalent capacitance of one half of the DC link $C = 2$ mF, and considering 800 V for the total DC link voltage.

The control of the converter is shown in Fig. 7, where a simple Proportional-Integral (PI) regulator is used to control the injected grid current. The grid voltage is added after the regulator as a feed-forward term. The balancing of the DC link capacitor is realized with a PI regulator that control the DC component of the grid current. If the injected grid current has no DC component and the capacitor voltages are balanced, the power drawn from each capacitor is equal. This also ensures that no DC current is injected into the grid. This aspect is of paramount importance, because the DC current injection from grid-connected converters must respect strict limits imposed by international regulations.

Fig. 8 shows the grid voltage and current when 3 kW of active power is delivered to the grid, with a switching frequency $f_{sw} = 40$ kHz.

In Fig. 8 the output voltage does not have flat tops because the capacitor voltages are changing within the grid voltage period. As a matter of fact, in unity power factor condition, the output is connected to the upper half of the DC link during the positive half-wave of the grid voltage, and to the lower half otherwise. This causes a voltage change over the 10 ms of the half wave, which is visible in the simulations.

The total losses of a full-SiC-MOSFET converter, that features the proposed modulation strategy, were calculated

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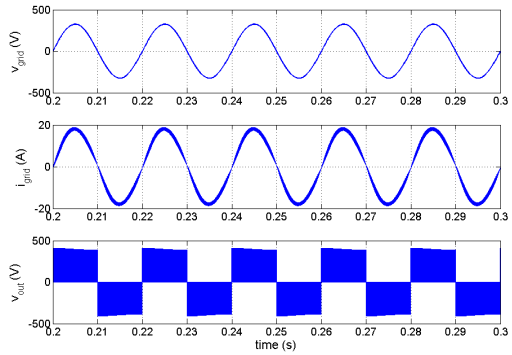

Fig. 8. Simulation results.

TABLE III. DEVICE PARAMETERS AT 25 °C

Device	R_{ds}/R_{ce} $m\Omega$	V_t V	V_f V	R_{ak} $m\Omega$	I_{rr} A	t_a ns	t_b ns
IGBT STGW35HF60WDB	15	1.7	0.75	75	3	29.4	20.6
SiC MOSFET SCT2120AF	120	-	1.4	290	3	17	16
CoolMos IPW60R045CP	45	-	-	-	-	-	-
Diode FFP30S60S	-	-	0.8	80	2.4	14	14

according to the formulae in Section III, for different values of delivered output power. The power losses were evaluated considering the parameters of TABLE III and compared with those of NPC, ANPC and SNPC converters.

Moreover, in order to highlight the advantages of employing MOSFETs instead of IGBTs, the power losses using the proposed modulation with an ANPC converter adopting IGBTs as the main switches, were calculated as well.

CoolMOS IPW60R045CP and soft switching diodes FFP30S60S were considered for the SNPC topology, as indicated in [15]. The adopted IGBTs are STGW35HF60WDB by STMicroelectronics, and the performance of their antiparallel body diode was also used for the single diodes of the NPC structure. The SiC MOSFETs were 650 V SCT2120AF by ROHM Semiconductor.

In Fig. 9 the power losses calculated for the converters under exam are displayed at different percentages of the nominal converter power of 3 kW. In particular, it can be observed that the full-SiC MOSFET ANPC converter with the proposed modulation strategy exhibits the highest efficiency at 10, 30, 50 percent of the nominal power, due to the better performance of MOSFETs at light load. At full power the SNPC, thanks to the very low on-state resistance of CoolMOSes, has almost the same efficiency as the proposed solution. Nevertheless, the performance of the proposed modulation remains higher than those of the other converters, but the benefits in employing MOSFETs instead of IGBTs are lower, because at 3 kW the performances of the chosen IGBTs are similar to those of the SCT2120AF SiC MOSFETs.

Moreover the zero-state conduction losses, thanks to the proposed modulation technique that enables the parallel operation of the MOSFETs, are the less significant in any case. Further benefits to the efficiency can be expected when the converter operates under non-unity power factor conditions. The switching losses are very low as can be expected with SiC devices, thus it can be stated that the total efficiency of the converter will not be highly dependent on the switching frequency in the range of considered switching frequencies (10-40 kHz).

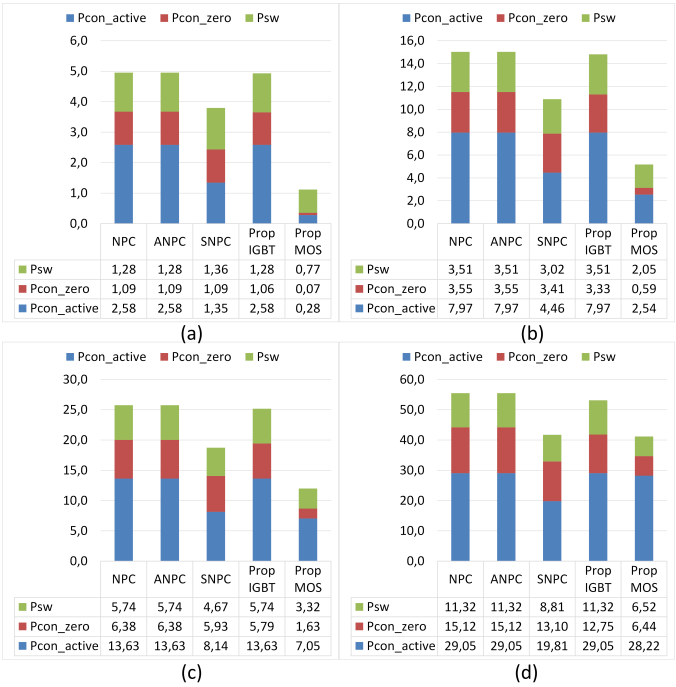

Fig. 9. Theoretical power losses of NPC, ANPC, SNPC and the proposed modulation with IGBT or SiC devices at 10%(a), 30%(b), 50%(c) and 100%(d) of the 3 kW nominal power.

TABLE IV. EUROPEAN AND CEC EFFICIENCY

Converter topology	European Efficiency	CEC Efficiency
NPC	98.3%	98.2%
ANPC in [11]	98.3%	98.2%
SNPC in [15]	98.7%	98.7%
Prop. Modulation with IGBT	98.3%	98.3%
Prop. Modulation with SiC	99.1%	99%

The ratio between the conduction active-state and zero-state losses depends on the ratio between the DC link voltage and the grid, since, for a given value of desired output current, the duration of the freewheeling state (zero-state) is larger when the DC source voltage is higher.

The calculated European efficiency and CEC efficiency for the converters under exam are reported in TABLE IV.As can be seen, the full-SiC MOSFET ANPC with the proposed modulation exhibits the highest efficiencies thanks to the better performance at low power.

A. *Discussion on the power losses of the different topologies*

As can be seen from Fig. 9, the NPC and ANPC have the same losses, if the comparison is done with the same output

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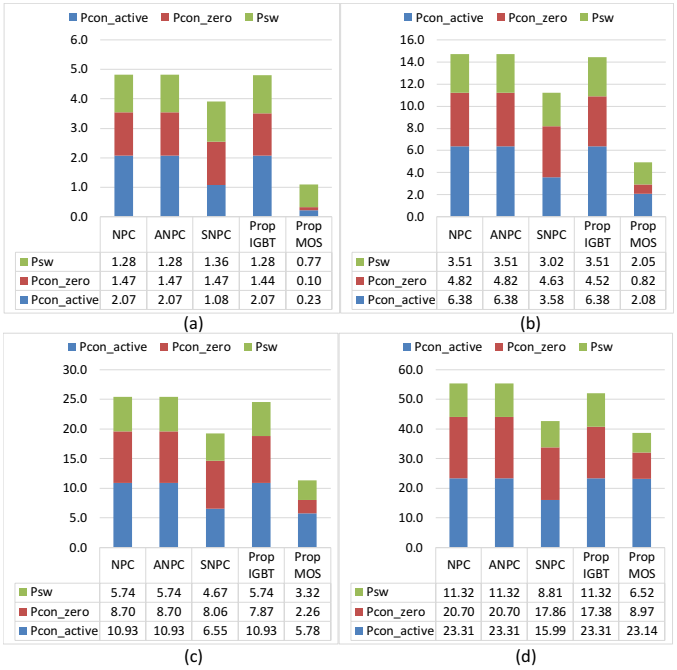

Fig. 10. Theoretical power losses of NPC, ANPC, SNPC and the proposed modulation with IGBT or SiC devices at 10%(a), 30%(b), 50%(c) and 100%(d) of the rated full current and power factor = 0.8.

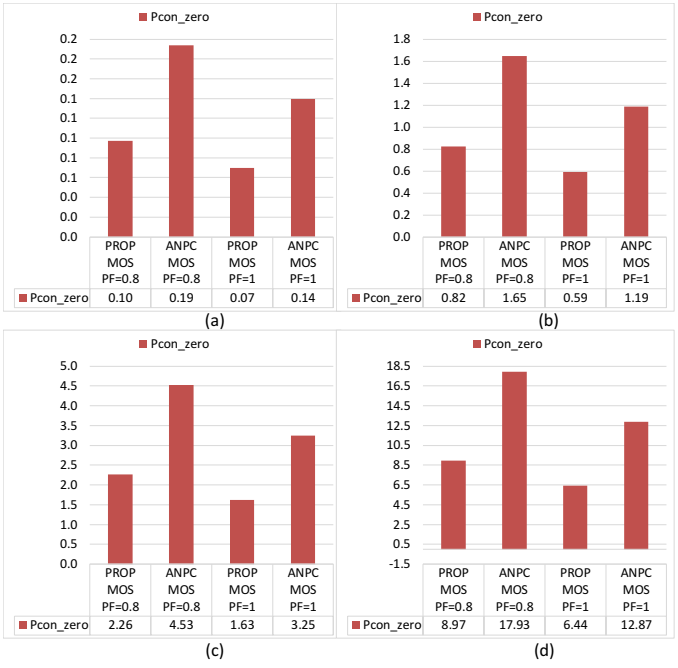

Fig. 11. Comparison between ANPC with SiC and ANPC with SiC and proposed modulation at 10%(a), 30%(b), 50%(c) and 100%(d) of the rated full current and different power factors.

THD. The benefits of the proposed PWM when Si devices are used are not evident, due to the threshold behavior of the bipolar devices, that show a constant component of the on-state voltage drop even at low current levels. The SNPC benefits from the adoption of the CoolMOSes, with a more complex architecture. However, if the operation is constrained to unity power factor, the adoption of CoolMOSes for high and low side devices is feasible even for the standard NPC.

What is important to highlight is that the adoption of SiC MOSFETs and the proposed PWM allows to greatly reduce the conduction losses during the zero state, even considering devices with a smaller package (TO220 against TO247).

B. Benefits of the modified PWM with non-unity power factor operation

References (2) and (6) show a dependency of the active and zero states conduction power losses to the phase displacement θ between grid current and voltage. In particular, regardless of the considered converter topology, as the power factor decreases the zero state conduction losses increase whereas those in active states decrease. This because there are more zero states facing a higher value of grid current relative to the case of unity power factor. Since grid connected converters have been recently requested to inject into the grid also a certain amount of reactive power, the converter efficiency in case of non-unity power factor must be taken into account to correctly evaluate the converter performance.

Fig. 10 reports the calculated losses for the converters under examination in case of $PF = 0.8$ and the same current amplitude considered for the data in Fig. 9. As can be seen, the ANPC coverter with SiC MOSFET and the proposed modulation is the one that performs better. In this case the impact of the proposed modulation on the converter efficiency is more evident as the conduction losses during zero states counts more relative to the total losses. SNPC maintains the lowest active conduction losses but, in comparison to the full SiC ANPC with the proposed modulation, pays more losses during zero states, resulting in a lower efficiency.

For the sake of completeness, in Fig. 11 an evaluation of the loss reduction achievable with the proposed modulation against the other ANPC solutions is performed. As can be seen, the losses during the zero state are exactly half, and the advantage is more evident considering non-unity power factors.

V. Experimental Results

The experiments were performed with a prototype converter based on the Freescale MC56F8323 MCU. The converter generates the power supplies needed for the logic and the gate driver circuits from the DC link. The DC source used was a DC Power supply that provides 700 V with up to 2 kW of continuous power. The converter output was connected to the secondary of an isolation transformer with 230 V rms and 50 Hz at the point of connection. Fig. 12 shows the output current and voltage in case of unity power factor (PF) and 2 kW of delivered output power for two different values of the switching frequency. Differently from the simulations, the grid voltage shows a marked third harmonic distortion. This behavior is quite common in the low-voltage grids, because

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of the widespread adoption of diode-bridge rectifiers as input stages. This third harmonic distortion causes also a small low-frequency distortion in the grid current, that could have been compensated with a more complex architecture of the current controller. However, the optimization of the current controller under distorted grid voltage is outside the scope of the paper.

The efficiency measurements were done with a N4L PPA5530 power analyzer, measuring the DC input power and the output power after the filter inductor, excluding the transformer losses.

The performance of the converter was evaluated both with the ROHM Semiconductor SCT2120AF SiC MOSFETs and the STMicroelectronics STGW35HF60WDB silicon IGBTs, for switching frequencies of 10, 20 and 40 kHz and different temperatures of the heat sink (25, 50, 75, 100 degrees Celsius for the SiC MOSFETs, up to 75 C for the IGBTs to avoid exceeding the maximum rated junction temperature).

In this work, the authors decided to perform the comparison considering the same heatsink temperature, while a fairer comparison would have been achieved considering the same junction temperature. However, the junction temperature is not directly measurable in an easy way, for this reason the heat sink temperature was controlled. This choice has consequences that need a supporting discussion.

As a premise, since different devices carry a different current during the grid voltage period, it is safe to assume that the junction temperatures will have some differences even inside the same test case (Si or SiC), making a test under the same junction temperature not feasible. The STGW35HF60WDB device presents a thermal resistance junction-case of 0.63 C/W for the IGBT and 1.5 C/W for the diode, while the SCT2120AF has 0.7 C/W. Considering that the results were obtained under unity power factor, the diode conduction happens only during the zero state. The zero state is applied for a longer time when the grid current is low, so it can be concluded that the diode losses constitute a small part of the total losses.

As an approximation, it is safe to say that the Si and SiC devices have similar thermal impedance, also considering that a very important thermal resistance contribution is given by the thermal pad between the case and the heatsink. Under these assumptions, Si and SiC devices will have similar junction temperature when the losses are similar. Since an on-line control of the junction temperature or of the losses is not feasible, if the trials are done under the same heat-sink temperature, the SiC and Si devices will have similar expected junction temperatures at 1.5 kW, while the SiC will benefit from the lower losses in the low power range.

A flyback converter directly connected to the DC link is used to generate the auxiliary power supplies, and these losses are included in the input power. The magnitude of these additional losses was measured to be 12.5 W when the converter is operating at 10 kHz. Considering that the auxiliary power supply losses and the output filter are kept the same for both IGBT and SiC converters, this has an impact on the maximum efficiency. For this reason, the measures must be read comparing the gain that can be achieved by employing SiC devices.

Differently from the theoretical analysis of Fig. 9, the losses on the converter output filter and auxiliary supply were included in the experimental measurements. Furthermore, the maximum converter output power was limited to 2 kW due to the DC power supply.

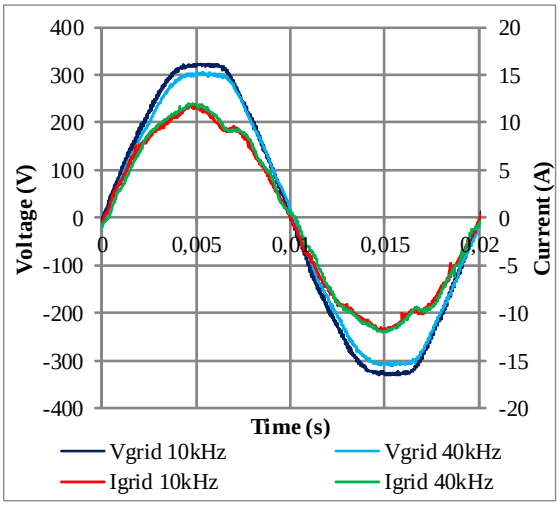

Fig. 12. Grid voltage and current in case of 2 kW of delivered output power with f_{sw} equal to 10 and 40 kHz.

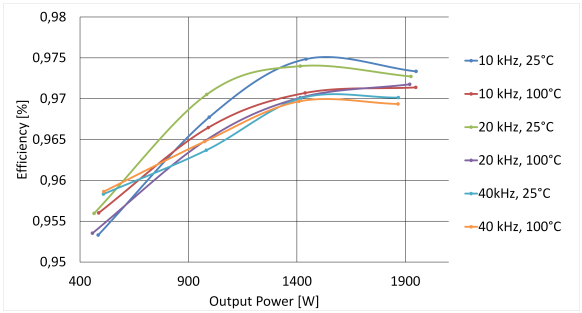

Fig. 13. Total efficiency of the ANPC converter with SiC MOSFETs as a function of switching frequency and operating temperature.

Fig. 13 reports the measured efficiency curves for the ANPC converter with SiC MOSFETs, while Fig. 14 refers to the

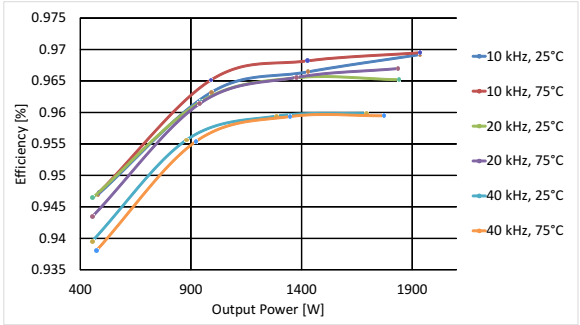

Fig. 14. Total efficiency of the ANCP converter with silicon IGBTs as a function of switching frequency and operating temperature.

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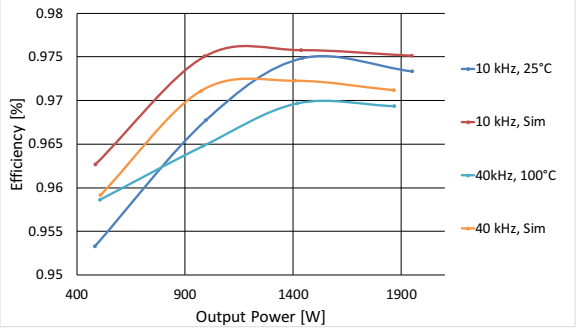

Fig. 15. Comparison between simulated and experimental efficiency of the ANCP converter with SiC MOSFETs.

use of silicon IGBTs. The advantage of the SiC MOSFETs is evident, especially at fractional power and at high temperature. The SiC MOSFETs maintain better performances than the IGBTs even though they come in a TO-220 package, smaller than the TO-247 of the IGBTs. Using SiC MOSFETs, the switching frequency can be doubled achieving roughly the same efficiency as with silicon IGBTs. This result is in good agreement with similar measurements presented in literature [21].

Finally, Fig. 15 reports a comparison between the simulated total efficiency of the full SiC ANPC converter, taking into account also the simulated losses in the filter inductors (copper and iron losses) and the logic losses, and the total efficiency measured throughout the experimental results. As can be seen, the simulated efficiency is slightly higher than the measured one. This can be due to the mismatch between the junction and heatsink temperatures and to other unmodeled loss sources, i.e., the capacitors ESR.

VI. Conclusion

In this paper an improved modulation for an active NPC inverter equipped with 650 V SiC MOSFETs was proposed. The proposed modulation reduces conduction power losses thanks to the parallel operation of the MOSFETs during the free-wheeling intervals. A theoretical analysis of the power losses for different percentages of the nominal output power of the converter was presented in order to evaluate the European efficiency. Moreover, a performance comparison with NPC, ANPC, SNPC inverters was included. For evaluating the actual advantages of using SiC MOSFETs, a comparison with the performance obtained by the same modulation driving an ANPC converter with IGBTs was provided as well. The proposed modulation was proven to yield the greatest benefits if adopted to drive MOSFETs. Furthermore, the SiC MOSFETs maintain better performance at higher frequencies and temperatures, even though they come in a TO-220 package smaller than the TO-247 of the IGBTs. Better performances are obtained with smaller devices, increasing the power density of the converter. Considering also that the size of the output filter can be reduced by increasing the switching frequency thanks to the low switching losses of SiC devices, the advantages of employing the proposed modulation with a full SiC MOSFET ANPC converter are evident.

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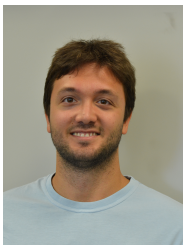

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